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Voltage and current Harmonics compensation in Micro grid Using Adaptive Nuero Fuzzy Logic Controller of Dual –Interfacing-converters

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Abstract: *During this paper charge of neighborhood load harmonic current compensation is utilizing one DG interface convertors could create the intensification of supply voltage harmonics delicate burdens, in the main once the basic grid voltage is incredibly mutilated. Dissimilar to the operation and generation of unified power quality conditioners (UPQC) with arrangement convertor, another harmonic current provide voltage and grid current harmonic play methodology is planned a utilizing facility to dominant of those shunt interfacing converters. especially, the first convertor is responsible of neighborhood offer voltage at load harmonics square measure reduction. Another convertor is used to alleviate the harmonic current created by the communication between the first interfacing convertor and also the near nonlinear load. here perceive basic dominant and command of those coincidental converters, associate altered mixture voltage and current controller is in addition created within the discussion of paper. Utilizing of this introducing controller, the grid voltage stage locked circle and identification of the heap current and also the provide voltage harmonics square measure pointless for each interfacing converters. during this method, the machine heap of interfacing converters may be basically lessened.*

Key terms : *power quality, dynamic voltage restorer, resonance, phase loop locked, active power filter, harmonic detection, LCL filter.*

I. Introduction

Here we tend to promoting requests of utilizing an influence modeling circuits in medium and low voltage management current system. contrastive with large detached filters that square measure terribly touchy to circuit perameters varieties, the dynamic power modeling hardwares square measure mix with dynamic voltage renovator (DVR), Active power filter (APF) and unified power quality conditioner (UPQC) is favored thanks to this part reactions and also the nice resistance to the system perameter modifying. Then again, the high entrance of distributed generation (DG) unit with interfacing convertor of power devices offers the chance of power appropriation system harmonic current compensation of multi interfacing converters.

Past research predominantly centered around the control of a single DG shunt interfacing converter as an APF, as their energy devices circuits have comparative structure. To understand an upgraded dynamic separating objective, the ordinary current control techniques for grid tied DG interfacing converter might be adjusted. To start with, the wide data transfer capacity current controllers are utilized so that the frequencies of harmonic load current can fall into the transmission capacity of the using controller. On the other hand, the particular frequency harmonic pay utilizing multi-resounding current controller has gotten a consider generation measure of constrictions, as detailed. In the killjoy controller is created for different DG units with dynamic harmonic separating capacity. In the neural system strategy is utilized to enhance the harmonic separating execution of DG interfacing converters that are associated with a grid with substantial variety of grid impedance. Notwithstanding the pay of harmonics at low voltage dissemination arranges, the dynamic separating of music in higher voltage circulation system utilizing multi-level converters. Nonetheless, it is critical to note that previously mentioned compensation strategies are primarily utilized as a part of grid tied converter systems.

II. Analyzation of DVR and APF

This place is quickly calculate the management of shunt APFs for network current harmonic alleviation and arrangement DVRs for provide voltage harmonic reduction. The distinction and also the introducing concurrent-converter is employed to adjusted half and half current and voltage controller as appeared within the following space, the sure enough knew double-loop current management and voltage management square measure connected to APFs and DVRs, individually.

A. parallel participating Convertors for Grid Current Harmonic Minimization

Fig.1 demonstrates the structure associated system of an interfacing convertor for compensating generation harmonic current from an area of un balanced load. To start out with, the neighborhood load is related to the final result of the interfacing convertor, and afterwards, they're coupled to the first network through the grid feeder.

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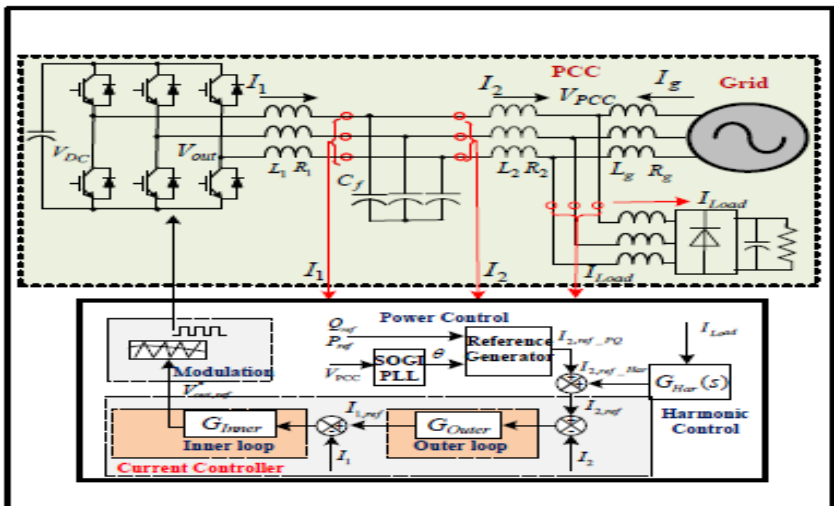

Fig.1. Diagram of local harmonic compensation using interfacing converter

The parameters of network feeder and interfacing converter LCL filter are recorded is $z_1(s) = sL_1 + R_1$, $z_2(s) = sL_2 + R_2$, $z_3(s) = 1/(sC_f)$, and $z_g(s) = sL_g + R_g$, where L_1,L_2 is the inductance and R_1,R_2 is the resistance of the filter arrangement stifles, C_f is that the capacitance of the parallel condenser, and L_g is grid inductance and R_g is square measure grid resistance

$$I_{2ref_h}=H_{Har}(S).I_{Load} \quad (1)$$

Here $H_{Har}(s)$ is exchange capacity of the harmonic segment indicator and $ILoad$ is the nearby load current. At the point when these two key and the harmonic parts are resolved, the reference current is acquired as $I_{2ref}= I_{2ref_f} + I_{2ref_h}$ and it is utilized as the contribution .

$$I_{1,ref}=H_{outer}(S).(I_{2,ref}-I_2) \quad (2)$$

$$V_{outer.}* = H_{inner}(S).(I_{1,ref}-I_1) \quad (3)$$

Here $H_{Outer}(s)$ is the external controller loop and $H_{Inner}(s)$ is the internal control loop of controllers. The $I_{1,ref}$ is the reference and I_1 is the quick invertar output current, separately. $V_{out,ref}$ *is the final voltage reference of the invertar.

B. Series participate convertor for final Voltage Harmonic reduction

The Point of coupling voltage was calculated by Dynamic voltage regulator. The central and PCC voltage segments are isolated. At that time, the provision voltage harmonic components is repaid by fixing the harmonic voltage reference of the DVR as $V_{refh} = V_{PCCh}$ and also the basic voltage reference V_{reff} of the DVR is resolved by the droop and swell compensation necessity of the system .At the purpose once the central and harmonic half references square measure resolved, the DVR reference voltage is gotten as $V_{C,ref}= V_{C,ref\ f} + V_{C,ref_h}$. a short while later, a double-loop voltage management is connected to ensure a fast voltage following is

$$I_{1\ ,ref} = H_{outer}(S).(V_{c,ref} - V_c) \quad (4)$$

$$V_{out.,ref} = H_{inner}(S).(I_{1,ref} - I_1) \quad (5)$$

III. THE INTRODUCING COORDINATED MANAGEMENT TECHNIQUE

Here we've a harmonic current alleviation of the grid current hormones and provide voltage compensation technique utilizing expedited management of two concurrent interfacing convertors is introduced during this section. The hardware and management outlines of the projected system area unit appeared in fig.2 and fig.3, singly. at the start a DG unit with two coincidental interface convertors having an identical DC rail is related to the PCC. each interfacing convertor having a output LCL filter and also the close nonlinear hundreds are place at the output electrical phenomenon filter of converter1. during present topology, the provision voltage to neighborhood local load is upgraded to dominant within the harmonic a part of interfacing converter1.

A. Controlling calculation for Converter1

To start with, the road current $I2$,c1 of convertor1 and $VPCC$ are appeared in fig.2 square measure calculate to the real and receptive output power of this convertor.

$$\begin{cases} P_{C1} = \frac{3\tau}{2(S+\tau)}(V_{PCC,\alpha}.I_{2\alpha,C1} + V_{PCC,\beta}.I_{2\beta,C1}) \\ Q_{C1} = \frac{3\tau}{2(S+\tau)}(V_{PCC,\beta}.I_{2\alpha,C1} + V_{PCC,\alpha}.I_{2\beta,C1} \end{cases} \quad (6)$$

Here P_{C1} and Q_{C1} be the output real and receptive convertor1 power, $V_{PCC,}$ and $V_{PCC,\beta}$ area unit the PCC voltage and $I_{2\alpha,C1}$ and $I_{2\beta,C1}$ be the converter1 line current, and the time τ constant of low pass filters. The time steady of the LPF is for the foremost half controlledby 2 elements. Herestart with, the real and receptive power swells brought on by line current music should be befittingly sifted through. Besides, the short part management ought to be well-kept. As per the define rule.

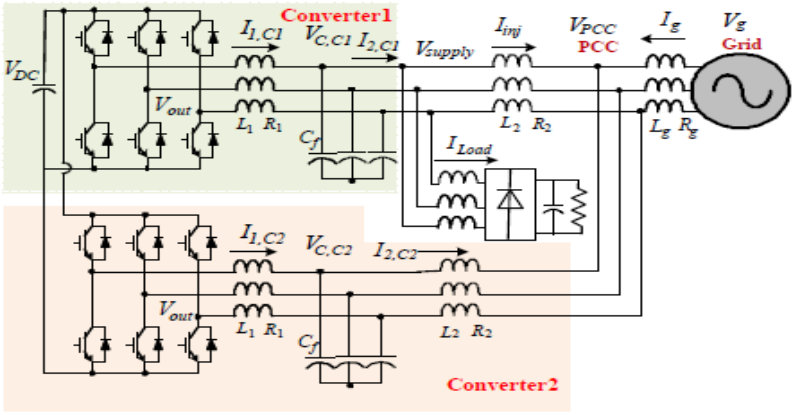

Fig. 2. Diagram of the proposed topology.

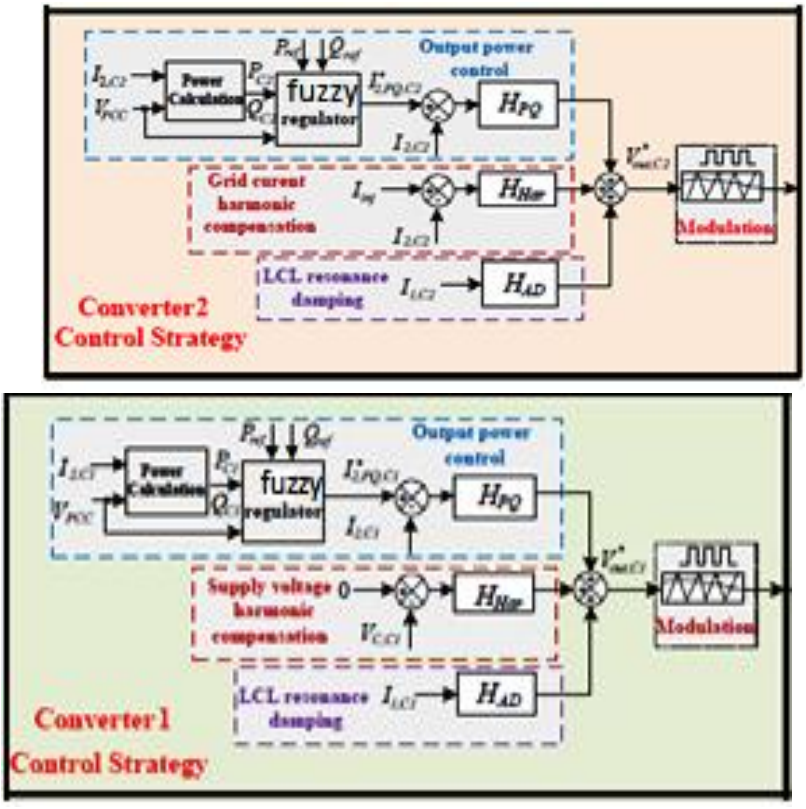

Fig.3. Diagram of introducing the interfacing converters control strategy

Here the power reference is generation decided by the accessible power from the rear part of the metric weight unit. At the purpose here there's a vitality of reposition system in metric weight unit. The facility reference will likewise be controlled by the vitality administration arrangement a small grid. on these lines, for straight forwardness, the harmonic pay administration is usually initiated here there's adequate power rating in interface of convertors. The final value of the facility reference generation is that the line current reference.

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$$I_{2,\,PQC1}^{*} = G_p.(V_{PCC,\,\alpha} + jV_{PCC,\,\beta}) + G_Q.(V_{PCC,\,\beta} - jV_{PCC,\alpha}) \quad (7)$$

The additions g_p and g_Q in are controlled by two ANFIS controllers as

$$\begin{cases} Gp = \left(Kp_pq + \frac{KI_{PQ}}{S}\right).(Pref - PC1) \\ Gq = \left(Kp_{PQ} + \frac{KI_{PQ}}{S}\right).(Qref - Qc1) \end{cases} \quad (8)$$

Where k_{ip}, and k_i, be the ANFSI controller coefficients. P_{ref} is the reference genuine and Q_{ref} is the receptive power, individually. Here this converter in charge of repaying harmonic parts of the provide voltage, the controlers in the half breed voltage and current controler is changed with harmonic supply voltage control and central line current control as in equation (9)

$$V_{OUT,C1}^{*} = H_{PQ}(S).(I^{*}_{2,PQ,C1} - I_{2,C1}) + H_{Har}(S).(V^{*}_{C,C1} - V_{C,V1}) + H_{AD}(S).I_{1,C1} \quad (9)$$

Here $V_{out,1}$* is voltage reference for the PWM preparing, $I_{2,PQ,C1}$* is the reference line current of the Power Controlling term. $V_{C,C1}$* is the voltage reference of the Harmonic Voltage Minimization term, $V_{C,C1}$ is the capacitive filter voltage, and $I_{1,C1}$ is the output current of converter1. The controllers of the Power Control, Minimization of Voltage Harmonics and Active Damping terms are recorded as

$$H_{PQ}(S) = K_{P1,C1} + \frac{2K_{i,f,c1}W_cS}{S^2 + 2\omega_C S + \omega_0^2} \quad (10)$$

$$H_{Har}(S) = K_{P2,C1} + \sum_{h=5,7,1,13} \frac{2K_{v,h,C1}\omega_c S}{S^2 + \omega_C S + h.w_0{}^2} \quad (11)$$

$$H_{AD(}S) = K_{AD,C1} \quad (12)$$

Here $k_{p1,C1}$ is that the relative develop and $k_{i,f,C1}$ is that the thunderous of controlers develop for power dominant controller of $H_{PQ}(s)$,$k_{p2,C1}$ is that the corresponding addition and $k_{v,h,C1}$ is the full controler develop for the voltage harmonic relief controler $H_{Har}(s)$, and $k_{AD,C1}$ is that the relative controler which will effectively stifle LCL filter reverb generation. This necessary to notice that alone the essential relative additions$k_{p1,c1}$ and $k_{p2,C}$1be the abundant less than the total dominant develop $k_{v,h,C1}$consequently.

The output of the facility management term on (9) has low harmonic half. Attributable to this part, thecontortednetworkvoltage willbe straightforwardly utilized because the contribution in (7), its harmonic half will be naturally sifted through with (10).

B. Controlling calculation for Converter2

The controling procedure of converter2 is equally converter1, as to boot exhibited in fig.3 Be that because it could, the elemental and therefore the harmonic convertor streams area unit to be controlled. within the 1st place, the controler as appeared on (6) to (8) area unit embraced to urge the reference of power control term $I_{2\alpha,1}$ and $I_{2\beta,C1}$ area unit the converter1 line current, and τ for converter2. after, another mixture controler is used to grasp the shunt circle convertor line current control of two is:

$$V_{out,c2}^{*} = H_{PQ}(S).(I_{2,PQ,C2}^{*} - I_{2,C2}) + H_{Har}(S).(I_{2,Har,C2}^{*} - I_{2,C2}) + H_{AD}(S).I_{1,C2} \quad (13)$$

Here $V_{out,2}$* is reference converter2 of voltage PWM handling,$I_{2,PQ,C2}$*is the present reference for converter2 control, $I_{2,Har,C2}$*is the present reference for line current harmonic control of converter2, $I_{1,C2}$ is the output current of converter2.theCurrent Harmonic Minimization, Power Control and Active Damping terms are recorded is

$$H_{PQ}(S) = K_{P1,C2} + \frac{2K_{i,f,c2}W_cS}{S^2 + 2\omega_C S + \omega_0^2} \quad (14)$$

$$H_{Har}(S) = K_{P2,C2} + \sum_{h=5,7,1,13} \frac{2K_{v,h,C2}\omega_c S}{S^2 + 2\omega_C S + h.w_0{}^2} \quad (15)$$

$$H_{AD(}S) = K_{AD,C2} \quad (16)$$

Here same to converter1, he Current Harmonic Minimization term and the Power Control term are exceptionally very much decoupled. In this manner, PLLs is a bit much and the contribution of Power Control term I_{pqc2}*can have a few bends when utilizing an immediate duplicate of PCC voltage. In rundown, the introduced topology and the altered cross breed controlling can understand an upgraded nature of supply voltage to the neighbor Stack and the primary system of grid current to in the meantime. Series system of grid current to in the minimum time.

C. Frequency Domain Analysis

here both converter2 and converter1 have frequency specific element in the major and they chose. The harmonic frequency of supply voltage harmonic and compensation of system current harmonic executed can be analyzed by frequency area investigation utilizing Bode plots. Initial, a LCL filter of a converter is displayed in fig.5. Where the neighborhood load is disentangled as a harmonic current source is associated with the converter LCL filter of shunt capacitor of. The reaction of the filter plant is given as

$$\left(\frac{V_{out}}{Z_1}+\frac{V_{PCC}}{Z_2}-I_{Load}\right).\left(\frac{1}{z_1}+\frac{1}{z_2}+\frac{1}{z_c}\right)=V_c \quad (17)$$

$$v_{out} - v_c = z_1.I_1 \quad (18)$$

$$V_C - V_{PCC} = Z_2.I_2 \quad (19)$$

In light of the control methodologies on(9) and(13), the exchange capacity of the LCL filter circuit (see (17) to (19)) for both converter1 and converter2, and expecting that $V_{out,C2}^* = V_{out,C2}$ and $V_{out,C1}^* = V_{out,C1}$, the shut circle current and voltage reaction of parallel converters can be set up. as harmonic frequencies.

$$V_{C,C1}=R_{11}(S)V_{C,C1}^*+R_{12}(S)I_{2,PQ,C1}^*-R_{13}(S)I_{2,C1} \quad (20)$$

$$I_{2,C1}=R_{21}(S)V_{C,C1}^*+R_{22}(S)I_{2,PQ,C1}^*+R_{13}(S)V_{PC} \quad (21)$$

$$I_{2,C2}=R_{31}(S)I_{2,PQ,C2}^*+R_{32}(S)I_{2,PQ,C2}^*-R_{33}(S)V_{PCC} \quad (22)$$

Where the coefficients $R_{11}(s)$ to $R_{33}(s)$ in portray the reaction of these two converters. to different excitations of converter1 of the system. In particular on(20) predominantly centers the execution.

IV. Using PI Controller Series and Shunt Compensation Simultaneously

4.1 Harmonic Compensation Using PI Controller

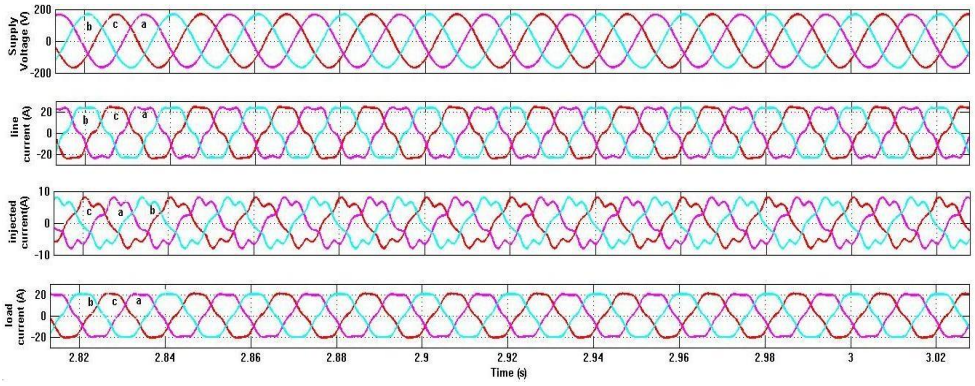


Fig.4. Performance of converter with PI (From up to down: V_{supply}, I_2,c_1,I_{inj}, I_{Load})

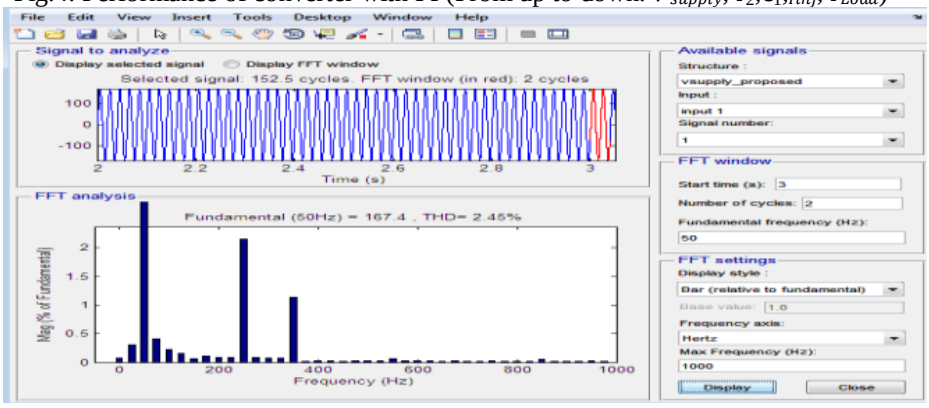


Fig.5. Supply voltage of FFT analysis and THD using PI controller

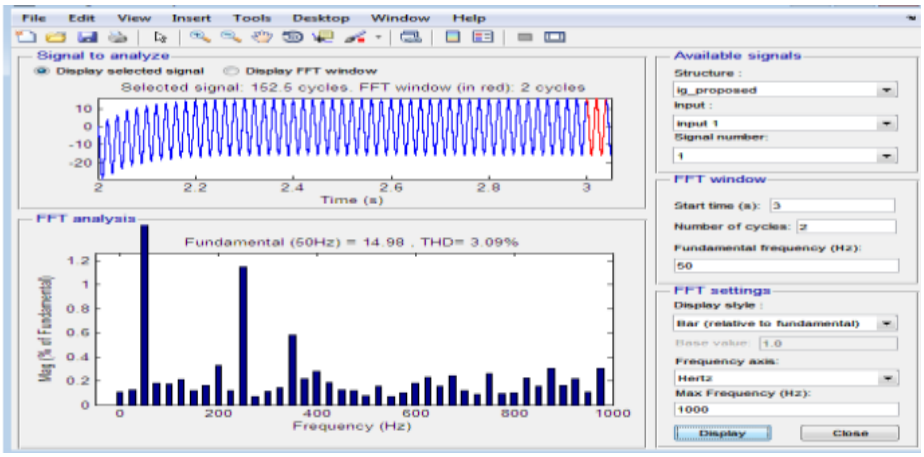
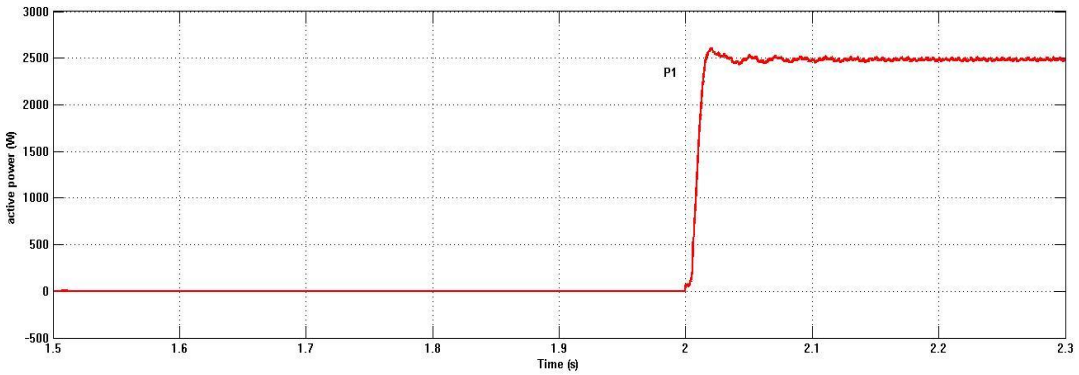
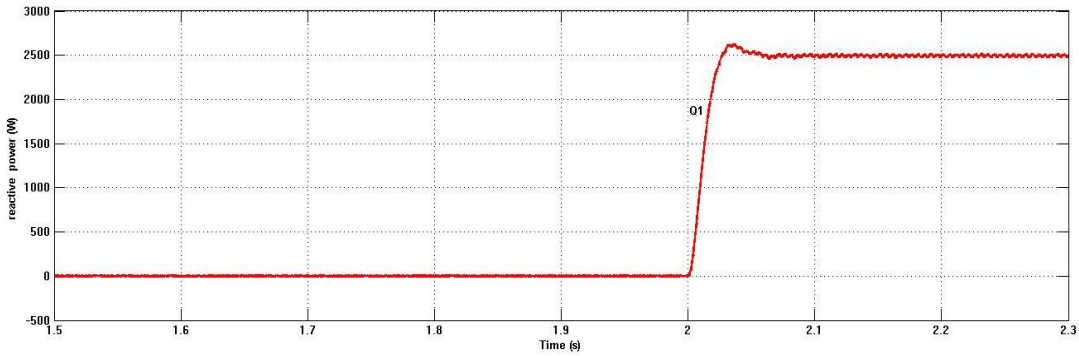
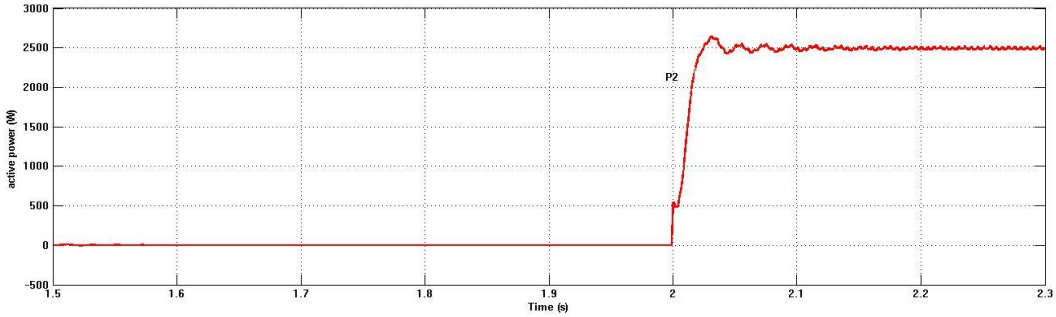


Figure 6: Grid Current of FFT analysis and THD using PI controller

4.1.1 Real and reactive power of converter1 and converter2 with PI controller







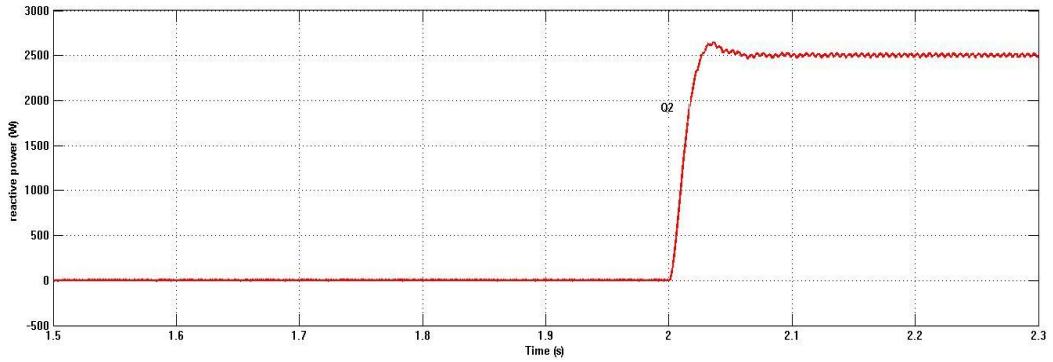


Figure 7: Active and reactive power of converter1and Converter2 with PI

4.2 Voltage Sag Using PI Controler

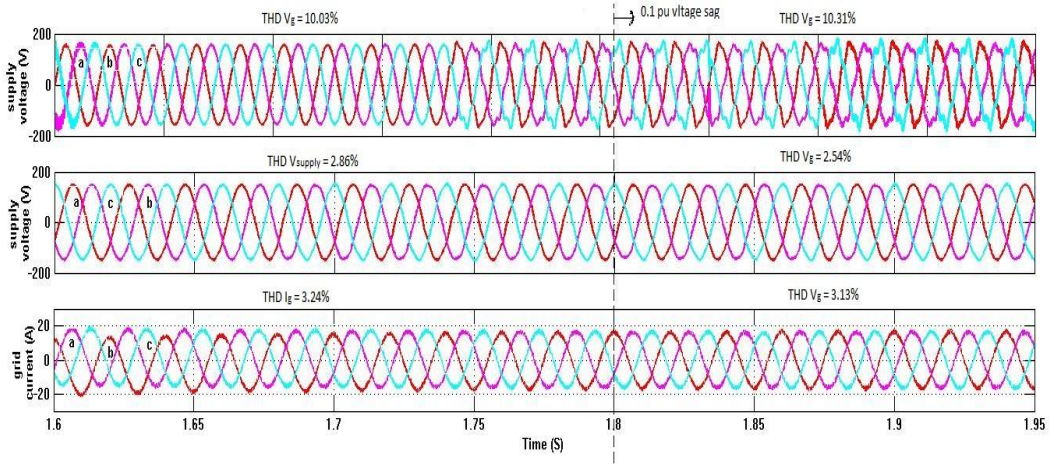


Figure 8: The performance of the dual-converter system during 10% grid voltage sags of PI controller

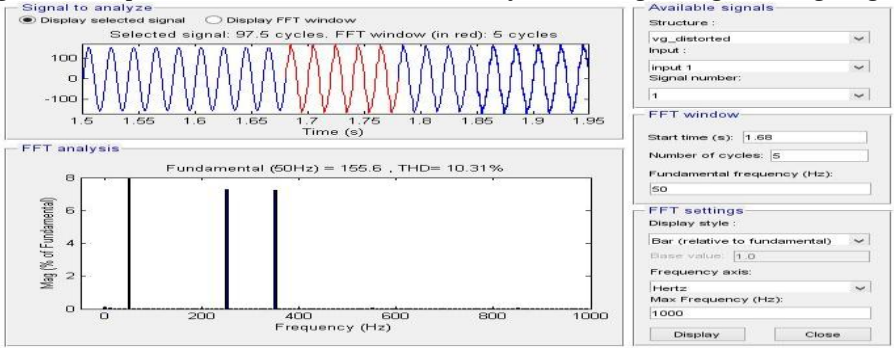


Figure 9: Grid voltage of FFT analysis and THD using PI controller

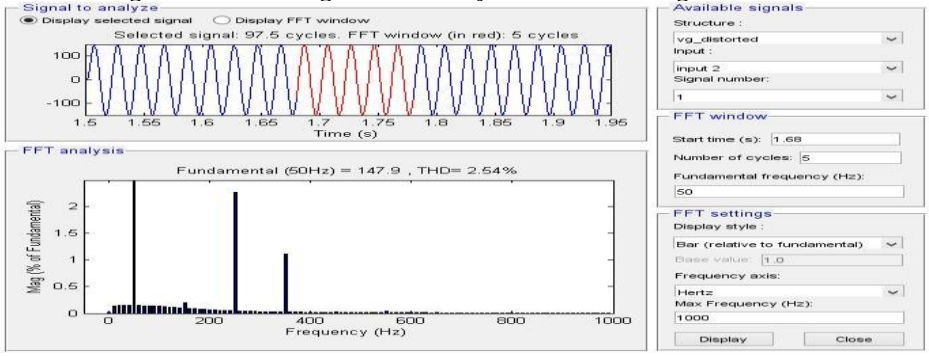


Figure 6.10: Supply voltage of FFT analysis and THD using PI controller

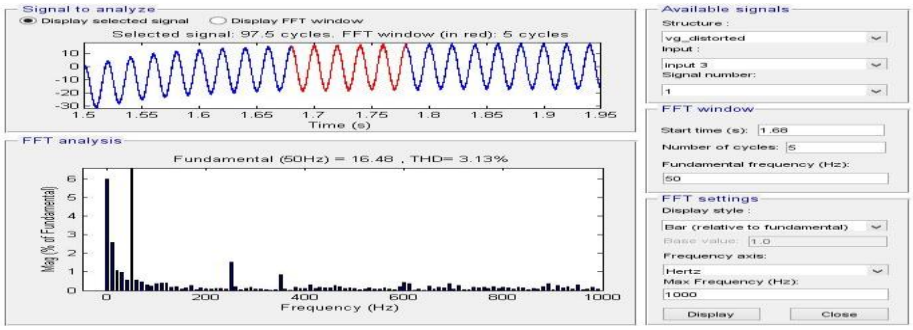


Figure 6.11: Grid current of FFT analysis and THD using PI controller

4.3 After Voltage Sag

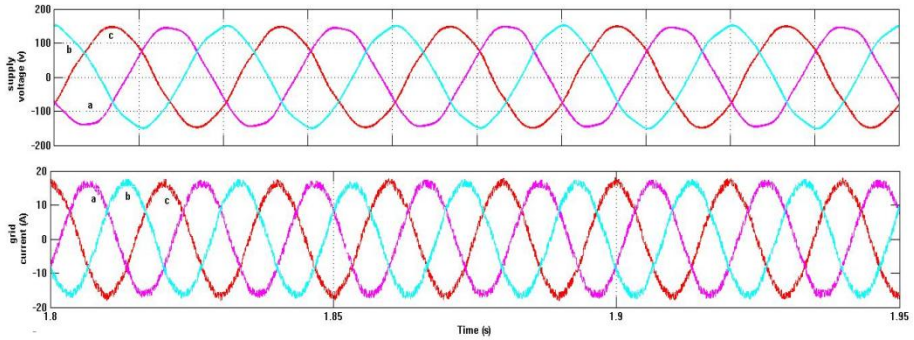


Figure 6.12: During voltage sag of grid using PI controller (From upper to lower: □□□□□□, □□)

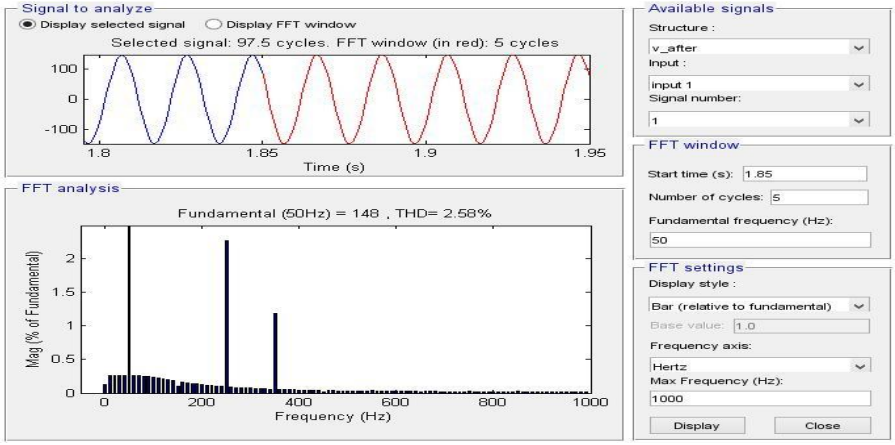


Figure 6.13: Grid voltage of FFT analysis and THD of PI controller

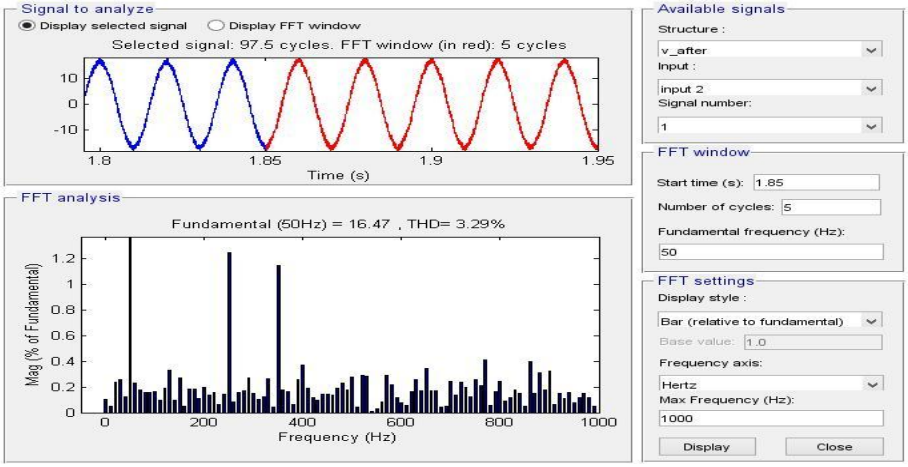


Figure 14: Grid current of FFT analysis and THD of PI controller

V. AN ADAPTIVE NEURO-FUZZY INFERENCE SYSTEM

An adaptive neuro-fuzzy derivation network or versatile system based fuzzy deduction network (ANFIS) is a sort of counterfeit neural system that depends on Takagi–Sugeno fuzzy induction network. The strategy was produced in the mid 1990s. Since it coordinates both neural systems and fuzzy rationale standards, it can possibly catch the advantages of both in a solitary structure. Its induction network compares to an arrangement of fuzzy IF–THEN decides that have learning capacity to inexact nonlinear capacities. ANFIS is thought to be an all inclusive estimator. For utilizing the ANFIS as a part of a more productive and ideal way, one can utilize the best parameters acquired by hereditary Calculation.

ANFIS: Artificial Neuro-Fuzzy Inference Systems

- ANFIS are a class of adaptive networks that are functionally equivalent to fuzzy inference systems.
- ANFIS represent Sugeno e Tsukamoto fuzzy models.
- ANFIS uses a hybrid learning algorithm.

In the field of artificial intelligence neuro-fuzzy alludes to mixes of fake neural systems and fuzzy rationale. Neuro-fuzzy hybridization brings about a half and half astute network that synergizes these two procedures by joining the human-like thinking style of fuzzy networks with the learning and connectionist structure of neural systems.

Neuro-fuzzy hybridization is genarelly named as Fuzzy Neural Network (FNN) or Neuro-Fuzzy System (NFS) in the writing. Neuro-fuzzy network (the more mainstream term is utilized from this time forward) fuses the human-like thinking style of fuzzy networks using fuzzy sets and a semantic model comprising of an arrangement of IF-THEN fuzzy standards.

The primary quality of neuro-fuzzy networks is that they are widespread approximates with the capacity to request interpretable IF-THEN principles. The quality of neuro-fuzzy networks includes two conflicting necessities in fuzzy displaying interpretability versus exactness. Practically speaking, one of the two properties wins. The neuro-fuzzy in fuzzy demonstrating research field is separated into two zones: semantic fuzzy displaying that is centered on interpretability, for the most part the Mamdani model; and exact fuzzy demonstrating that is centered around exactness, primarily the Takagi-Sugeno-Kang (TSK) model.

5.1 Harmonic Compensation Using ANFIS Controller

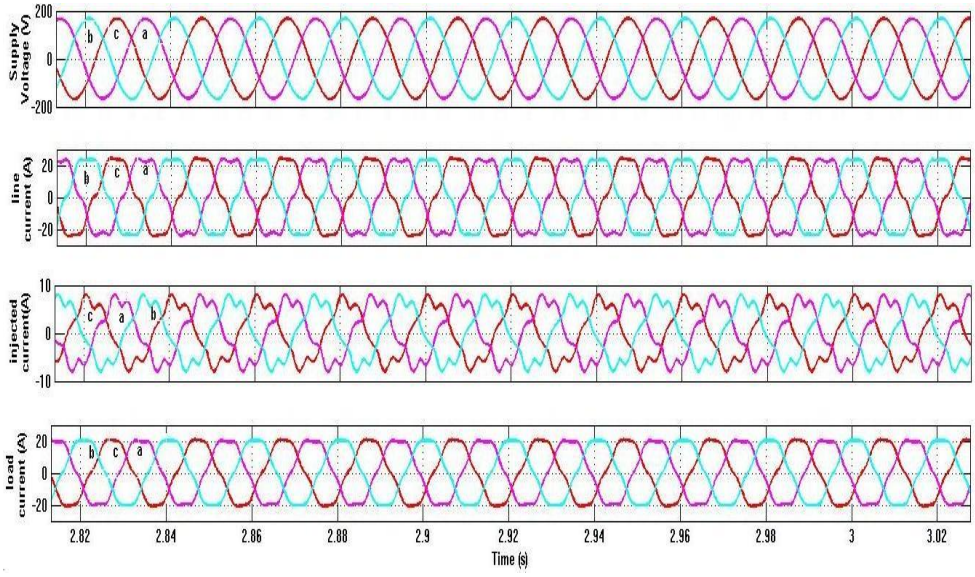


Figure 15: Performance of converter with ANFSI (From up to down: V_{supply}, I_2,c_1,I_{inj}, I_{Load})

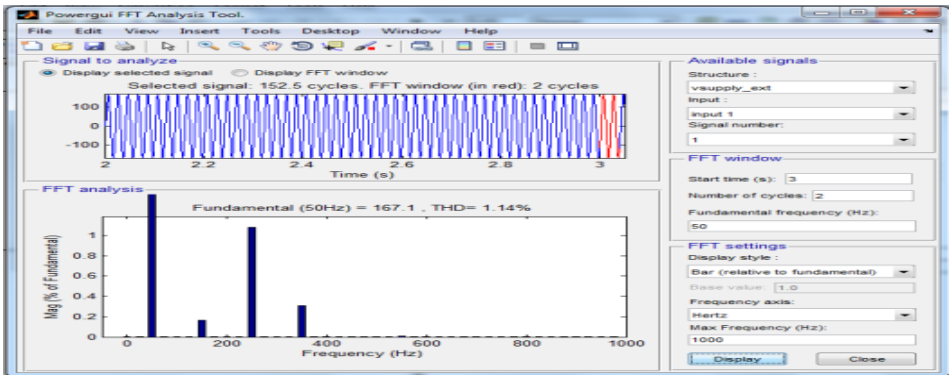


Figure 16.Grid voltage of FFT analysis and THD with ANFIS Controller

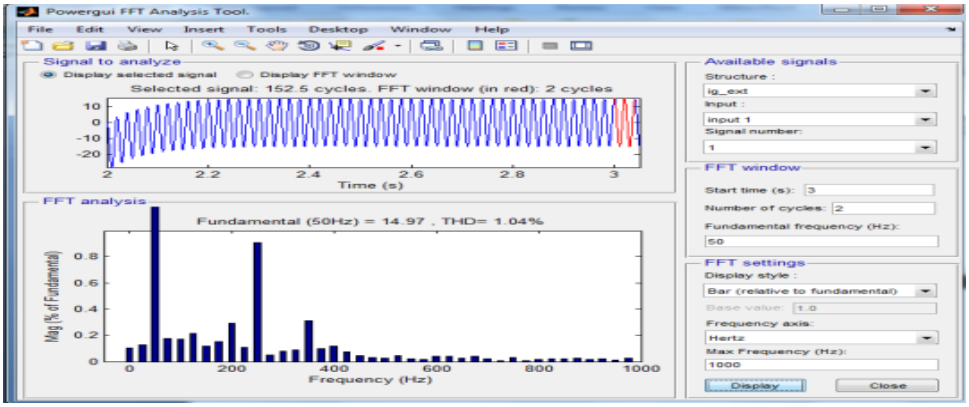
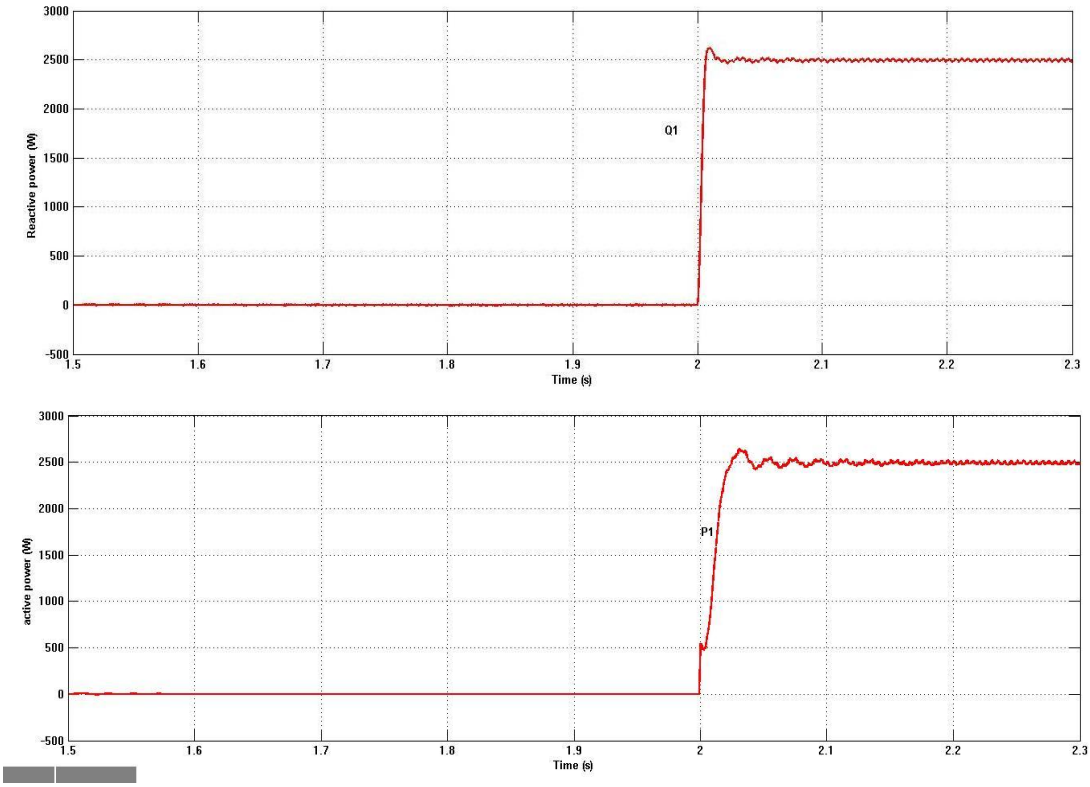


Fig 17.Grid current of FFT analysis and THD with ANFIS Controller

5.1.1. Real and reactive power of converter1 and converter2 with ANFSI controller



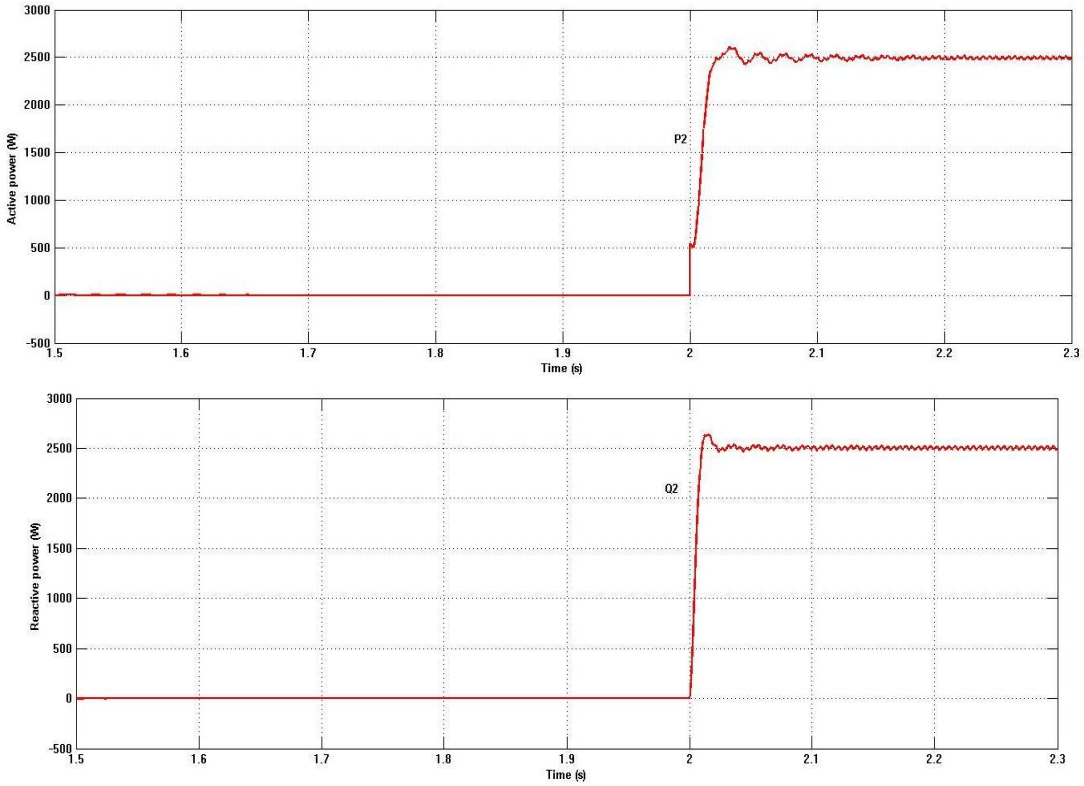


Figure 18: Real and reactive power of converter1and Converter2 with ANFIS Controller

5.2 Before voltage sag

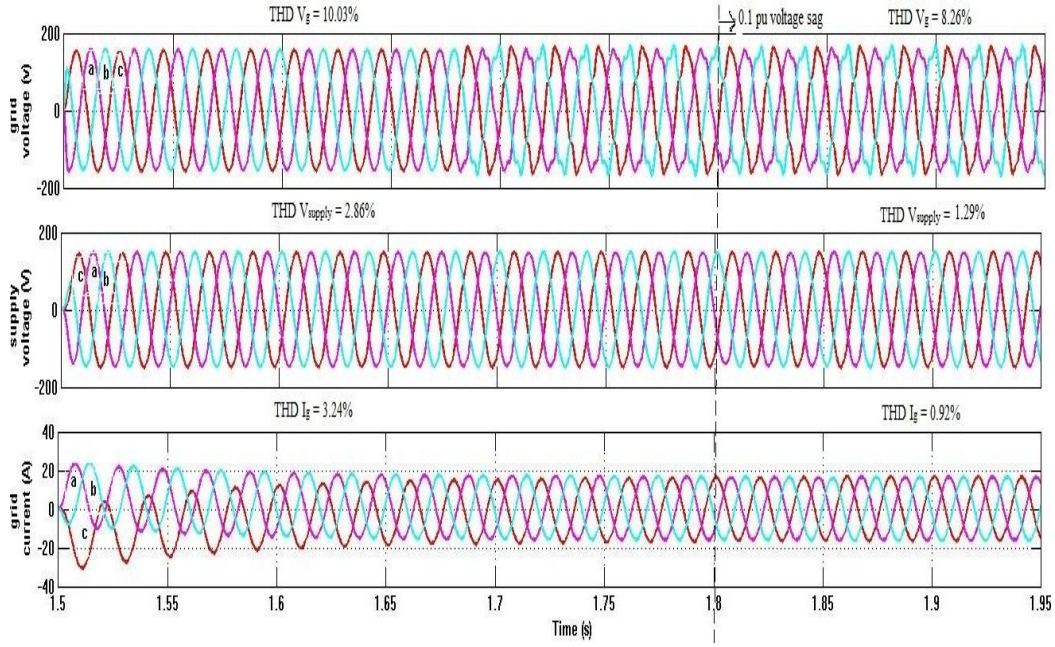


Figure 19: The performance of the dual-converter system during 10% grid voltage sags, with ANFIS Controller

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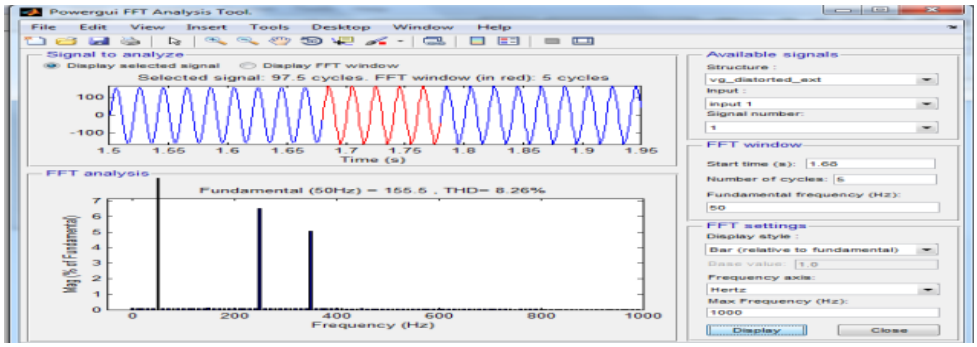

Figure 20: Grid voltage of FFT analysis and THD with ANFIS Controller

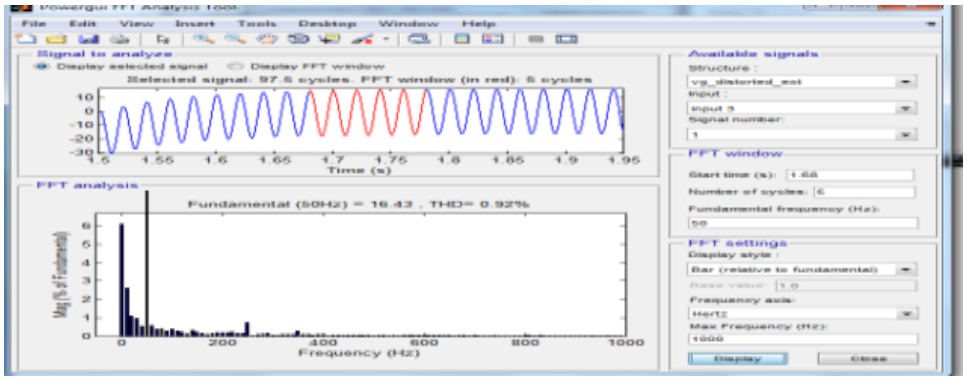

Figure 21: Supply voltage of FFT analysis and THD with ANFIS Controller

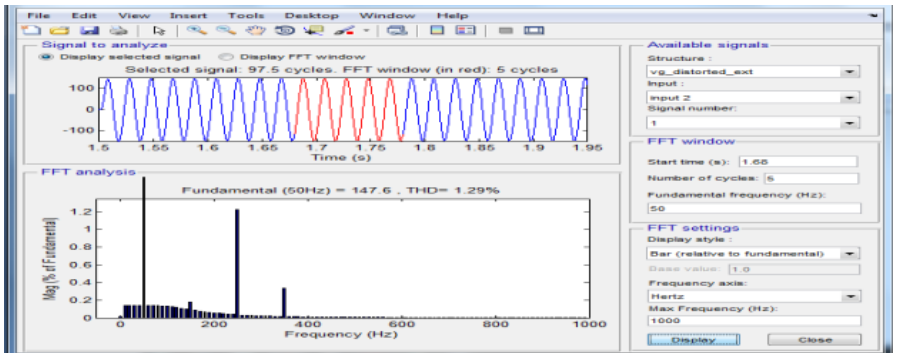

Figure 22: Grid current of FFT analysis and THD with ANFIS Controller

5.3 After voltage sag

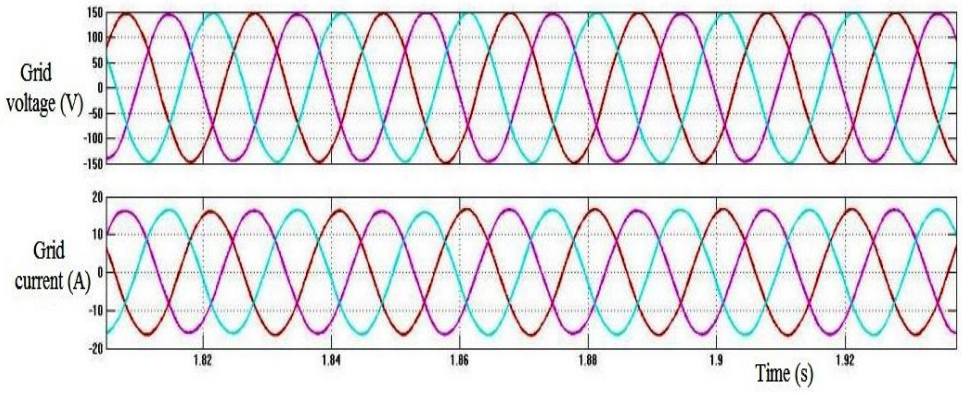

Figure 23: After voltage sags grid with ANFIS Controller

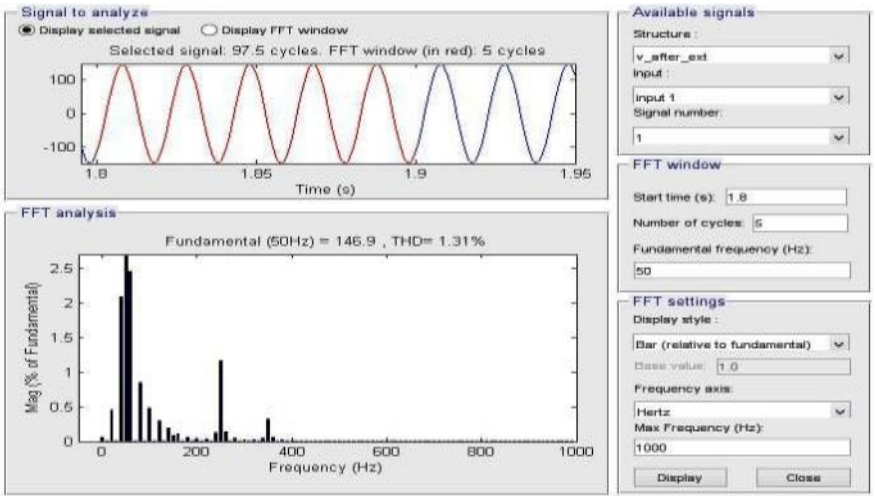

Figure 24: Grid voltage of FFT analysis and THD with ANFIS Controller

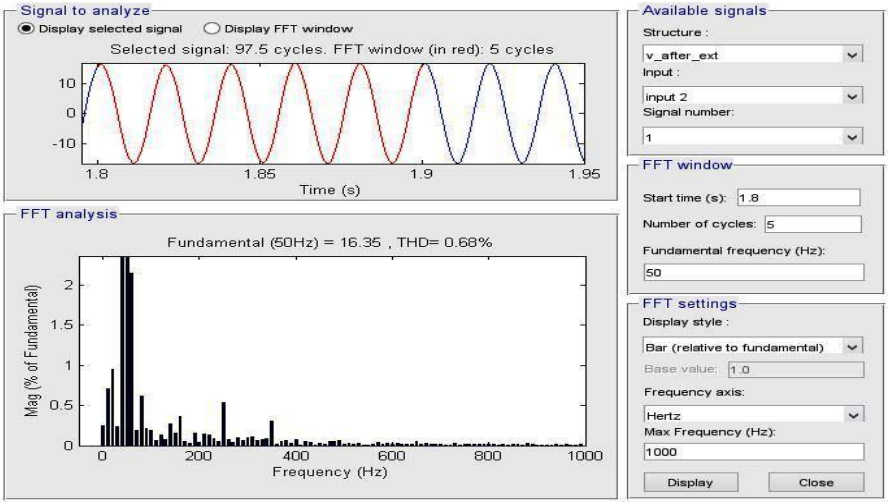

Figure 25: Grid current of FFT analysis and THD with ANFIS Controller

We are clear understanding of the principle of the proposed ANFIS controller for parallel converter coordinated control, the spectrum of grid current and supply voltage, grid current ,grid voltage, line current, and capacitive current, active and reactive power compensation In this , it can be noticed that both grid current, voltage and quality are significantly improved caring with PIcontroller comparing with ANFSI controller.

VI. Conclusion

We are design the proposed model using ANFIS controller for dual interfacing converters in Mat lab/Simulink software and tested the performance of the system and take the output waveforms of the system. In the total system we use ANFIS controller for getting proper results in controlling of the controllers. And compare results the results using PI controller and ANFIS controller. At the purpose wherever one multi-useful interfacing device is received from compensating generation near native load (nonlinear) burdens of the harmonic current. the character of provide voltage to neighborhood load will barely be increased within the meanwhile, specific once the elemental network voltage is mixed. This paper examines a completely unique composed current and voltage controller for double device system within which the near load is squarely related to the shunt condenser of the first device. With the setup, the character of provide voltage is to be improved by means that of an immediate shut circle filter condenser voltage of harmonic voltage management. The organized current and voltage management while not utilizing provide voltage /load harmonics harmonic extractions or stage bolt loops is made to acknowledge to composed management of coincidental converters.

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