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Design and Simulation of PFC Rectifier for DC Motor Drive

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Abstract — *In order to reduce the cost, many single- stage PFC converters, which integrate the PFC stage with the DC/DC stage into a single stage, have been proposed recently. The main idea is that the PFC stage and DC/DC stage share a common switch so that one main switch and its controller can be saved. This paper presents the design and implementation of a three-phase high power factor mains interface concept appropriate for many power electronic applications such as electric vehicle battery charging, supplies for dc power distribution systems in telecommunication, variable-speed ac drives, dc motor drives ,future more electric aircraft and high power lighting systems. The circuit topology comprises a power factor correction rectifier which is of buck-type circuit built by the combination of an active third-harmonic injection rectifier and a series-connected dc–dc buck-type chopper. The characteristics of this rectifier topology, including the, modulation strategy, principles of operation, suitable control structure, and dimension equations, are described in this paper. The practicality of the presented converter for buck-type rectifier applications is verified by means of a constructed through Matlab/Simulink. the implemented system has been compared to another remarkable buck-type Swiss Rectifier. Finally DC-Motor is connected to the system and observes the motor is settling down to Study State at 0.5 Seconds.*

Keywords- *Active Third-Harmonic Current Injection, Swiss Rectifier, PWM Control, Buck type Power Factor Correction Rectifier Systems, DC Motor Drive, Matlab/Simulink*

1 INTRODUCTION

The pattern of an electronic system in the industry is often based on the experience of the designer or even a trial-and error method. Evidently, this does not lead to an optimum design, whereas analytical calculations of the component stresses [1] provide a clear and general guideline for the component selection and for the converter design. As an application case a front-end converter for telecommunications power supply modules shall be dimension ed that should have the following features: constant output voltage of U0= 400V for operation at the 400 V mains(UN,l-l,rms=400 V 10, output power of P0= 5 kW, sinusoidal mains currents, unity power factor, high power density and simplicity of the power circuit structure.

Basically, two structures are possible for performing this task: i) a boost-type input rectifier (e.g., Vienna rectifier, [2]), that typically features two 400-V output voltages with a three-level isolated dc–dc converter or two isolated dc–dc output stages and ii) a buck- type input rectifier (conventionally six-switch topologies as proposed in [3]–[6]) with only one two-level isolated dc–dc converter output stage. In particular, the number of utilized active and passive components is much lower. Furthermore, there is no middle-point that has to be stabilized, as this is the case for the boost- type structures especially for the case of asymmetrical load of the two parallel output stages.

Further system advantages are the potential of a direct start-up and the over current protection in case of an output short circuit. Therefore, this topology is of high interest for these applications and could also be attractive for future electric aircraft applications or as power supplies for process technology. The three- switch buck rectifier topology was first proposed in [7]. In [8] and [9], aspects of the system modulation and control have been treated. The application of the topology used as an active filter is discussed in [10]. In [11] and [12], the function of the 12-pulse rectifier is emulated by interleaving of two three-switch Buck rectifier stages which lead to a reduction of the input filtering requirements. The addition of a dc–dc output boost-stage has been proposed in [13] in order to maintain 400-V output voltage for a wide input voltage range and for the case of unbalanced mains as, e.g., the loss of one phase. scheme A modulation aiming for minimum switching losses and minimum input current distortion has been proposed, a parallel operation of two dc-side connected rectifiers has been discussed, and a common mode (CM) and differential mode (DM) input filter has been designed. However, in none of these publications a complete system design has been performed discussing current and voltage stresses and selection criteria for the passive and active components of the rectifier. Therefore, in this paper the design of the three-phase three switch buck-type rectifier system is discussed in detail. The output voltage obtained from the buck-type PFC rectifier is fed to a DC Motor. Finally the DC motor fed from the proposed PFC converter is shown in the figure 1.

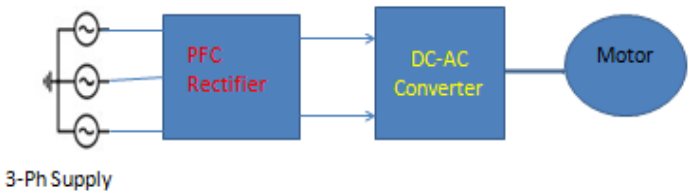


Fig 1. Overall proposed system

2. HYBRID ACTIVE THIRD-HARMONIC CURRENT INJECTION BUCK-TYPE PFC RECTIFIER

Suitable 400-V dc power distribution architecture for telecom and/or data center applications is shown in Fig. 2.1.There, a unidirectional three-phase power factor correction (PFC) rectifier is utilized as mains interface circuit in order to power the telecom equipment at the dc side with controlled voltage, while at the ac side, high-power-factor operation is maintained. If isolation of the dc bus from the PFC rectifier is required for safety reasons, this can be facilitated by an isolated dc–dc converter connected in series, which can additionally be used for voltage regulation.

In the European market with the typical three-phase 400 V (line-to-line rms voltage) ac mains, boost-type PFC rectifiers produce an output voltage (typically 700–800 V) that is too high to directly feed the telecom 400-V dc bus and thus call for a step-down dc–dc converter at their output even if no isolation is required. On the other hand, buck-type PFCs, see Fig. 2.2, are particularly interesting because they provide a wide output voltage control range, while maintaining PFC capability at the input, enable direct start-up, and allow for current limitation in case of an output short circuit .

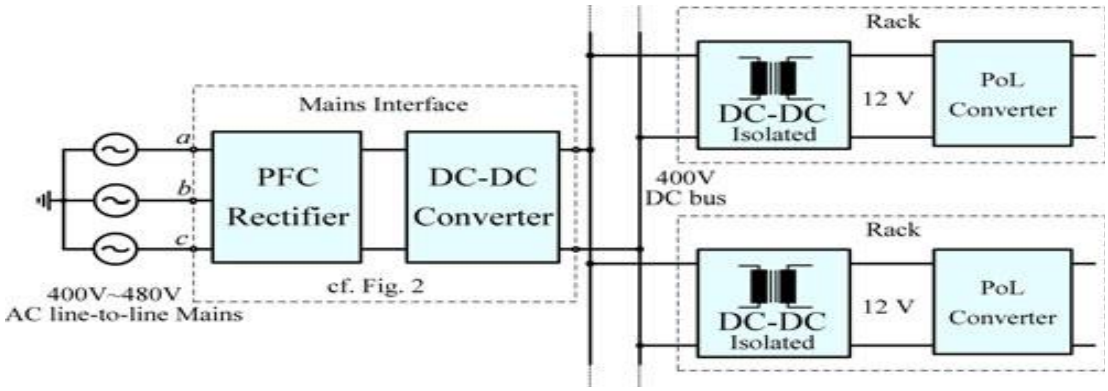
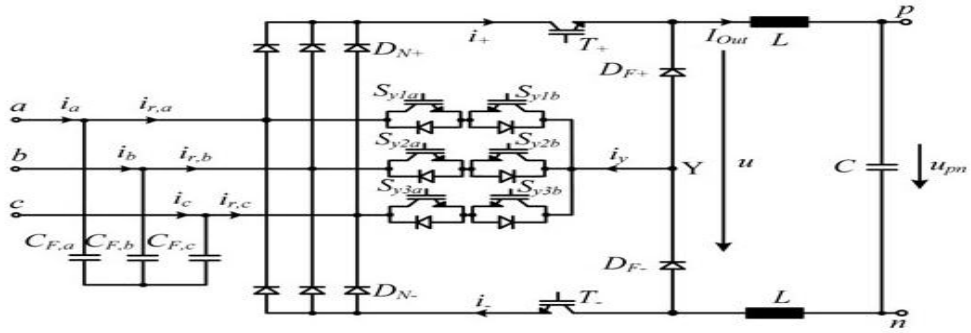
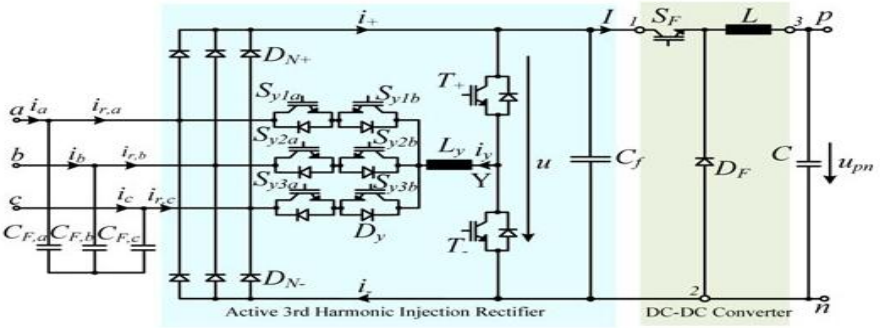


Fig.2.1. Possible 400-V dc distribution architecture for telecom and/or data center applications



(a)



(b)

Fig.2.2. Basic structure of three-phase buck-type PFC rectifiers employing an active third-harmonic current injection circuit: (a) SR and (b) H3R.

Recent discussions about three-phase buck-type PFC systems have identified topologies based on third-harmonic current injection circuit appropriate for mains interface of dc distribution architectures. The circuit schematic depicted in Fig. 2.2(a), also referred as the SWISS rectifier (SR), is a remarkable example, as for some operation conditions it can achieve a superior efficiency performance than conventional buck-type structures, i.e., at high switching frequencies. In fact, the main advantage of the SR is not only seen in the higher achievable efficiency but also that the system can be controlled similarly to a dc–dc converter. Accordingly, basic knowledge of the function of a buck-type dc–dc converter and a three-phase passive diode rectifier is sufficient to implement a three-phase PFC rectifier with sinusoidal input currents and a controlled output voltage. For more details about this converter concept, the interested reader is referred to and, where this system was comprehensively studied.

Another interesting three-phase buck-type PFC rectifier is depicted in Fig. 2.2(b). This circuit, referred to here as hybrid active third-harmonic injection buck-type rectifier (H3R) combines an active current injection electrolytic capacitor-less converter (front-end) with a series-connected dc–dc buck-type converter (back-end). The main advantage of this concept over conventional buck-type PFCs is that only a single power transistor S_F and two line-commuted diodes *DN* +/− exist in the main current path, which leads to low conduction losses. Additionally, the components in the injection circuit require relatively low current rating devices, i.e., the maximum value of the flowing current is rated half the amplitude of the sinusoidal input current.

The front-end circuit concept of the H3R system was first introduced in late 90s by Jantsch and Verhoeve, where three phase grid-connected photovoltaic inverters without electrolytic capacitor for improved life time were proposed. In , this topology was implemented as an auxiliary circuit to attenuate the input current harmonics of a conventional diode rectifier-fed inverter having a very small dc-link capacitor. Thus, that system did not provide the full functionality of an output voltage regulated PFC rectifier and critical operating conditions could

Damage the system reliability, i.e., problems could occur due to the low energy storage during short-term input voltage interruption or during load variations which would be passed on directly to the mains. Only recently the full potential of the H3R circuit has been investigated (cf.,), but no hardware implementation with experimental results validating the proposed circuit analyses has been shown. Additionally, a general guideline for the H3R system design, dealing with some implementation issues, such as a distinct modulation of the current injection circuit providing the required uninterrupted current flow, is still missing in the literature.

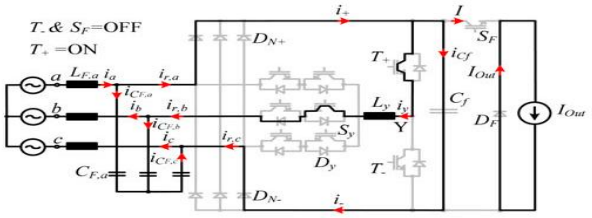
The basic configuration of a three-phase high-power-factor rectifier solution is shown in Fig. 2.2(b). The front-end converter consists of a three-phase electrolytic capacitor-less line commuted rectifier combined with an active current injection circuit, which is formed only by a single fast-commuted half bridge leg, a phase inductor, and three low-frequency bidirectional switches. Accordingly, this circuit shows a relatively low implementation effort, however, at the expense of a missing output voltage control. The output voltage *u* is now determined directly by the diode bridge rectifier and hence exhibits a six-pulse shape. Therefore, a series-connected dc–dc converter (back-end) is necessary to provide the required dc-bus voltage level regulation and/or dynamic current limitation.

The high-power-factor operation is assured by the back-end converter, which needs to be controlled to demand (fundamental) constant power *P* and no smoothing capacitor of higher capacitance C_f is connected to the dc link. In this case, currents *I* varying in opposite phase to the six-pulse rectifier voltage will be impressed at the output of the front-end converter. This leads to a sinusoidal shape of all mains phase currents after overlaying with the currents of the injection current circuit (i_y, i_+, and i_-). Although the capacitor C_f can degrade the sinusoidal controllability of the mains currents, a minimum capacitance value is required for proper converter operation. For some conduction states, this component provides the necessary current path for the imposed injection current *iy* . This characteristic can be seen in the conduction state depicted in Fig. 2.2(b) valid for the mains interval [0, 30◦] ($u_a > u_b > u_c$). There, the value of C_f should also be selected to limit the rise of the voltage at the output of the diode bridge.

As illustrated in Fig. 2.3, the implementation of this system with a simple dc–dc buck converter is very attractive as few active switches in the main current path exist (only the single power transistor *SF*), leading to low conduction losses, i.e., in particular at high output voltages with a relatively short freewheeling interval. In addition, the negative output voltage terminal is always connected to the mains via a diode of the rectifier. Therefore, no output common-mode (CM) voltage with switching frequency is generated. The implementation effort of the CM EMI filter can thus be reduced as only the parasitic capacitors of the power semiconductors lead to high-frequency CM noise currents.

Note that the buck dc–dc converter unit and the four-quadrant switches can be replaced by other typical power electronic circuits. For example, the line-commutated injection switches could be implemented with an anti-parallel connection of reverse blocking insulated bipolar transistors (IGBTs) with a low forward voltage drop. Additionally, if converter isolation and/or further voltage level regulation is necessary, another dc–dc converter with galvanic isolation could be used to replace the simple buck-type circuit. A bidirectional implementation can be accomplished by adding discrete IGBTs in parallel to the line diodes *DN* +/− and fast diode *DF* , while an auxiliary fast diode would be required

in parallel to *SF* . Finally, in applications such as high-power electric vehicle battery charging and variable-speed ac drives, interleaved dc–dc converters, resonant topologies, or multiphase inverters could be advantageously utilized as replacement for the simple dc–dc buck converter.



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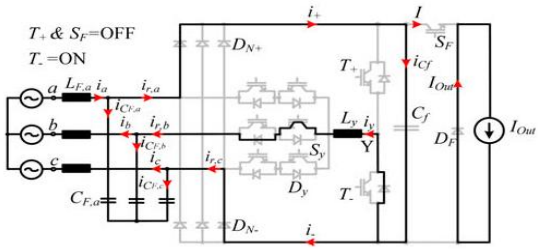

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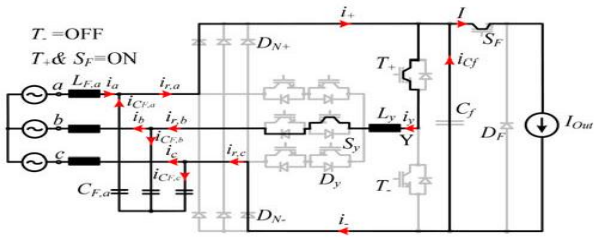
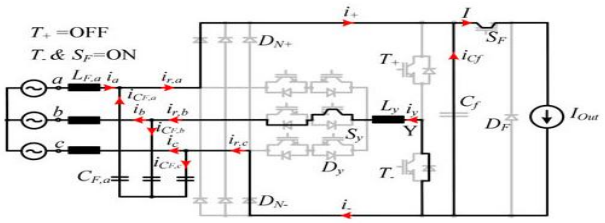
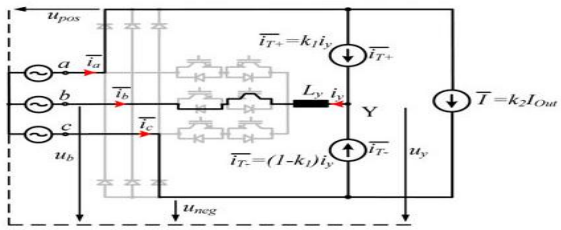


(c)



(d)



(e)

Fig.2.3 (a) - (d) Conduction states and (e) equivalent circuit of the rectifier for $u_a > u_b > u_c$.

For proof of the sinusoidal controllability of the mains currents, the four conduction states and equivalent circuit of the H3R circuit valid for the mains interval [0, 30◦] ($u_a > u_b > u_c$) are considered for analysis (cf., Fig. 2.3). Ideally, the rectifier system operates as a symmetric three-phase load of phase conductance *G* to the mains; therefore, the value of the current to be injected into phase *b* may be written as

$$i_{y=-ib=-Gu_b}$$

The mains frequency voltage drop across the inductor of the current injection circuit can in a first approximation be neglected for the formation of i_y

$$u_L = 0$$

Accordingly, the voltage formed at the output of the bridge leg will be given by

$$u_y = u_b$$

If the voltage at the terminal *Y* is formed according to the relative on-time of the transistor *T*+ as *k*1 and *T*− as $(1-k_1)$, it will result in

$$u_y = k_1 u_a + (1-k_1)u_c = k_1 u_{ac} + u_c$$

For the duty cycle k_1 given by $u_{pos} = max(u_a, u_b, u_c)$

$$u_{neg} = min((u_a, u_b, u_c)$$

$$k_1 = \frac{-(u_{pos} + 2u_{neg})}{u_{pos} - u_{neg}} = \frac{u_{bc}}{u_{ac}}$$

the current across *T*+ can be calculated as

$$i_T = k_1 i_y = -k_1 i_b = -k_1 G u_b = -G u_b \frac{u_{bc}}{u_{ac}}$$

Considering the fundamental input currents that have to be generated at the input

$$i_a = G u_a, \quad i_b = G u_b, \quad and \; i_c = G u_c$$

And the current consumption of the constant power load as

$$\bar{I} = K_2 I_{out} \; with \; k_2 = \frac{u_{pn}}{u_{pos} - u_{neg}}$$

Gives

$$\bar{I} = \frac{P}{u_{ac}} = \frac{\bar{i_a} u_{ac} + \bar{i_b} u_{bc}}{u_{ac}} = G \frac{u_a u_{ac} + u_b u_{bc}}{u_{ac}}$$

The resultant low-frequency current drawn from phase *a* is therefore proportional to the mains voltage.

$$\bar{i_a} = I + \bar{i_{T+}} = G u_a$$

Additionally, the low-frequency current for phase *c* can be determined,

$$\bar{i}_a + \bar{i}_b + \bar{i}_c = 0, \text{ and } ua + ub + uc = 0$$

$$\bar{i_c} = G u_c$$

Therefore, sinusoidal shape of all phase currents for the mains interval [0, 30◦] (*ua* > *ub* > *uc*) has been proven. Finally, high-power-factor operation and controlled output voltage *upn* for all mains sector can be achieved with the relative on-times k_1, (1−k_1) and k_2 of the power transistors *T*+/*T*− and S_F given in Table I (cf., Fig. 3.2). These variables are reliant on the instantaneous values of the mains voltages *ua, b, c* converted to line-to-line quantities and the output voltage reference *u* pn.*

Sector	k_1	k_2	S_{y1a}	S_{y1b}	S_{y2a}	S_{y2b}	S_{y3a}	S_{y3b}
0°-30°	u_{bc}/u_{ac}	u^*_{pn}/u_{ac}	0	0	1	1	0	0
30°-60°	u_{bc}/u_{ac}	u^*_{pn}/u_{ac}	0	0	1	1	0	0
60°-90°	u_{ac}/u_{bc}	u^*_{pn}/u_{bc}	1	1	0	0	0	0
90°-120°	u_{ac}/u_{bc}	u^*_{pn}/u_{bc}	1	1	0	0	0	0
120°-150°	u_{ca}/u_{ba}	u^*_{pn}/u_{ba}	0	0	0	0	1	1
150°-180°	u_{ca}/u_{ba}	u^*_{pn}/u_{ba}	0	0	0	0	1	1
180°-210°	u_{ba}/u_{ca}	u^*_{pn}/u_{ca}	0	0	1	1	0	0
210°-240°	u_{ba}/u_{ca}	u^*_{pn}/u_{ca}	0	0	1	1	0	0
240°-270°	u_{ab}/u_{cb}	u^*_{pn}/u_{cb}	1	1	0	0	0	0
270°-300°	u_{ab}/u_{cb}	u^*_{pn}/u_{cb}	1	1	0	0	0	0
300°-330°	u_{cb}/u_{ab}	u^*_{pn}/u_{ab}	0	0	0	0	1	1
330°-360°	u_{cb}/u_{ab}	u^*_{pn}/u_{ab}	0	0	0	0	1	1

TABLE 1 MODULATIONS OF THE CURRENT INJECTION CIRCUIT AND DUTY CYCLE CALCULATION FOR PFC OPERATION (CF., FIG. 3.2)

3. PWM CONTROL SCHEME

A possible implementation of a control scheme for the H3R circuit is shown in Fig. 3.2, and consists of two control loops: one for the dc–dc converter, corresponding to the constant-power Load, and a second for the injection circuit, controlling the voltage applied across *Ly*, thus regulating the current injected back into the mains phases. The modulation of the current injection circuit is performed at low frequency (twice the input frequency, with two 60◦ conduction periods within a period), following the rectifier input voltages *ua, b, c* in such a way that the active current injection always occurs into only one mains phase as presented in Table I (cf., Fig. 3.2). Due to the requirement of uninterrupted current flow through the inductor *Ly*, while still allowing a dead time preventing short circuits between the

individual phases, the modulation depicted in Fig. 3.2 is implemented. Auxiliary free-wheeling diodes *D*FW1 and *D*FW2 can also be placed as alternative or supplementary protection to the current injection switches. Ideally, *D*FW1 and *D*FW2 never conduct.

3.1 MAIN DESIGN EXPRESSIONS

In this section, the main expressions for designing the H3R rectifier, which models the stresses of the active and passive components, are given. These are functions of the modulation index *M*, the output voltage u_{pn} , amplitude of the sinusoidal input current $\hat{I}_N$, and output current I_{Out} . There, it is assumed that the rectifiers have a purely sinusoidal phase current shape; ohmic mains behavior, no low-frequency voltage drop across the inductors; and a switching frequency f_P , which is much higher than the mains frequency f_N ($f_P >> f_N$).

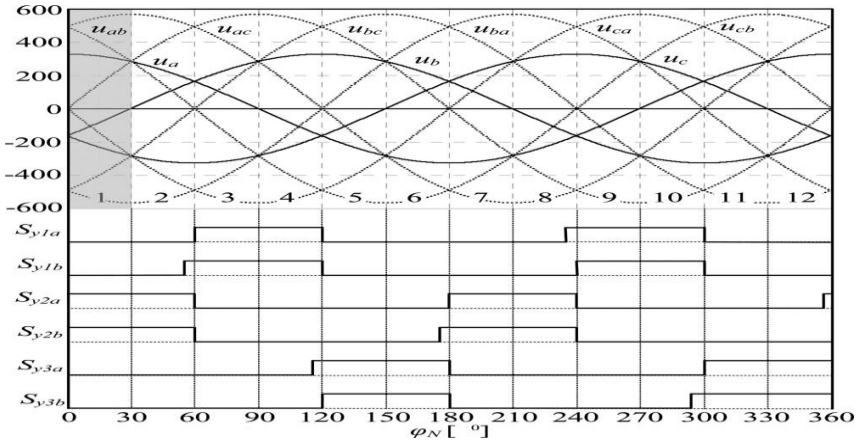


Fig.3.1. Mains sectors 1–12 defined by the different relations of the instantaneous values of the mains phase voltages $u_{a,b,c}$ and respective gate signals of the third-harmonic injection circuit switches providing the injection current logic and the required uninterrupted current path for *Ly*.

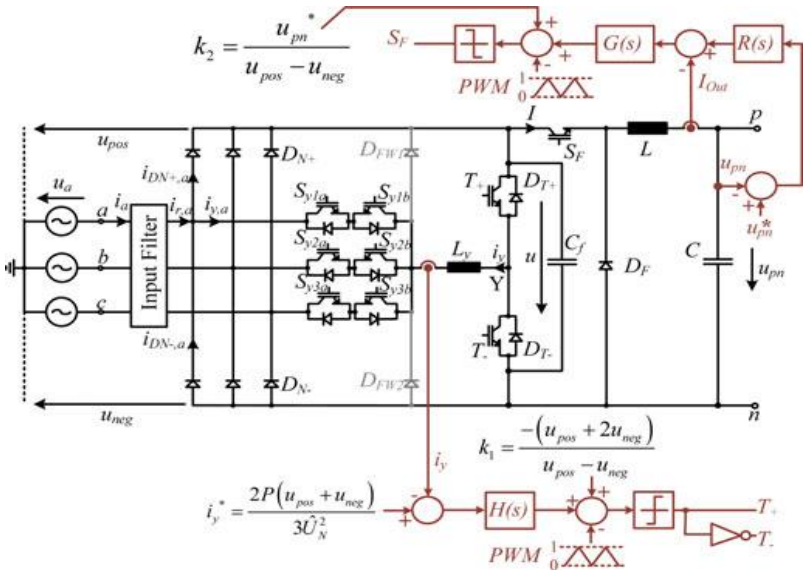


Fig. 3.2 Control structure for the H3R rectifier.The modulation/on-time of the current injection circuit is given in Table I. $\hat{U}_N$ and u_{pn}^* are the amplitude of the input phase voltage and output voltage reference, respectively.

3.2. Rectifier Analytical Model Accuracy

In order to verify the accuracy of the derived equations modeling the voltage and current stresses of the proposed rectifier, an appropriate switching frequency and the values of the passive components according to Table II have been selected. A switching frequency of f_P = 36 kHz is designated as it constitutes a good compromise between high efficiency, high power density, and high control bandwidth. Advantageously, the fourth switching frequency harmonic is found near, but below the beginning of the considered electromagnetic compatibility measurement range (150 kHz). With f_P = 36 kHz, the values for the *Ly* = 2 mH and output filter *L* = 610 μH, *C* = 470 μF, and C_f = 4 μF

Table II Rectifier Specifications

Input phase voltage $u_{a,b,c}$	230 V *rms* ±10%
Mains frequency f_N	50 Hz
Switching frequency f_P	36 *k*Hz
Rated output power P	5 *k*W
Output capacitor C	470 μF
Input capacitor $C_{F,i}$	4.4 μF
Input capacitor $C_{F,i}$	4 μF
DC inductor L	610 μH
Current injection inductor L_y	2 *m*H

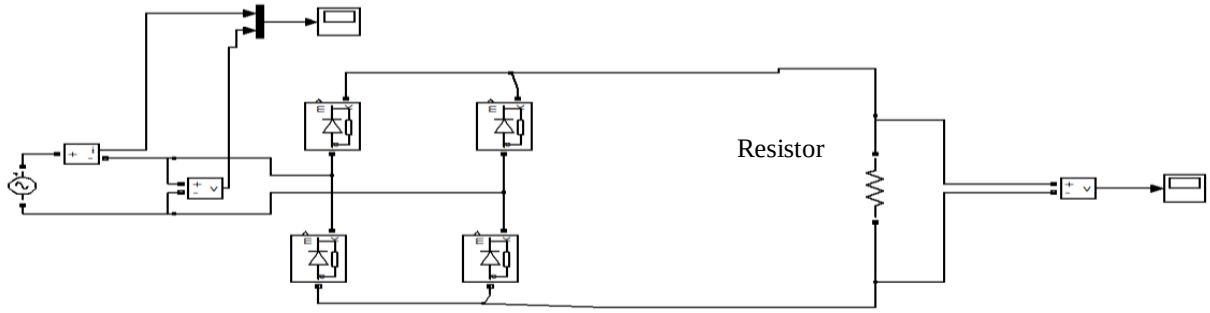
TABLE III
Comparison of active and passive component Stresses determined By analytical calculations and digital simulations

	Analytical Calculations	**Simulation**	**Deviation [%]**
$I_{Sy,avg}$ /$I_{Dy,avg}$	0.44	0.44	+0.00
$I_{Sy,rms}$ /$I_{Dy,rms}$	1.23	1.28	-3.90
$I_{DN,avg}$	2.83	2.82	+0.35
$I_{DN,rms}$	4.98	5.07	-1.77
$I_{T,avg}$	0.24	0.25	-4.0
$I_{T,rms}$	0.8	0.84	-4.7
$I_{DT,avg}$	1.05	1.07	-1.87
$I_{DT,rms}$	1.98	2.03	-2.46
$I_{SF,avg}$	9.32	9.27	+0.54
$I_{SF,rms}$	10.79	10.83	+0.37
$I_{DF,avg}$	3.18	3.20	-0.62
$I_{DF,rms}$	6.31	6.32	-0.16
$\Delta i_{L,pp,max}$	5.27	5.28	-0.19
$\Delta i_{Ly,pp,max}$	1.99	1.93	+3.1

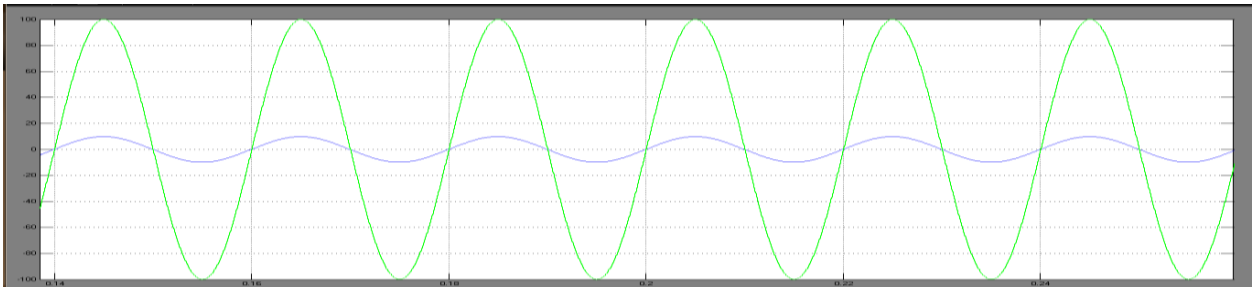
are selected. The component values of the input filter stage are $L_{F,i}$ = 220 μH and $C_{F,i}$ = 4.4 μF.
In Table III, the values of the average and rms component stresses calculated with the respective equations for Table II specified converter are compared to the results obtained with a digital simulation and show a good accuracy.

4. MATLAB/SIMULATION RESULTS

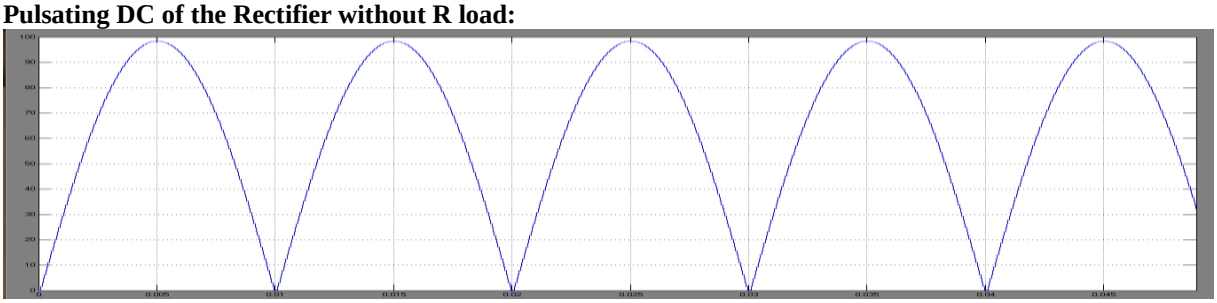
4.1. Mat Lab/Simulink Model Of Rectifier With R-Load:



Simulated wave form of Power factor of the Source with R-LOAD:

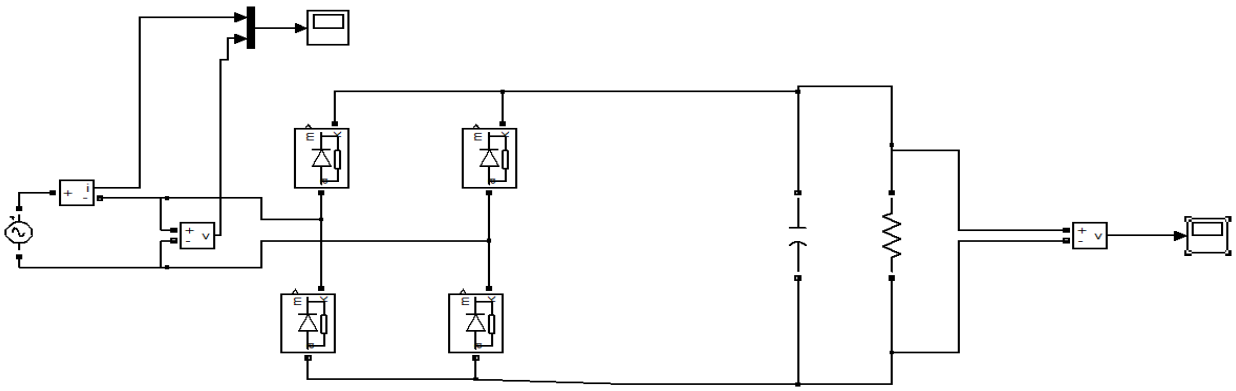


Pulsating DC of the Rectifier without R load:

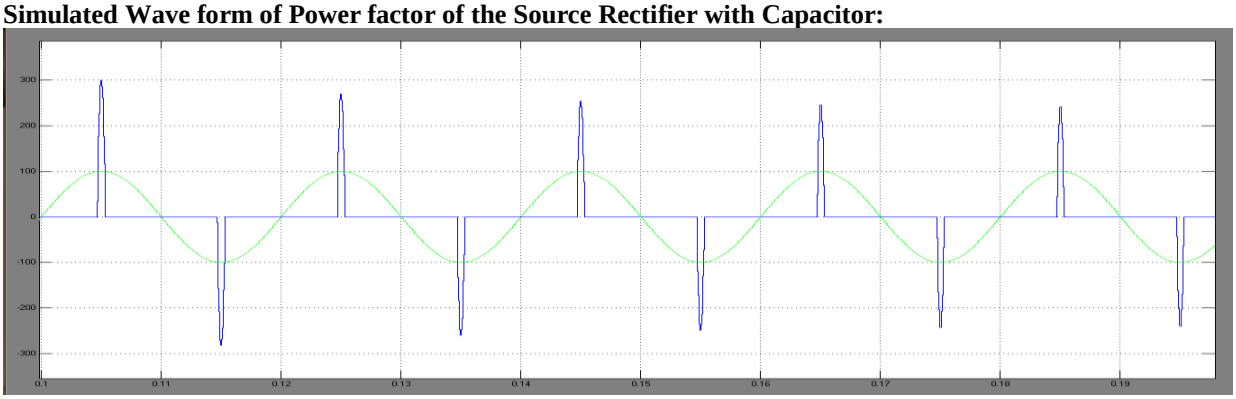


Description: As seen from above simulated wave forms with only resistor load the output voltage is pulsating dc not the pure dc wave form where as the input side power factor is unity i.e voltage is in phase with the current.

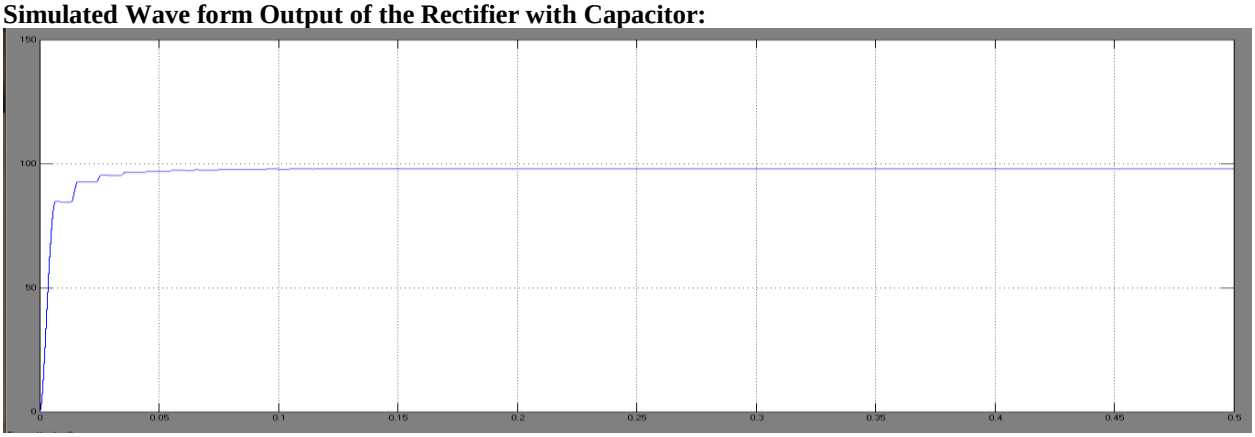
4.2 Mat Lab/Simulink Model of The Rectifier With Capacitor:



Simulated Wave form of Power factor of the Source Rectifier with Capacitor:

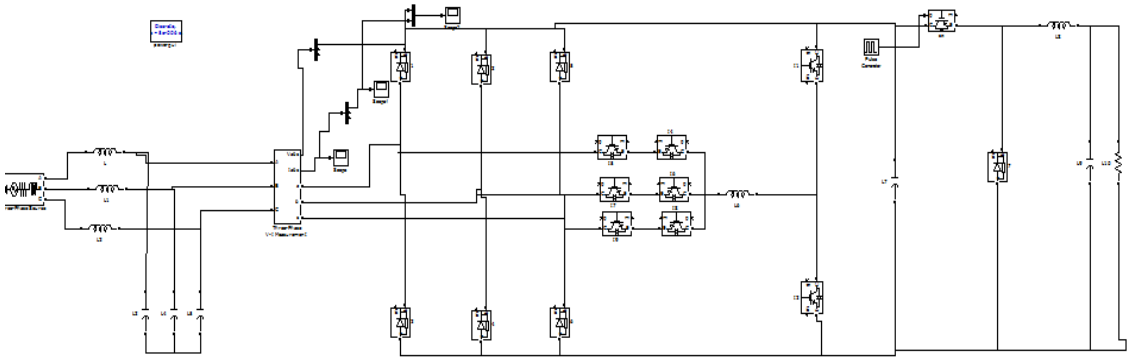


Simulated Wave form Output of the Rectifier with Capacitor:

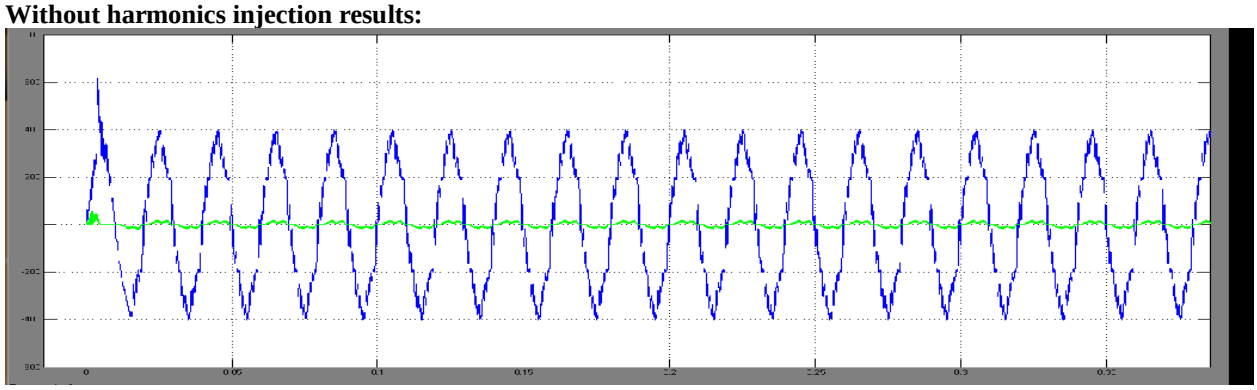


Description: As seen from the above simulated by using the capacitor of high value in the rectifier the output voltage is almost constant that is dc voltage we get but due the capacitor the input side power factor is not unity

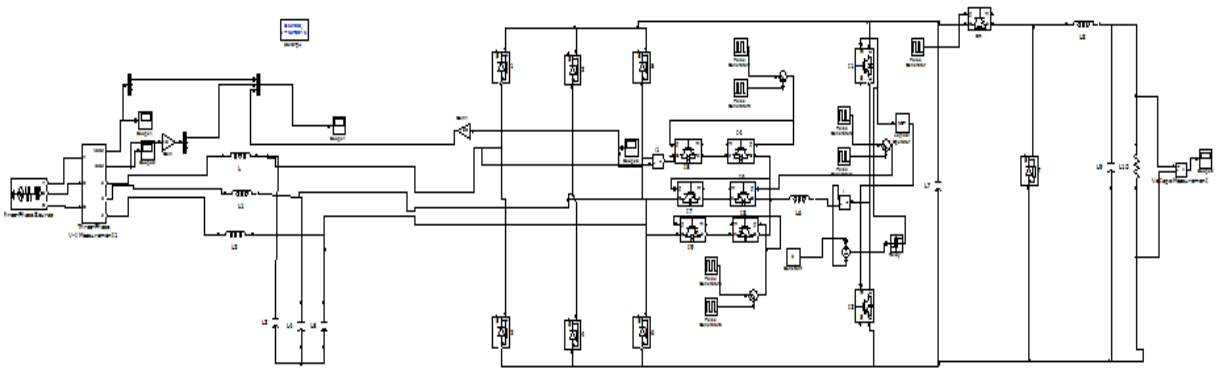
4.3 MATLAB/SIMULINK MODEL WITHOUT CONTROL SIMULINK DIAGRAM:



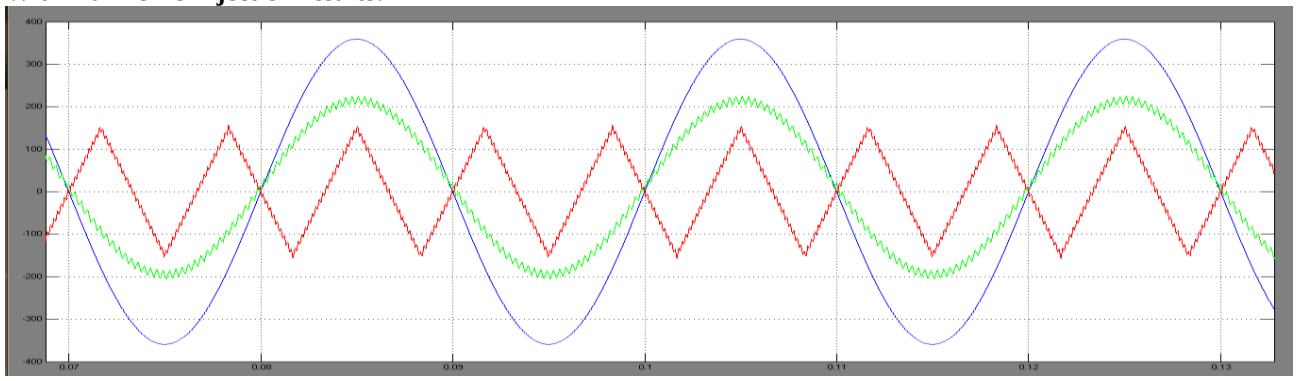
Without harmonics injection results:



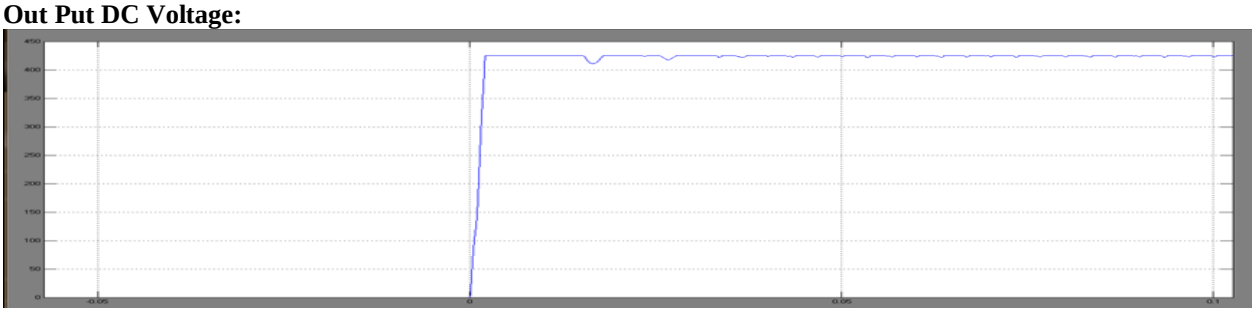
4.4 MAT LAB/SIMULINK MODEL FOR WITH CONTROLLED ACTIVE THIRD HARMONIC INJECTION BUCK TYPE PFC RECTIFIER:



With Harmonic Injection results:

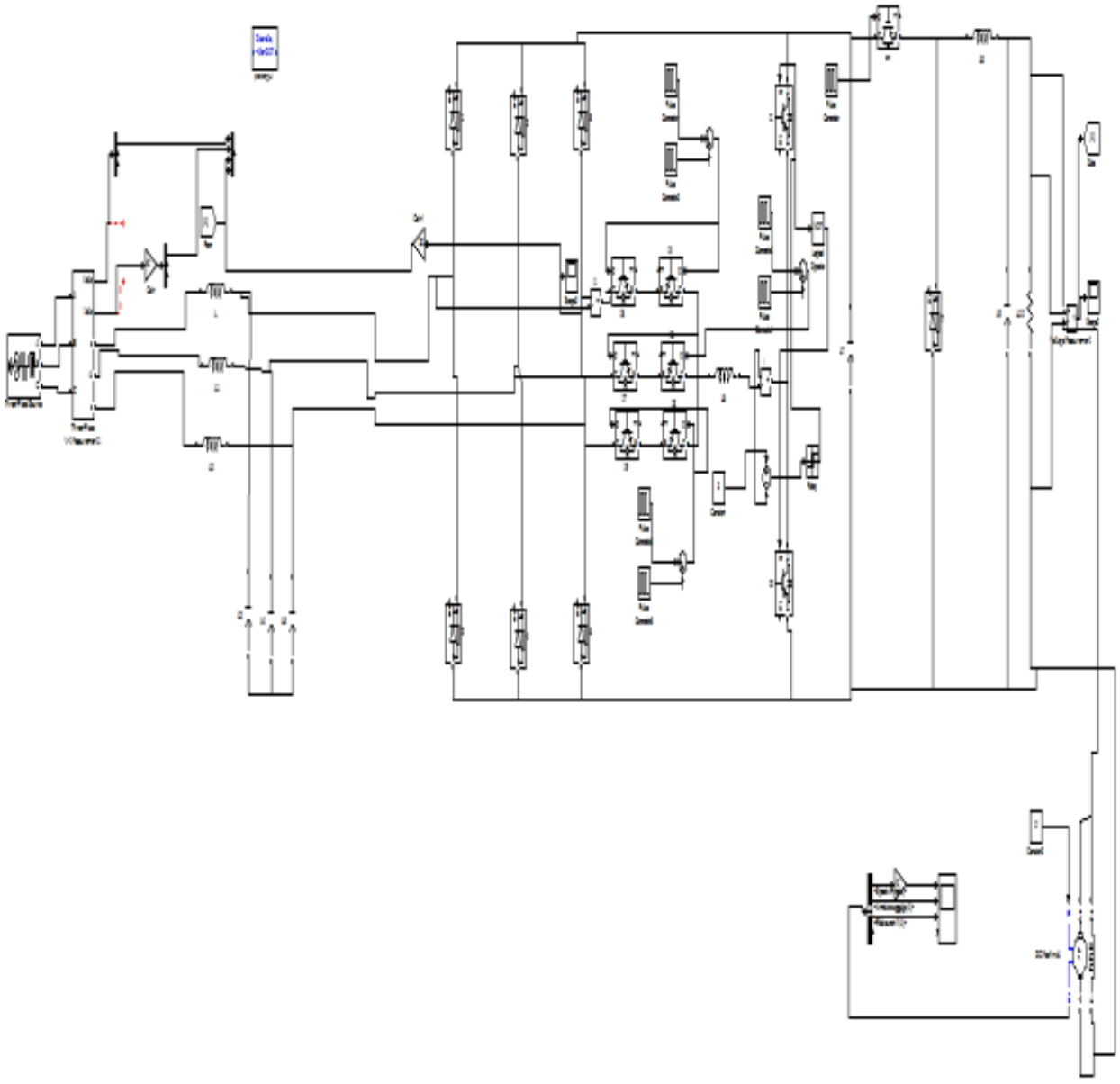


Out Put DC Voltage:

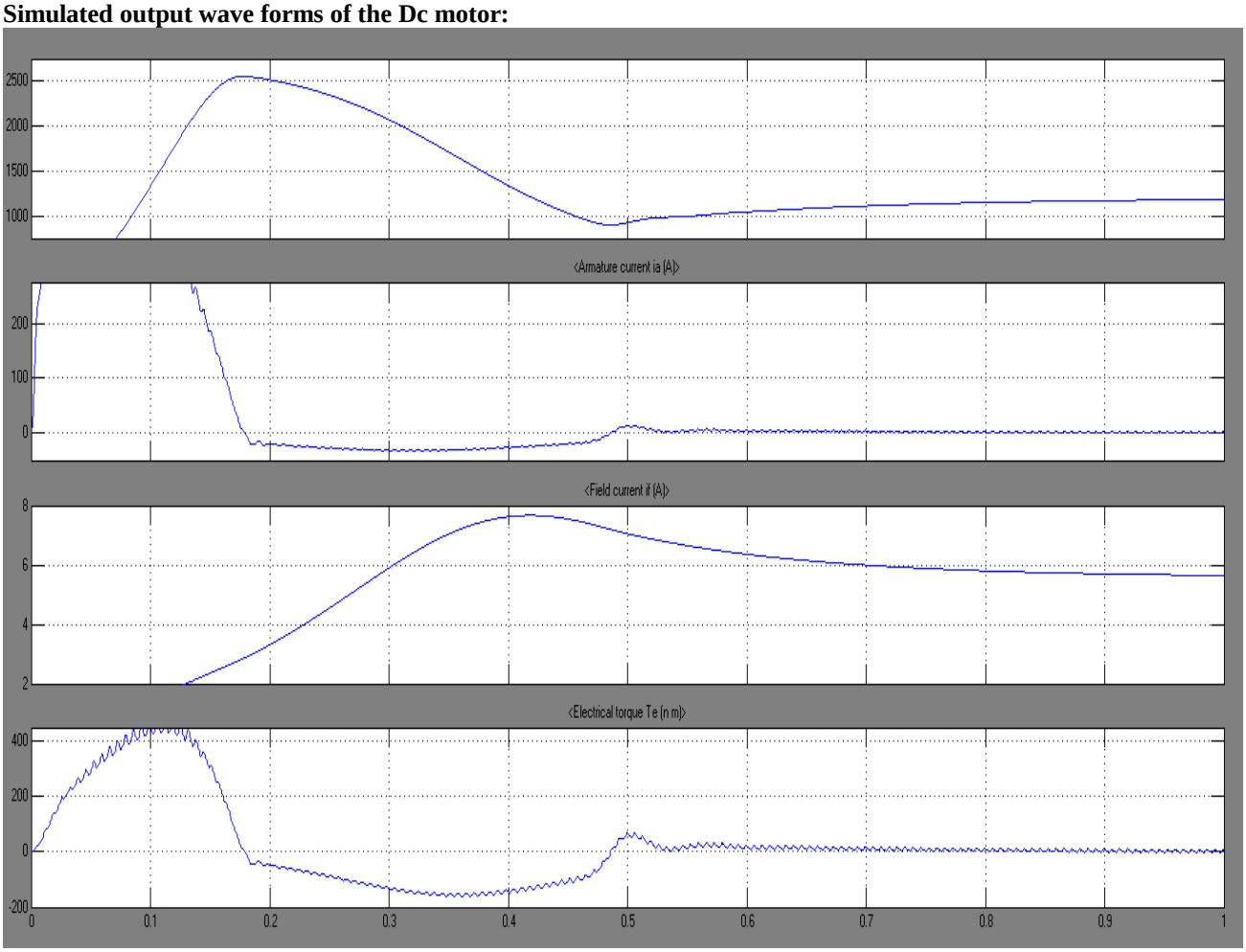


Description: As seen from above wave forms the input side power factor is unity that is there is no phase difference between the input voltage and current wave form by injecting current out of phase with the input current. There by it eliminates the harmonic currents in the input current wave and then it follows same as the input voltage, in order to get this result here I am using third harmonics injection rectifier circuit by using three bidirectional switches as shown above figure. Depending on the gating pulses given to the circuit in each phase it will get current is same as voltage wave form. And also the output voltage is Constant dc as shown in above wave form.

4.5 MATLAB/SIMULLINK MODEL OF DC MOTOR AT OUTPUT TO THE PROPOSED CIRCUIT:



Simulated output wave forms of the Dc motor:



Description: In above the parameters of the dc motor that is armature current, field current, speed, torque is analyzed as shown above.
The motor is settling down or coming to steady state at 0.5seconds as shown above.

CONCLUSION & FUTURE SCOPE

CONCLUSION:

This paper deals with the design and implementation of a three-phase buck-type PFC rectifier employing an active third harmonic current injection rectifier. The principle of operation, the main designing expressions, suitable modulation scheme, and PWM control have been described. the implemented system has been compared to another remarkable buck-type Swiss Rectifier. Finally DC-Motor is connected to the system and observes the motor is settling down to Study State at 0.5 Seconds.

FUTURE SCOPE:

The proposed power factor correction technique can be implemented by reducing the number of components in the DC-DC Converter which can reduce the size and cost.

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