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BER Analysis and Design of CDMA Transmitter and Receiver using Simulink

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Abstract — *Spread spectrum techniques are implemented in military applications to answer the challenges. In these techniques the transmitted spectrum is highly expanded using different signaling schemes. This paper mainly concentrates on Direct Sequence Spread Spectrum (DS/SS). A DS/SS System is designed using MATLAB – Simulink tool. To design the DS/SS system a Pseudo Noise (PN) generator is used with codeword length of 128 bits and code rate of 4 MHz along with Binary Phase Shift Keying (BPSK) modulator. The receiver is implemented with BPSK demodulator, correlator and synchronization unit. The system is equivalent base-band Binary Phase Shift Keying Direct Sequence Spread Spectrum (DS/SS) system. Then, the system performance is evaluated by comparing the received data and transmitted data. The effect of noise is analyzed by considering different channels and Bit Error Rate (BER) is calculated. The results show that, the performance of the system in the presence of AWGN is better when using Integrator and Dump filter in active correlator.*

Keywords- *Pseudo Noise (PN) code, BPSK modulator, Additive White Gaussian Noise (AWGN), Bit Error Rate, Integrator and Dump Receiver.*

I. INTRODUCTION

Due to simplicity and ease of implementation DS/SS system is one of the preferred spread spectrum system in the field of wireless communication system. In DS/SS system the baseband information is spreaded using PN sequence. The spreaded data is modulated with a sinusoidal oscillator. The performance of spread spectrum technique is always depends on its coding scheme. The parameters like code length, type of code and chip rate can be considered while designing a PN sequence [1],[4]. The capacity of a system can be increased by spreading the message signal in both time and frequency domains simultaneously. At the same time crosstalk is also considered while designing multi channel system. The effect of crosstalk and noise can be calculated in the form of Bit Error Rate. The objective of this paper is to design and implement a Direct sequence Spread Spectrum CDMA system using MATLAB- Simulink and study the bit-error rates in the presence of different noise channels. These types of communication models can be preferred between movable devices in the communication system [7].

II. CDMA TRANSMITTER AND RECEIVER

The CDMA communication system consists with transmitter and receiver.

A. Transmitter

The input message bits are spreaded by performing Modulo- 2 addition with PN sequence in the transmitter. The datarate of PN sequence depends on the codelength. The codelength of PN sequence is more than the data signal. The spreaded data signal is modulated with any shift keying modulations. There are several schemes available for modulation like BPSK, QPSK, M-QAM. The most widely used modulation scheme is the BPSK due to less probability error. In this design, BPSK modulation is used to modulate and transmits the spread signal [3]. The basic building blocks of a DS CDMA transmitter system are shown in Figure1.

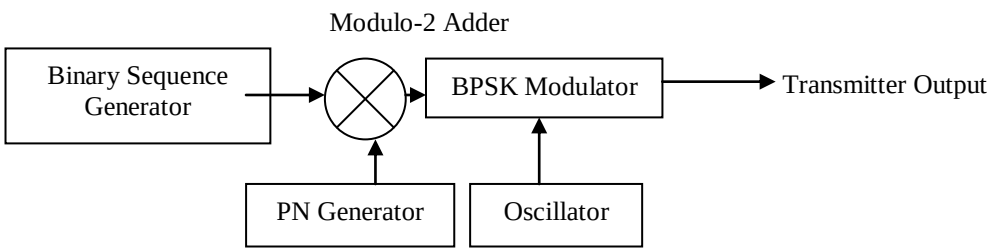

Figure.1 CDMA Transmitter

A.1 Design of PN Sequence Generator

In DS-CDMA communication system, the design of PN sequence generator is important.

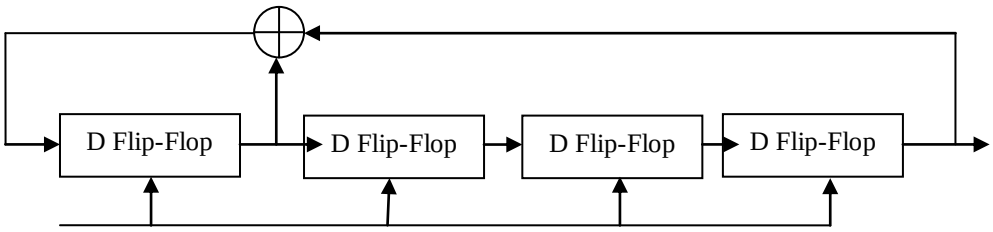

Figure.2. Block diagram of PN sequence generator

A Pseudo-random Noise (PN) sequence code is a binary sequence that exhibits random properties but it has a finite length sequence with deterministic characteristics. The PN sequence generator can be implemented using Linear Feedback Shift Registers (LFSR) to generate several types of PN sequences given in Figure.2. Maximal length sequences are LFSR based PN sequence generators which can produce the maximum possible length sequence. For n bit size shift registers the PN sequence length will be 2^n-1 bits [3].

A.2 Design of Spreader

Spreader is a Modulo-2 adder which performs Modulo-2 addition between the input data and PN sequence.

A.3 Design of BPSK Modulator

Modulation is the process of changing the characteristics of a carrier wave in proportion to the message signal to be transmitted. The carrier signal is given by

$$e(t) = E_C \sin(2\Pi f_c t + \Phi) \quad (1)$$

Where e(t) is instantaneous amplitude of the modulated signal. E_C is the amplitude of the carrier, f_C is the carrier frequency. Φ is the phase of the carrier.

In BPSK, the phase of the carrier signal changes in accordance with the binary input transitions by keeping amplitude and frequency of the carrier signal is constant. Carrier signal modulates according to spreaded binary data as shown below.

$e(t) = A_c \sin(2\Pi f_c t)$ is for binary 0

$e(t) = -A_C \sin(2\Pi f_c t)$ is for binary 1

A "0" represent a 0 degree reference phase and "1" represents a carrier shift of 180°.

B. Receiver

In DS-CDMA receiver shown in Figure.3, the input to the system is the BPSK modulated signal. The received BPSK modulated signal is multiplied with the locally generated carrier wave.

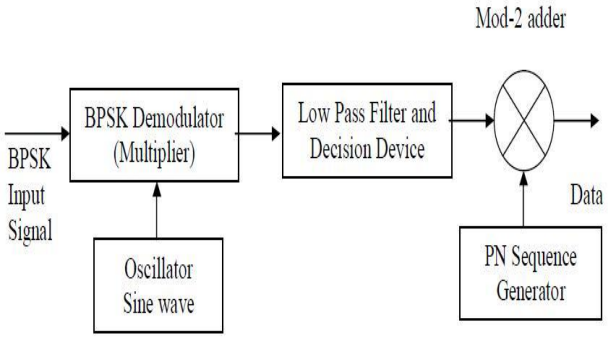

Figure.3 DS-CDMA Receiver

The multiplied signal is then passed through the low pass filter to get low frequency components only. A decision device recognizes logic 0 or logic 1 by comparing with the threshold voltage. The output of the decision device is the spreaded data signal.

The most sensitive part of the DS-SS receiver is the synchronization of the locally generated PN sequence and the sequence obtained from the decision device. The data signal may be interpreted as noise even if single mismatch between data and PN sequence. Therefore a suitable technique is required to obtain the synchronization between transmitter PN

sequence and receiver PN sequence [6]. Modulo-2 addition has been done between decision device output and PN sequence to obtain the data signal. In this design, common clock is used at receiver and transmitter, a small delay is considered between transmitted signal and received signal and it is modeled appropriately.

The multiplied output will have higher frequency components and channel noise as well. The high frequency components are eliminated using a suitable Low Pass Filter. The filtered low frequency component will have distortion in the signal. Hence a suitable 'Decision Device' is used to smoothen to binary sequence [5], [8].

III. IMPLEMENTATION OF CDMA TRANSMITTER AND RECEIVER

In this chapter CDMA Transmitter and Receiver are implemented using simulink shown in Figure.4

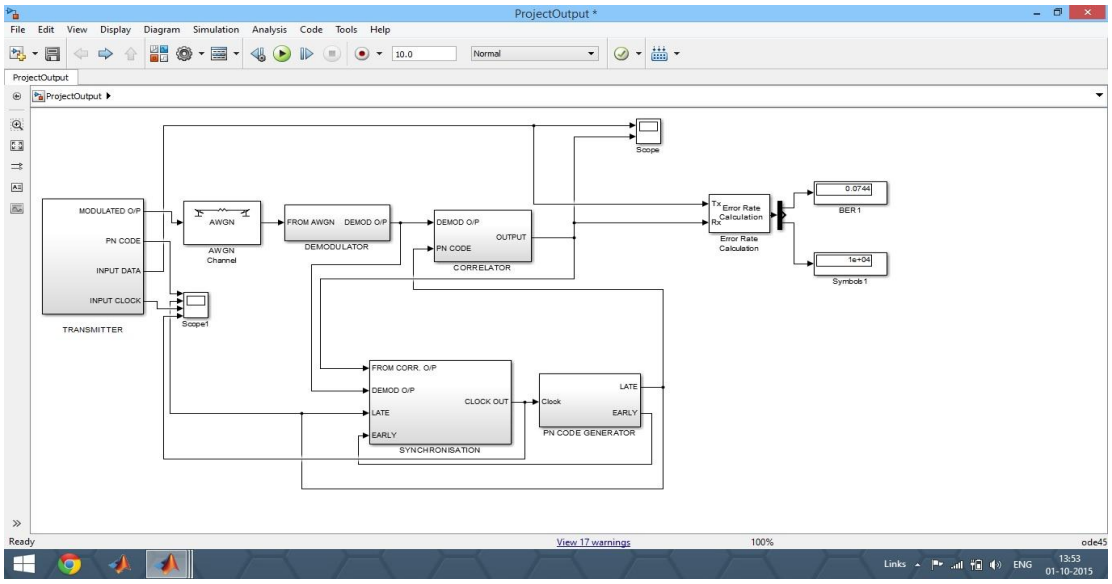

Figure.4. CDMA Transmitter and receiver

A. CDMA Transmitter

In the transmitter shown in Figure.5 the binary data is generated with the help of the random Integer generator. There are two pseudorandom sequence generators, by changing the position of switch any one of the PN Generator is selected to generate pseudorandom sequence. The spreaded signal is generated by multiplying the message signal and PN Sequence. The multiplier output is modulated with BPSK Modulator block [2]. Since modulation is performed in baseband, no radio frequency RF carrier is present. The unipolar to bipolar converter is used at the output of random integer generator to identify the data in the form of +1 and -1.

Since BPSK modulator block of simulink accepts the data in the form of logic0 and logic1, bipolar to unipolar converter is used prior to BPSK modulator block in the design.

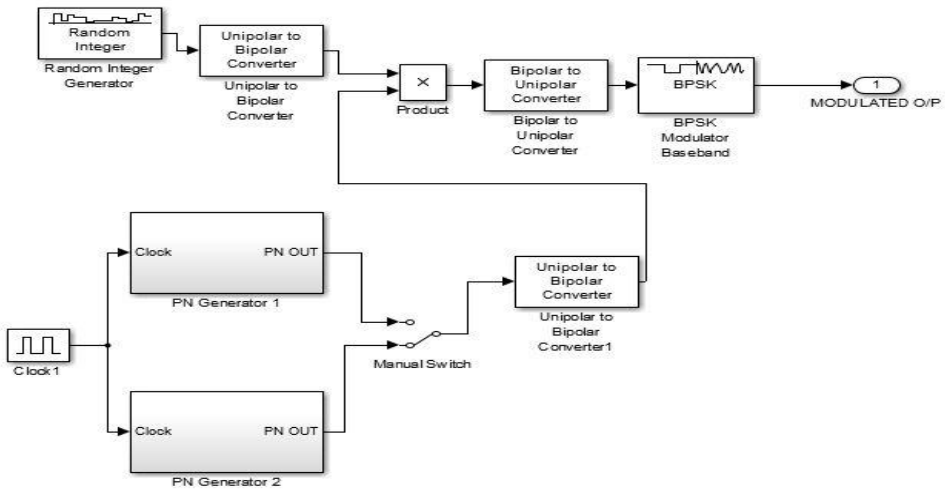

Figure.5.CDMA Transmitter

A.1. PN Sequence Genarator

There are two PN sequence generators, the PN Generator1 is shown in Figure.6. is implemented as maximal-linear code with a polynomial $f(x) = 1+X^2+X^7$ by using seven D-Flip-Flops. The outputs of two feedback shift register coefficients (X^7, X^2),are Ex-ORed to the input of the first stage D Flip-Flop, in order to get 128 bit length PN Sequence.

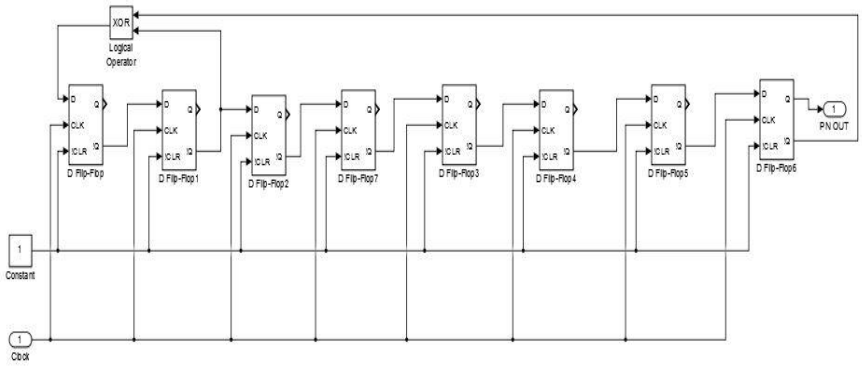

Figure.6.PN Generator1

The second PN sequenceshown in Figure.7. is generated with a polynomial $f(x) = 1+X^4+X^7$ with the same length of PN Generator1.

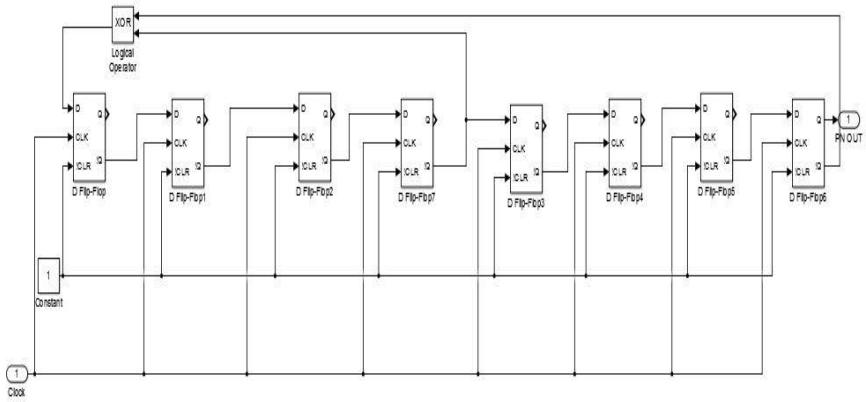

Figure.7. PN Generator2

A. CDMA Receiver

The receiver Shown in Figure.8 consists of demodulator, Active correlator, Synchronization unit and Local PN code generator with a clock, which is driven by voltage control oscillator (VCO).

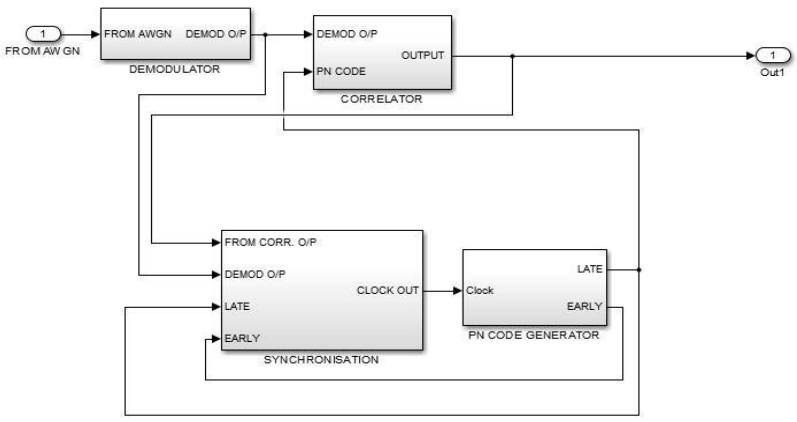

Figure.9. Correlator

B.1. Synchronization

The synchronization unit in the receiver are designed with acquisition, tracking, corrrelator and SLCU(Search/Lock Control Unit). The output of the correlator is compared with the preset threshold level in acquisition subsystem. If the correlator output is more than the threshold no delay is introduced in the local PN sequence otherwise the clock of local PN sequence is delayed by half chiprate and acquisition process is continued , and SLCU enables the tracking loop after the acquisition.

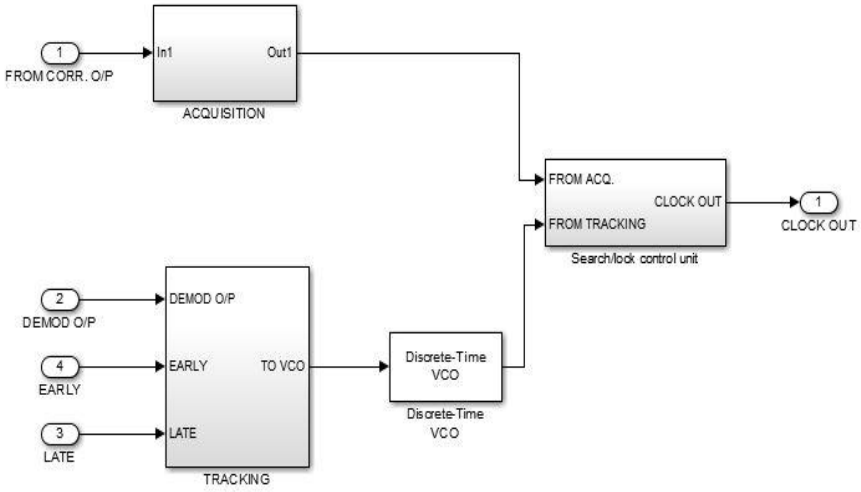

Figure.10. Synchronization Unit

Acquisition subsystem shown in Figure 11. uses a serial search, it contains square law envelop detector, integrator and dump receiver to detect the correlated signal energy at constant test intervals. The output of integrator and dump filter is compared with a preset threshold voltage. If the output of integrate and dump filter exceeds threshold voltage then the phase of local PN Sequence is corrected and tracking is initiated, otherwise SLCU block generates a phase update signal for the next phase test operation[7-8].

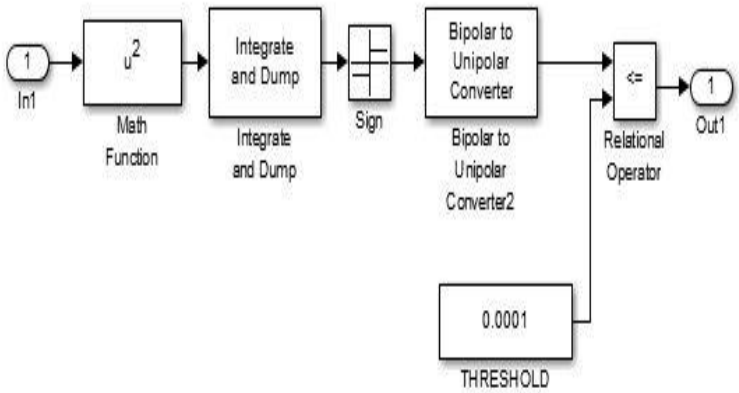

Figure.11. Acquisition block

The tracking subsystem shown in Figure 12 consists of two branches, the common input to these branches is the demodulated signal and the second input to the upper branch is the output of the local PN code generator (Early), while the second input to the lower branch is the output of the 6th flip- flop of local PN code generator (Late). Each branch consists of product (multiplier), integrate and dump filter and square law detector (envelop detector).The detected energy from both branches is subtracted to generate an error signal to excite the voltage control oscillator (VCO) to correct the local generated frequency.

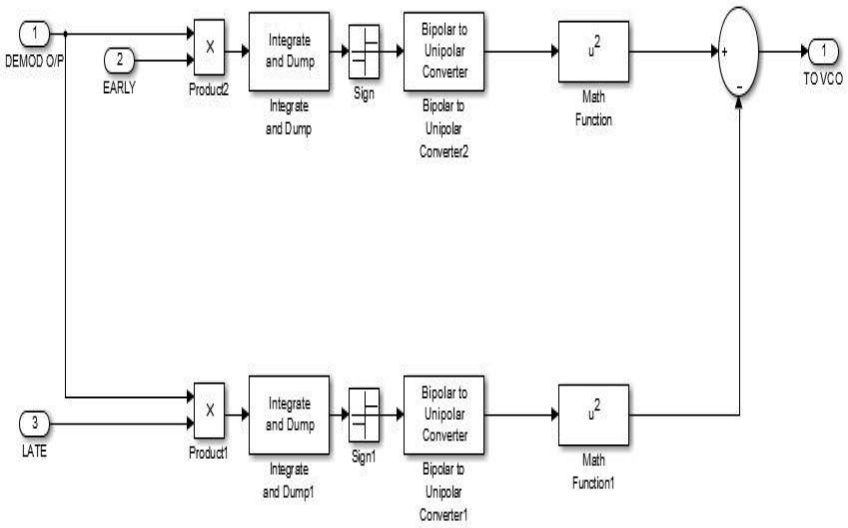

Figure 12. Tracking Subsystem

B.2. Search Lock Control Unit (SLCU)

The pulse generator generates a pulse with width equal to half of chip period. The inverted pulse is given to NAND gate with other input is output of acquisition subsystem to check the acquisition status. Thus the output of NAND gate is either a HIT (acquisition declaration pulse) or not, such that a new phase replica is tested. A J-K flip-flop configured as a T flip-flop to generate an extra half chip clock at each half chip period, In case, if there is no HIT has occurred. This is actually done after module-2 addition. Since the VCO output is polar, it must be converted to unipolar format to satisfy the requirement of XOR gate which produces the final update signal (local PN clock). However, if at each chip duration a phase update signal triggers a clock pulse then acquisition occurs and local PN sequence code is same as received PN sequence otherwise local PN sequence is faster than the received PN sequence. The implemented SLCU is shown in Figure 12.

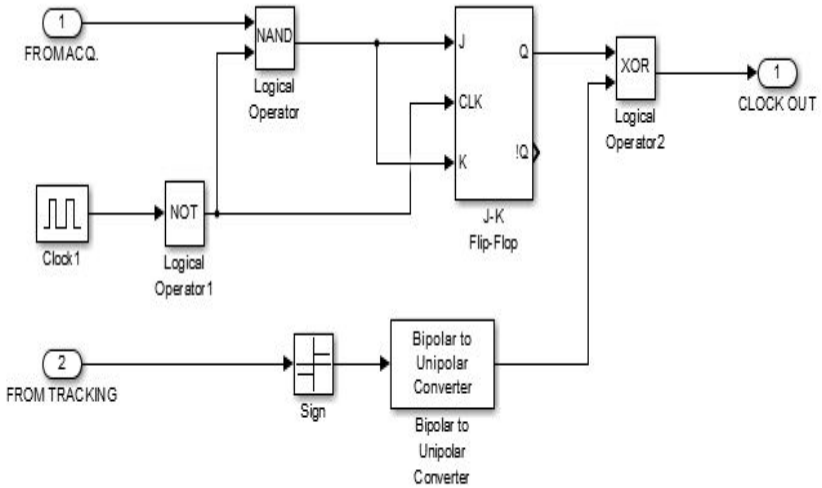

Figure.12. SLCU Block

IV. SIMULATION RESULTS

The generated Pseudo random Noise sequences (PN) is observed at Pn_out of PN generator1 shown in Figure 12. The Same code will repeat after every 15 clock cycles.

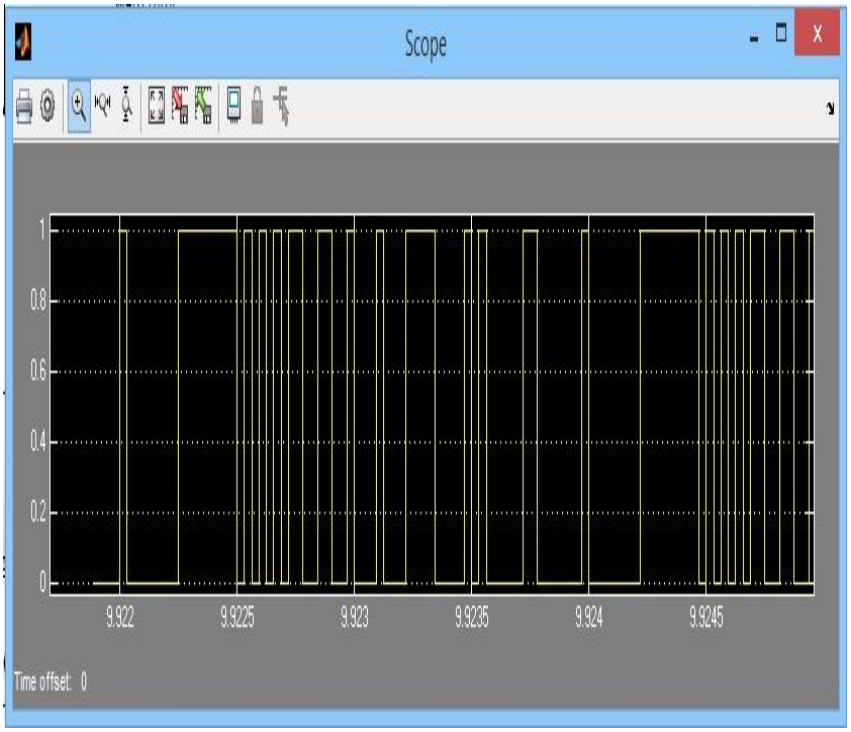

Figure.12.PN Generator1 output waveform

The message signal, PN sequence and multiplier outputs are shown in Figure 13.

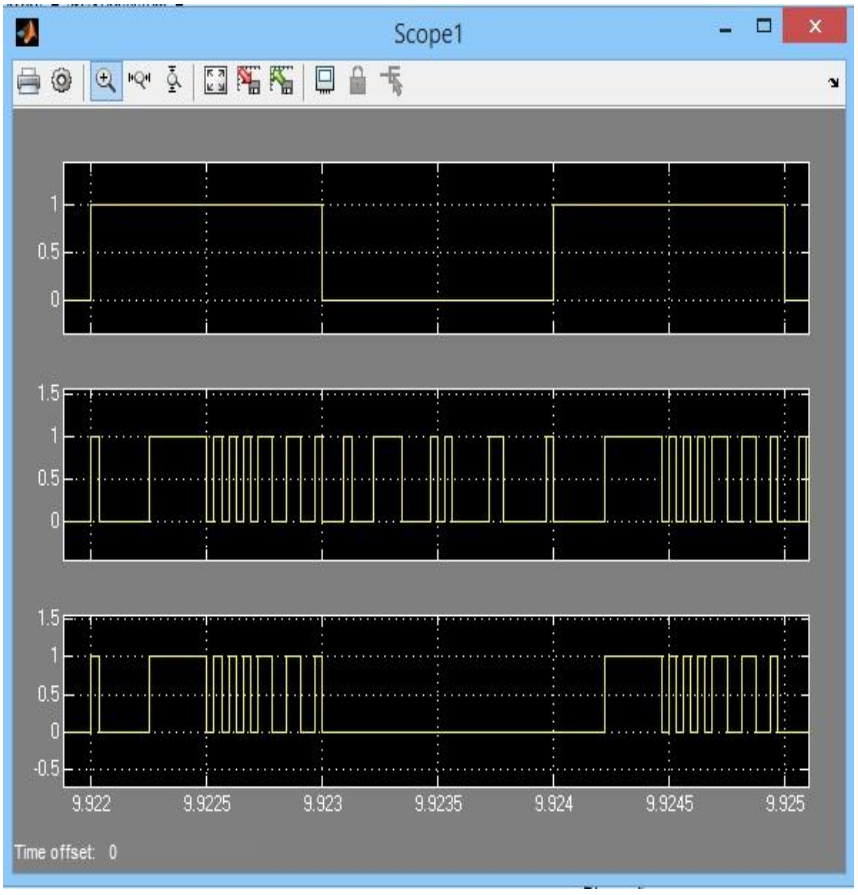

Figure. 13. CDMA transmitter output waveforms

Finally the output of demodulator and message signals are compared shown in Figure 14.

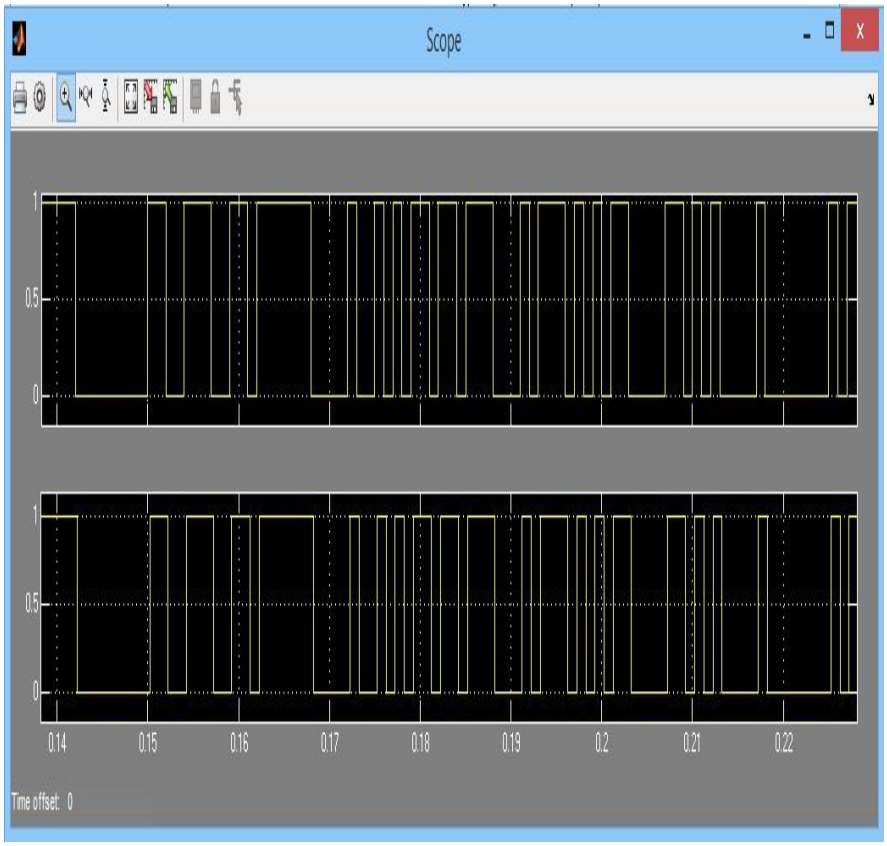

Figure.14. Receiver output

The BER values are computed for CDMA transmitter and receiver under different channel conditions. Computed BER values are given in Table I.

Table I
BER Values for different channels

Channel	BER
AWGN channel	0.0744
Multipath Racian channel	0.1386
Multipath Reyleigh channel	0.4789

V. CONCLUSION

CDMA is one of the important multiple access technique. In this paper the designed transmitter and receiver has been tested using an arbitrary chosen data stream, where these data have been transmitted through implemented transmitter and different channels. At the receiver BER is computed for different channels. A comparison has been done between the transmitted and received data and satisfactory results have been achieved for AWGN channel. Increasing the number of bits using the same topology, it is possible to reach the standard rates specified for CDMA.

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