Scientific Journal of Impact Factor (SJIF): 7.37

E-ISSN (O): 2348-4470
P-ISSN (P): 2348-6406

International Journal of Advance Engineering and Research Development

Volume 13,Issue 11,November 2026

Comparative Performance Analysis of Conventional and Reduced-Switch Single-Phase 21-Level Multilevel Inverters for Renewable Energy Applications.

Mrunal Bhawal, Prof. Narendra Neghinal

[1]*Electrical Engineering Department, Zeal College of Engineering & Research*
[2]*Electrical Engineering Department, AISSMS COE Pune 411001 Narendra.neghinal @zealeducation.com*
[1]*bhawalmrunal@gmail.com*

Abstract —*Multilevel inverters are widely used in power-electronic applications, particularly in renewable-energy systems, because they can provide improved output-voltage quality with reduced switching losses and lower harmonic distortion. This paper presents a comparison between a conventional single-phase 21-level cascaded H-bridge multilevel inverter and a single-phase 21-level topology that uses fewer switches and DC sources. The switching angles for both configurations, along with the timing required to generate the IGBT gate pulses, are determined using the Equal Phase (EP) method. The conventional cascaded H-bridge configuration requires 40 IGBT switches and 10 independent DC sources to produce a 21-level output. In contrast, the reduced-component topology achieves the same number of output levels using 8 IGBT switches and 4 independent DC sources. The reduced number of power devices simplifies the circuit structure and can lower the overall implementation cost. The performance of both inverter configurations is evaluated through MATLAB/Simulink simulations.*

Keywords—*Multilevel Inverter (MLI), Equal Phase(EP), Separate DC Sources (SDCS), Total Harmonic Distortion (THD).*

I. INTRODUCTION

Multilevel inverters have attracted considerable attention because of their capability to operate at higher voltage levels while offering high efficiency, reduced switching losses and improved total harmonic distortion (THD) performance. The development of multilevel inverter technology began with the three-level inverter introduced by Nabae et al. in 1981. These converters are now widely considered in power applications because they can meet increasing power-rating and power-quality requirements while reducing harmonic distortion and electromagnetic interference.

Several multilevel inverter configurations have been developed. The commonly used topologies include diodeclamped, flying-capacitor and cascaded H-bridge multilevel inverters. Among these, the cascaded H-bridge configuration is widely adopted. This paper compares a conventional single-phase 21-level cascaded H-bridge multilevel inverter with a single-phase 21-level inverter topology that uses a reduced number of switches and DC sources. The output-voltage waveforms of both configurations are obtained and evaluated through simulation [1], [2].

The switching angles for multilevel inverters can be determined using several methods, including:

- Equal Phase (EP) Method.
- Half Equal Phase (HEP) Method.
- Half Height (HH) Method.
- Feed Forward (FF) Method. In the present study, the switching angles for both the conventional single-phase 21-level cascaded H-bridge inverter and the reduced-switch, reduced-source 21-level inverter are calculated using the Equal Phase method. The two inverter configurations are then compared, and the analysis is presented in the following sections.

II. CONVENTIONAL SINGLE PHASE 21 LEVEL CASCADED H-BRIDGE MULTILEVEL INVERTER

A conventional single-phase cascaded H-bridge multilevel inverter consists of multiple H-bridge cells connected in series. Each H-bridge cell is supplied by an independent DC source, and the individual cell output voltages are combined to obtain the stepped AC output waveform. The resulting output voltage is formed by adding the voltage contributions of the cascaded H-bridge cells [3]. Figure 1 presents the generalized block diagram of a conventional single-phase m-level cascaded H-bridge multilevel inverter. By controlling the switching states of the individual H-bridge cells, the converter produces a stepped output waveform with 21 voltage levels. The series-connected cell voltages combine to form the overall output voltage. For this conventional configuration, the relationship between the number of output levels (m) and the number of DC sources (s) is m = 2s + 1, where each independent DC source supplies one H-bridge cell. Therefore, 10 separate DC sources are required to obtain 21 output levels. The output voltage, Va[(m−1)/2], is the sum of the individual H-bridge output voltages connected in series. The simulated output-

@IJAERD-2019, All rights Reserved

voltage waveform is presented in Figure 2. The THD and harmonic spectrum of the conventional single-phase 21-level cascaded H-bridge inverter are shown in Figure 3, obtained through FFT analysis in MATLAB/Simulink [4].

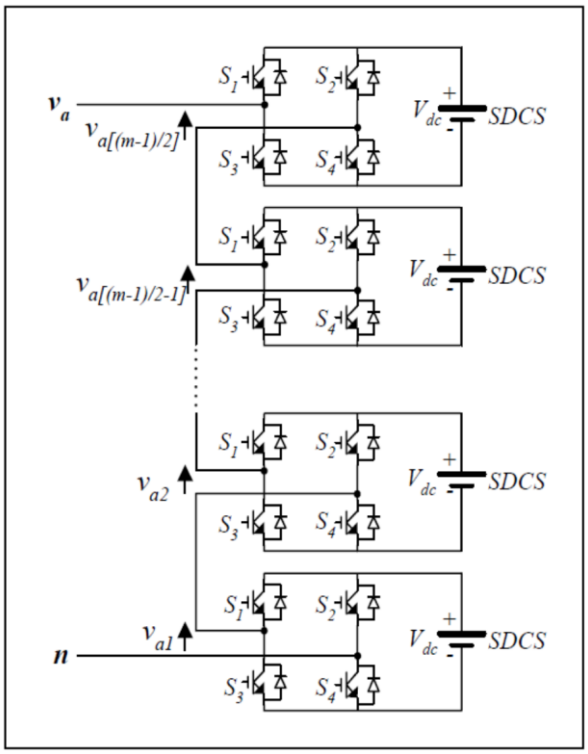


Figure 1. Generalized block diagram of Conventional Single Phase m-level Cascaded H-bridge Multilevel Inverter

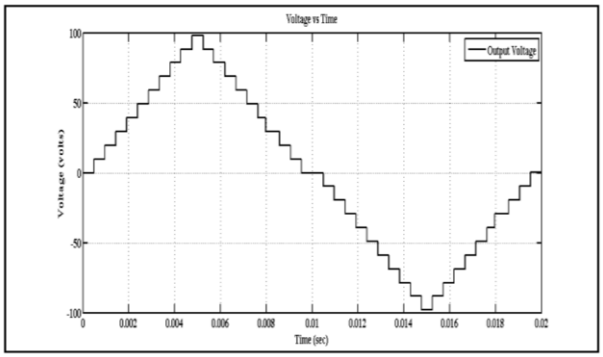


Figure 2. Voltage output of conventional single phase 21 level cascaded H-Bridge MLI by EP method

VOLTAGE LEVEL	NUMBERS OF ON SWITCHES
10 Vdc	1,2,6,10,14,18,22,26,30,34,37,38
9 Vdc	1,2,6,10,14,18,22,26,30,33,34,38
8 Vdc	1,2,6,10,14,18,22,26,29,30,34,38
7 Vdc	1,2,6,10,14,18,22,25,26,30,34,38
6 Vdc	1,2,6,10,14,18,21,22,26,30,34,38
5 Vdc	1,2,6,10,14,17,18,22,26,30,34,38
4 Vdc	1,2,6,10,13,14,18,22,26,30,34,38
3 Vdc	1,2,6,9,10,14,18,22,26,30,34,38
2 Vdc	1,2,5,6,10,14,18,22,26,30,34,38
1 Vdc	1,2,6,10,14,18,22,26,30,34,38
0	-

@IJAERD-2026, All rights Reserved

- 1 Vdc	4,8,12,16,20,24,28,32,36,39,40
-2 Vdc	4,8,12,16,20,24,28,32,35,36,39,40
-3 Vdc	4,8,12,16,20,24,28,31,32,36,39,40
-4 Vdc	4,8,12,16,20,24,27,28,32,36,39,40
-5 Vdc	4,8,12,16,20,23,24,28,32,36,39,40
-6 Vdc	4,8,12,16,19,20,24,28,32,36,39,40
-7 Vdc	4,8,12,15,16,20,24,28,32,36,39,40
-8 Vdc	4,8,11,12,16,20,24,28,32,36,39,40
-9 Vdc	4,7,8,12,16,20,24,28,32,36,39,40
-10 Vdc	3,4,8,12,16,20,24,28,32,36,39,40

III. CALCULATION OF SWITCHING ANGLES

Various techniques have been reported for determining the switching angles of multilevel inverters. In this work, the Equal Phase (EP) method is used to calculate the switching angles for both the conventional single-phase 21-level cascaded H-bridge inverter and the single-phase 21-level inverter with reduced switches and DC sources [5]. Equal Phase Method - Under the Equal Phase method, the switching angles are calculated using following equation $\alpha_i = i \times (180° / m)$ (3.1) where i = 1, 2, 3, 4, …, (m−1)/2 and m represents the number of output voltage levels. The switching angles are uniformly distributed over the angular interval from 0° to 180°. The switching states of the conventional single-phase 21-level cascaded H-bridge MLI are listed in Table 2.1. The switching angles obtained using the EP method, together with the corresponding PWM inputs, are applied to both the conventional cascaded H-bridge inverter and the 21-level inverter with reduced switches and DC sources. Figure 2 presents the output-voltage waveform of the conventional inverter generated using the EP method. Its harmonic spectrum is evaluated using the Fast Fourier Transform (FFT) function available in MATLAB/Simulink [6].

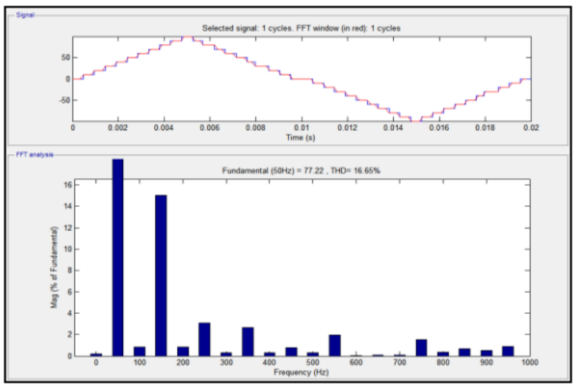


Figure 3. THD and FFT analysis of conventional single phase 21 Level Cascaded H-Bridge MLI

IV. PROPOSED 21 LEVEL MULTILEVEL INVERTER WITH REDUCED SWITCHES AND SOURCES

Figure 4 shows the circuit configuration of the proposed single-phase 21-level multilevel inverter with reduced switches and DC sources. The topology employs 8 IGBT switches, 4 independent DC sources and 8 power diodes [7]. Its operating principle is explained through the switching states listed in Table 1.

@IJAERD-2026, All rights Reserved

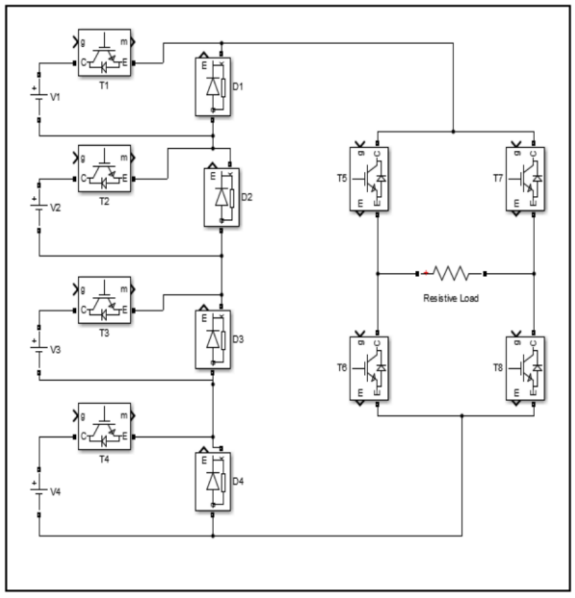


Figure 4. The circuit diagram of the proposed single phase 21 level multilevel inverter with reduced switches and sources

Operating modes:

- Mode 1: All eight switches (T1–T8) are in the OFF state, resulting in zero output voltage.
- Mode 2: When switches T1, T5 and T8 are turned ON, the load voltage is V1.
- Mode 3: When switches T2, T5 and T8 are turned ON, the output voltage is V2.
- Mode 4: When switches T3, T5 and T8 are turned ON, the output voltage is V3.
- Mode 5: When switches T4, T5 and T8 are turned ON, the load voltage is V4.
- Mode 6: When switches T1, T4, T5 and T8 are turned ON, the output voltage is V1 + V4.
- Mode 7: When switches T2, T4, T5 and T8 are turned ON, the output voltage is V2 + V4.
- Mode 8: When switches T3, T4, T5 and T8 are turned ON, the output voltage is V3 + V4.
- Mode 9: When switches T1, T3, T4, T5 and T8 are turned ON, the load voltage is V1 + V3 + V4.
- Mode 10: When switches T2, T3, T4, T5 and T8 are turned ON, the output voltage is V2 + V3 + V4.
- Mode 11: When switches T1, T2, T3, T4, T5 and T8 are turned ON, the output voltage is V1 + V2 + V3 + V4.
- Mode 12: When switches T1, T6 and T7 are turned ON, the load voltage is −V1.
- Mode 13: When switches T2, T6 and T7 are turned ON, the output voltage is −V2.
- Mode 14: When switches T3, T6 and T7 are turned ON, the output voltage is −V3.
- Mode 15: When switches T4, T6 and T7 are turned ON, the load voltage is −V4.
- Mode 16: When switches T1, T4, T6 and T7 are turned ON, the output voltage is −V1 − V4.
- Mode 17: When switches T2, T4, T6 and T7 are turned ON, the output voltage is −V2 − V4.
- Mode 18: When switches T3, T4, T6 and T7 are turned ON, the output voltage is −V3 − V4.
- Mode 19: When switches T1, T3, T4, T6 and T7 are turned ON, the load voltage is −V1 − V3 − V4.
- Mode 20: When switches T2, T3, T4, T6 and T7 are turned ON, the output voltage is −V2 − V3 − V4.
- Mode 21: When switches T1, T2, T3, T4, T5 and T8 are turned ON, the output voltage is −V1 − V2 − V3 − V4.

@IJAERD-2026, All rights Reserved

Table 1. The all positive level switching states of single phase 21 level MLI with reduced switches and sources with corresponding voltage levels.

voltage	T1	T2	T3	T4	T5	T6	T7	T8
V1+V2 +V3+V4	1	1	1	1	1	0	0	1
V2+V3+V4	0	1	1	1	1	0	0	1
V1+V3+V4	1	0	1	1	1	0	0	1
V3+V4	0	0	1	1	1	0	0	1
V2+V4	0	1	0	1	1	0	0	1
V1+V4	1	0	0	1	1	0	0	1
V4	0	0	0	1	1	0	0	1
V3	0	0	1	0	1	0	0	1
V2	0	1	0	0	1	0	0	1
V1	1	0	0	0	1	0	0	1
0	0	0	0	0	0	0	0	0

V. SWITCHING PULSE PATTERN BY EQUAL PHASE METHOD FOR SINGLE PHASE 21 LEVEL MLI WITH

REDUCED SWITCHES AND SOURCES

The Equal Phase method is used to determine the switching angles and generate the corresponding gate pulses. The resulting switching-pulse patterns are presented in Figure 5.

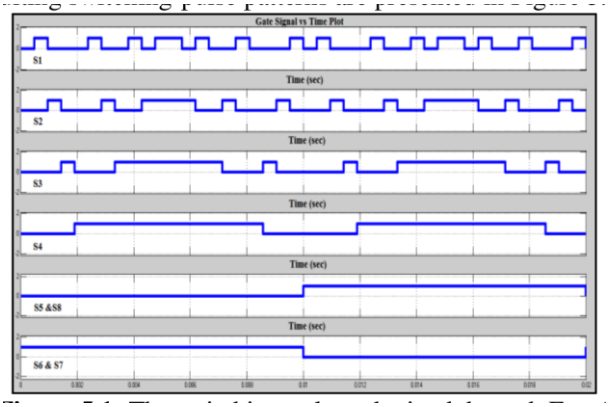


Figure 5. The switching pulses obtained through Equal

Pulse Method Figure 6 presents the output-voltage waveform of the proposed single-phase 21-level MLI with reduced switches and DC sources, obtained using the EP method. The corresponding harmonic spectrum is calculated using the FFT function in MATLAB/Simulink.

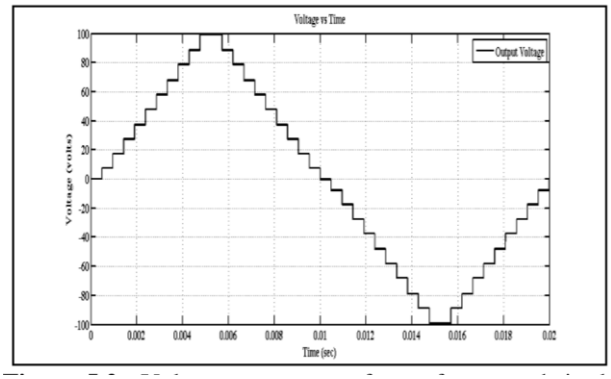


Figure 6. Voltage output waveform of proposed single phase 21 level MLI with reduced switches and sources by EP method

@IJAERD-2026, All rights Reserved

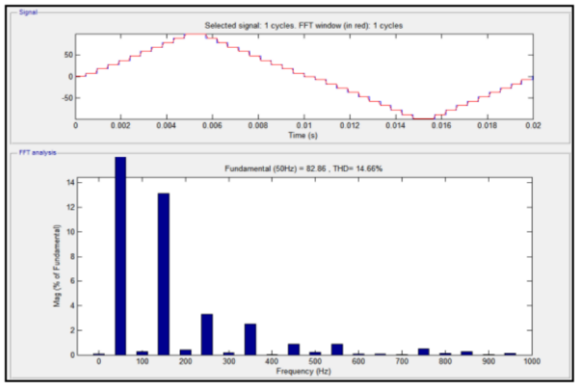


Figure 7. THD analysis of proposed single phase 21 level

MLI with reduced switches and sources by EP method

A comparison of the proposed and conventional inverter configurations is carried out in terms of the number of switches, diodes and DC sources required to generate a 21-level output voltage. The comparative results are summarized in Table 6.1. As indicated by the table, the proposed topology uses fewer switches and DC sources than the conventional cascaded H-bridge configuration.

	PARAMETER	**CASCADED CONVENTIO-NAL MLI**	**REDUCED SWITCHES AND SOURCES MLI**
1.	Number of Levels	21	21
2.	No. of DC Sources	10	4
3.	No. of Switches	40	8
4.	THD	16.65%	14.66%
5.	Cost	More	Less

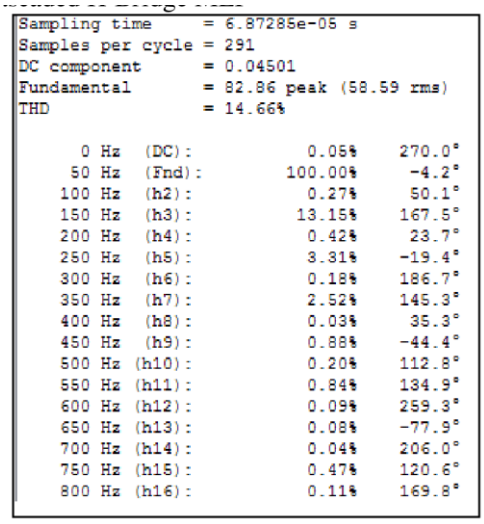
THD Analysis

```
Sampling time     = 0.000162602 s
Samples per cycle = 123
DC component      = 0.1587
Fundamental       = 77.22 peak (54.6 rms)
THD               = 16.65%

     0 Hz   (DC):          0.21%    270.0°
    50 Hz   (Fnd):       100.00%      0.3°
   100 Hz   (h2):          0.81%     21.6°
   150 Hz   (h3):         15.07%    181.7°
   200 Hz   (h4):          0.83%     -1.2°
   250 Hz   (h5):          3.08%     -2.4°
   300 Hz   (h6):          0.31%    213.5°
   350 Hz   (h7):          2.66%    185.1°
   400 Hz   (h8):          0.31%     18.2°
   450 Hz   (h9):          0.77%     23.9°
   500 Hz  (h10):          0.30%     -2.7°
   550 Hz  (h11):          1.94%    171.1°
   600 Hz  (h12):          0.03%    116.2°
   650 Hz  (h13):          0.08%     45.5°
   700 Hz  (h14):          0.06%    246.6°
   750 Hz  (h15):          1.51%    202.9°
   800 Hz  (h16):          0.32%     50.8°
```

Figure 8. Harmonic analysis of conventional single phase 21 Level Cascaded H-Bridge MLI

@IJAERD-2026, All rights Reserved



```
Sampling time      = 6.87285e-05 s
Samples per cycle = 291
DC component       = 0.04501
Fundamental        = 82.86 peak (58.59 rms)
THD                = 14.66%

     0 Hz   (DC):          0.05%    270.0°
    50 Hz   (Fnd):       100.00%     -4.2°
   100 Hz   (h2):          0.27%     50.1°
   150 Hz   (h3):         13.15%    167.5°
   200 Hz   (h4):          0.42%     23.7°
   250 Hz   (h5):          3.31%    -19.4°
   300 Hz   (h6):          0.18%    186.7°
   350 Hz   (h7):          2.52%    145.3°
   400 Hz   (h8):          0.03%     35.3°
   450 Hz   (h9):          0.88%    -44.4°
   500 Hz  (h10):          0.20%    112.8°
   550 Hz  (h11):          0.84%    134.9°
   600 Hz  (h12):          0.09%    259.3°
   650 Hz  (h13):          0.08%    -77.9°
   700 Hz  (h14):          0.04%    206.0°
   750 Hz  (h15):          0.47%    120.6°
   800 Hz  (h16):          0.11%    169.8°
```

Figure 9. Harmonic analysis of single phase 21 Level MLI with reduced switches and sources

VI. CONCLUSION

The single-phase 21-level multilevel inverter considered in this study produces 21 output-voltage levels using 8 switching devices and 4 independent DC sources. Compared with the conventional cascaded H-bridge configuration, which requires 40 switches and 10 DC sources, the proposed topology uses fewer power components and has a simpler circuit arrangement. The simulated output-voltage results show a THD of 14.66% for the reduced-switch topology, compared with 16.65% for the conventional configuration. The switching angles are calculated using the Equal Phase method, and the simulation results indicate a lower THD than that obtained with the normal pulse-generator input. The EP method also provides a higher RMS output voltage, as reported in the original simulation results. Further investigation may consider extending the same circuit arrangement to obtain a 31-level inverter.

REFERENCE

[1] M. bin Arif, S. Ayob, A. Iqbal, S. Williamson, and Z. Salam, "Ninelevel asymmetrical single phase multilevel inverter topology with low switching frequency and reduce device counts," in 2017 IEEE International Conference on Industrial Technology (ICIT), 2017.

[2] A. V. Singh and R. S. Singh, "A Comparative Study of Multilevel Inverter Topologies," International Research Journal of Engineering and Technology (IRJET), vol. 5, no. 3, Mar. 2018.

[3] V. Devi and S. Srivani, "Modified phase shifted PWM for cascaded H-bridge multilevel inverter," in 2017 Third International Conference Advances Electrical, Electronics, Information, Communication and Bio-Informatics (AEEICB), 2017.

[4] E. Najafi and A. H. M. Yatim, "Design and Implementation of a New Multilevel Inverter Topology," IEEE Transactions on Industrial Electronics, vol. 59, no. 11, Nov. 2012.

[5] N. Agrawal and P. Bansal, "A new 21-level asymmetrical multilevel inverter topology with different PWM techniques," in 2017 Recent Developments in Control, Automation & Power Engineering (RDCAPE), 2017.

[6] A. Prayag and S. Bodkhe, "A Comparative Study of Symmetrical and Asymmetrical Cascaded H-Bridge Multilevel Inverter Topology for Industrial Drive," International Research Journal of Engineering and Technology (IRJET), vol. 5, no. 2, Feb. 2018.

[7] M. T. Islam, M. S. Islam, and A. K. Bairagi, "A New Single Phase 21 Level Inverter Topology with Reduced Number of Switches and Sources for Renewable Energy Applications," in 4th International Conference on Electrical Engineering and Information and Communication Technology.

[8] C. M. Nirmal Mukundan, A. Al-Durra, K. Vineeth, P. Jayaprakash, T. H. M. EL-Fouly, and H. H. Zeineldin, "A New Multilevel Inverter With Reduced Component Count for a Standalone Solar Energy Conversion System," IEEE Transactions on Industry Applications, vol. 60, no. 2, pp. 3247– 3262, 2024, doi: 10.1109/TIA.2023.3331672.

[9] A. Seifi, S. H. Hosseini, M. T. Hagh, and M. Hosseinpour, "Reduced component cascaded switched capacitor multilevel inverter for renewable energy applications," The Journal of Engineering, vol. 2024, no. 12, Art. no. e70037, 2024, doi: 10.1049/tje2.70037.

[10] S. M. Sundaravel and M. B. Veerayan, "Reduced switch single source multilevel inverter topology for renewable photovoltaic system applications," Journal Power Electronics, vol. 25, no. 3, pp. 440–457, 2025, doi: 10.1007/s43236-024-00910-5.

@IJAERD-2026, All rights Reserved