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A Low-Power Single-Phase Dual-Modulous Prescaler

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Abstract — *In this paper, a wideband 2/3 prescaler is verified in the design of proposed wide band multimodulus 32/33/47/48 prescaler. A dynamic logic multiband flexible integer-N divider is designed which uses the wideband 2/3 prescaler, multimodulus 32/33/47/48 prescaler. Since the multimodulus 32/33/47/48 prescaler has maximum operating frequency of 6.2 GHz, the values of Program (P) and Swallow(S) counters can actually be programmed to divide over the whole range of frequencies. However, the P and S counters are programmed accordingly. The proposed multiband flexible divider also uses an improved loadable bit-cell for Swallow - counter and consumes a power of 0.96 and 2.2 mW, respectively, and provides a solution to the low power PLL synthesizers for Bluetooth, Zigbee, IEEE 802.15.4, and IEEE 802.11a/b/g WLAN applications with variable channel spacing.*

Keywords-*Very Large Scale Integration(VLSI), CMOS, Prescaler, Swallow Counter, Program Counter, Wireless LAN(WLAN), Phase Lock Loop(PLL), Source Coupled Logic(SCL), True Single Phase Clock(TSPC), Extended True Single Phase Clock(E-TSPC), Phase Frequency Detector(PFD), Bluetooth, Zigbee*

INTRODUCTION

WIRELESS LAN (WLAN) in the multi-gigahertz bands, such as Hiper LAN II and IEEE 802.11a/b/g, are recognized as leading standards for high-rate data transmissions, and standards like IEEE 802.15.4 are recognized for low-rate data transmissions. The frequency synthesizer is one of the power-hungry blocks in the RF front-end and the first-stage frequency divider. The best published frequency synthesizer at 5 GHz consumes 9.7 mW at 1-V supply, where the first-stage divider is implemented using the source-coupled logic (SCL) circuit, which allows higher operating frequencies but uses more power. The TSPC and E-TSPC designs are able to drive the dynamic latch with a single clock phase and avoid the skew problem. However, the adoption of single-phase clock latches in frequency dividers has been limited to PLLs with applications below 5 GHz. The Multiband Frequency Divider is usually formed by a prescaler, a program counter (P counter) and a swallow counter (S counter). Such a topology can provide a programmable division ratio of N X P + S, where N, P and S are the division ratios of three blocks respectively.

I. DUAL-MODULOUS PRESCALER

The prescaler is the most challenging part in the high-speed frequency-divider design because it operates at the highest input frequency. A dual-modulus prescaler usually consists of a divide-by-2/3 (or 4/5) unit followed by several asynchronous divide-by-2 units. The operation of the divide-by-2/3 unit at the highest input frequency makes it the bottleneck of the prescaler design. To achieve the two different division ratios, D flip-flops (DFFs) and additional logic gates, which reduce the operating frequency by introducing an additional propagation delay, are used in the unit. The power consumption of this divide-by-2/3 unit, which is the greatest portion of the total power consumption in the prescaler, significantly increases due to the power consumption of the additional components.

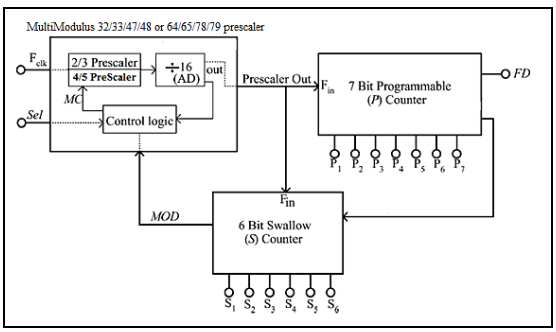

Figure.1 Dual Modulus Prescaler

II. WIDEBAND SINGLE-PHASE 2/3 PRESCALER

The E-TSPC 2/3 prescaler reported in consumes large short-circuit power and has a higher frequency of operation than that of 2/3 prescaler. The wideband single-phase clock 2/3 prescaler used in this design was reported which consists of two D-flip-flops and two NOR gates embedded in the flip-flops as in Figure. 2.

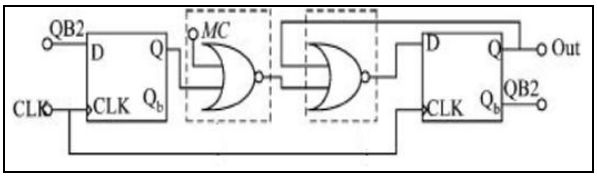

Figure. 2 Wideband Single-Phase Clock 2/3 Prescaler

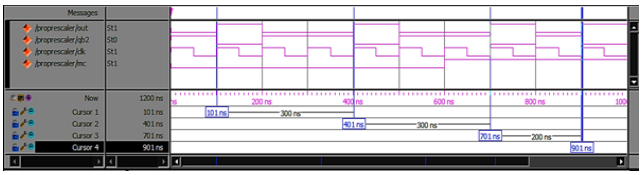

Figure. 3 Simulation Result of 2/3 Prescaler

III. WIDEBAND SINGLE-PHASE 4/5 PRESCALER

The Wideband Single-Phase 4/5 Prescaler can be designed in the similar fashion as the 2/3 Prescaler is designed. The Simulation result is shown in Figure. 4.

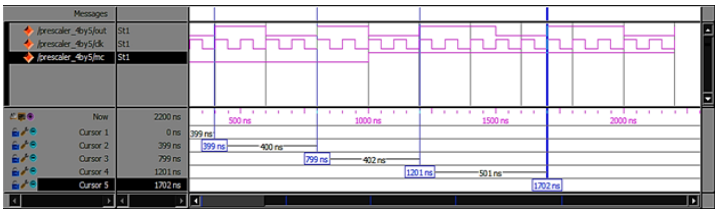

Figure. 4 Simulation Result of 4/5 Prescaler

IV. P-COUNTER

The program counter is responsible for counting *P* pulses of *SlowCLK* before outputting a pulse to the phase/frequency detector and resetting itself and the swallow counter. The implementation used in this paper, using a 7-bit ripple counter, a 7-bit comparator, and a zero-detector is shown in Figure. 5. The ripple counter is clocked by *SlowCLK*, and increments its count by one each clock cycle. At each stage, the 7-bit comparator compares each count bit to the corresponding bit in the control signal, and outputs a 0 for each equal bit. When the zero-detector detects equivalence in all of the 7 bits, indicating that the desired count has been reached, F_{out} is driven high. On the next clock cycle, the program counter is reset to zero and the count is restarted. In addition, the output pulse on F_{out} is used to reset the count of the swallow counter, indicating the end of one complete cycle of the frequency divider.

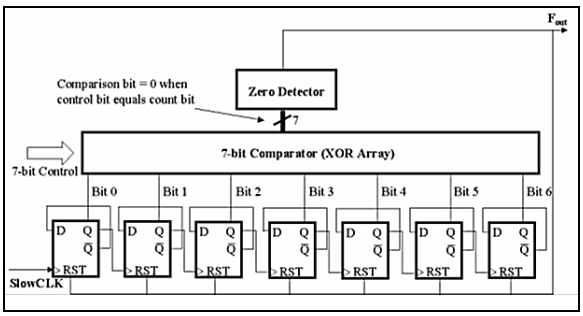

Figure. 5 7-Bit Program Counter

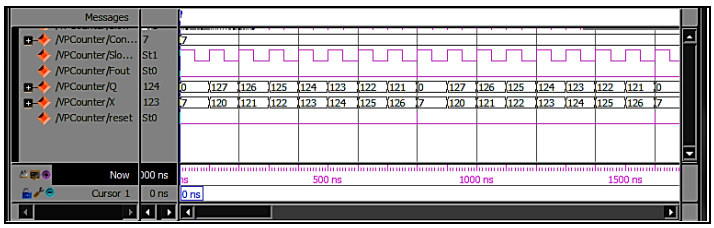

Figure. 6 Simulation Result of 7-Bit Program Counter

V. S-COUNTER

The swallow counter, as indicated in Figure. 7, is used to count *S* pulses of *SlowCLK* before asserting the *modulus control* signal and changing the modulus of the DMP to *N*. A comparator compares each count bit with its corresponding bit in the control signal, and a zero-detector asserts **modulus control** when all bits are equal. However, the swallow counter does not reset when the count is reached, but masks the input clock using an AND gate connected to the inverse of **modulus control**. As a result, the ripple counter stops counting when the count is reached, and the state of the circuit is maintained until a reset signal (**SwallowRST**) is received from the program counter. the control signal must be set to *S-1*, since the zero-state is included in the count.

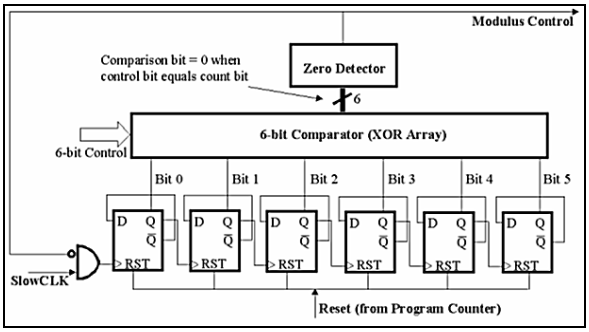

Figure. 7 6-Bit Swallow Counter

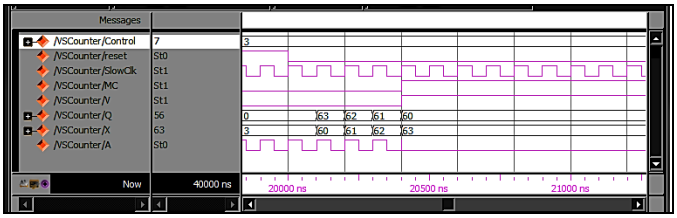

Figure. 8 Simulation Result of 6-Bit Swallow Counter

VI. MULTIMODULUS 32/33/47/48 PRESCALER

The proposed wideband multimodulus prescaler which can divide the input frequency by 32, 33, 47, and 48 is shown in Fig. 3.2. It is similar to the 32/33 prescaler used in, but with an additional inverter and a multiplexer. The proposed prescaler performs additional divisions (divide- by-47 and divide-by-48) without any extra flip-flop, thus saving a considerable amount of power and also reducing the complexity of multiband divider.

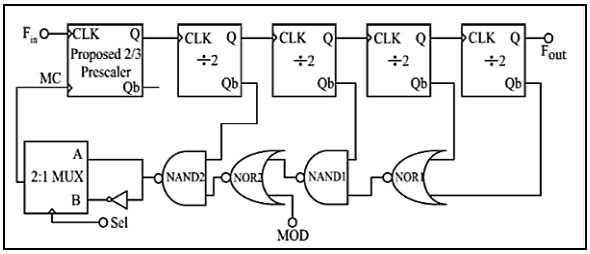

Figure. 9 Multimodulus 32/33/47/48 Prescaler

Case 1: Sel='0': $N = (AD*N_1)+(0*(N_1+1)) = 32$ ...(1)

$N + 1 = ((AD - 1)*N_1)+(1*(N_1+1)) = 33$ ...(2)

Case 2: Sel='1': $N + 1 = ((AD*(N_1+1))+(0*N_1)) = 48$ ...(3)

$N = ((AD - 1)*(N_1+1)) + (1*N_1) = 47$ ...(4)

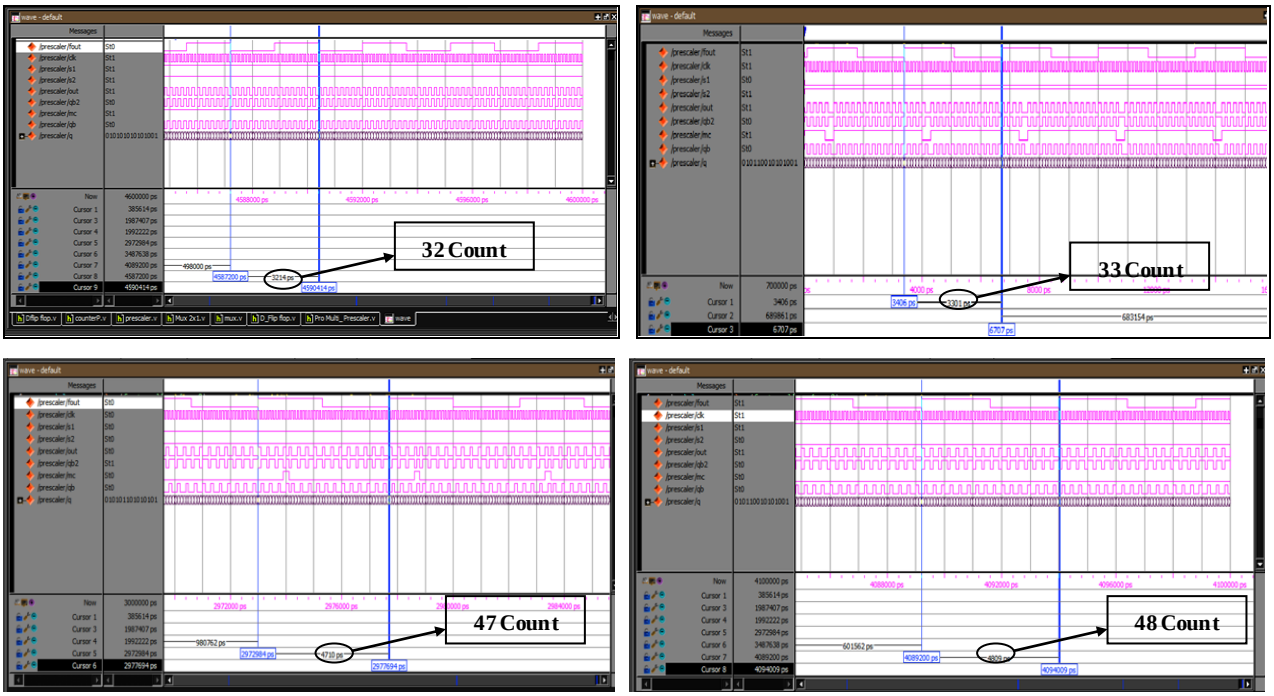

Figure. 10 Simulation Results of Multimodulus 32/33/47/48 Prescaler

VII. CONLUSION

The clock distribution network consumes nearly 70% of the total power consumed. This is the only signal which has the highest switching activity. This project is highly useful and recommended for communication applications like Bluetooth, Zigbee, WLAN. Our proposed multiband flexible divider is combined by 2/3 Prescaler and 4/5 Prescaler in multi modulus Prescaler. By using mux we can operate either 2/3 Prescaler and 4/5 Prescaler. It will operate 32/33/47/48 or 64/65/78/79 bandwidth.

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