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MultilevelInverter Technology for Induction Motor Drive by Sinusoidal PWM Technique

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Abstract*—Multilevel inverter is more recent and popular type control of power electronic converter that synthesizes a desired output voltage from several levels of dc voltages as inputs. The poor quality of voltage and current of a conventional inverter fed induction machine is due to the presence of harmonics and hence there is significant level of energy losses.In the proposed scheme a diode clamped three level inverter fed induction motor is simulated by SPWM technique. This circuiteffectively control drive performance through reduction in total harmonic distortion (THD).*

Keywords—Diode clamped, Multilevel Inverter, Induction motor, SPWM technique, THD.

I. INTRODUCTION

The inverters which produce an output voltage or a current with levels either 0 or $\pm$ V_{dc} are known as two level inverters. In high-power and high-voltage applications, these two-level inverters, however, have some limitations in operating at high frequency mainly due to switching losses and constraints of device rating. This is where multilevel inverters are advantageous. Increasing the number of voltage levels in the inverter without requiring higher rating onindividual devices can increase power rating. The unique structure of multilevel voltage source inverter's allows themto reach high voltages with low harmonics without the use of transformers or series-connected synchronized-switching devices. The harmonic content of the output voltage waveform decreases significantly.

The concept of multilevel inverter [1], [7], [11] control has opened a new possibility that induction motors can be controlled to achieve dynamic performance equally that of dc motors.

II. MULTILEVEL INVERTER

A multilevel converter has several advantages over a conventional two-level converter that uses high switching frequency pulse width modulation (PWM). The attractive features of a multilevel converter can be briefly summarized as follows.

1) Staircase waveform quality: Multilevel converters not only can generate the output voltages with very low distortion, but also can reduce the dv/dt stresses; therefore electromagnetic compatibility (EMC) problems can be reduced.

2) Common-mode (CM) voltage: Multilevel converters produce smaller CM voltage; therefore, the stress in the bearings of a motor connected to a multilevel motor drive can be reduced. Furthermore, CM voltage can be eliminated by using advanced modulation strategies such as that proposed in.

3) Input current: Multilevel converters can draw input current with low distortion.

4) Switching frequency: Multilevel converters can operate at both fundamental switching frequency and high switching frequency PWM. It should be noted that lower switching frequency usually means lower switching loss and higher efficiency.

Unfortunately, multilevel converters do have some disadvantages. One particular disadvantage is the greater number of power semiconductor switches needed. Although lower voltage rated switches can be utilized in a multilevel converter, each switch requires a related gate drive circuit. This may cause the overall system to be more expensive and complex.

Some inconvenient features can be derived from the increased number of switching devices and voltage sources which means a more complex control strategy. The continuous price reduction in power electronics components and also in digital signal processors can lead to the extension of multilevel technologies to low power applications. The extra number of devices might not necessarily mean an increment of conduction losses. Finally, among the wide variety of proposed MI circuits, the following classification is the most broadly accepted: neutral point diode-clampedcapacitor-clamped (flying capacitors) and cascaded multiple-cells (with separate DC sources) [1], [6], [7]. There are three basic multilevel converter topologies: diode clamped, flying capacitor, and cascaded H-bridge with separate dc sources. Among these topologies, diode-clamped converters are especially interesting because of their simplicity: the multiple voltage levels are generated passively through a set of series-connected capacitors.The diode clamped inverter provides multiple voltage levels from a series bank of capacitors. The voltage across the switches is only half of the DC bus

voltage. These features effectively double the power rating of voltage source inverter for a given semiconductor device.

III. DIODE CLAMPED THREE-LEVEL INVERTER

A. *Overall Simulation Circuit of three level inverter*

Fig.1 shows the power circuit of three level Inverter Fed Induction Motor. The clamped diode is used to connect the neutral point *N*to the midpoint of the transistor. The neutral N, generating an additional voltage level, yields the name "three-level inverter".
In this power circuit MOSFET is used as switching devices.
There are 12 MOSFETs in the inverter. For generation of three levels, each leg of three phase inverter has four MOSFET, two for upper half and two for lower half. There are two diodes used for neutral point clamping for each leg.

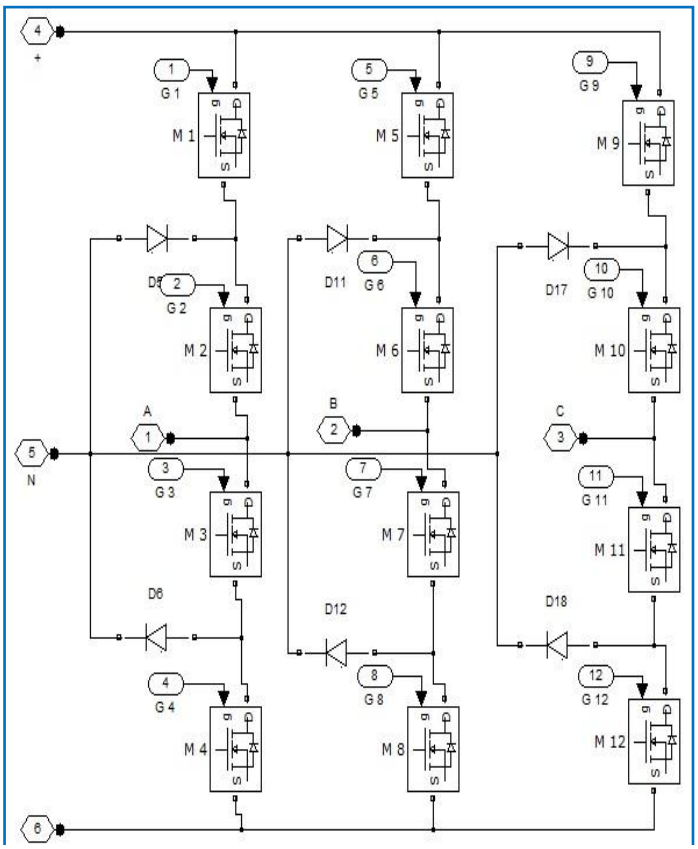


Fig. 1 Power circuit diagram of Three Level Inverter

B. *Gate Pulse for the MOSFET and Modulation Index*

Two classical high frequency modulation techniques for power converters are the carrier-based sinusoidal pulse width modulation (SPWM) [4], [7] and the space vector pulse width modulation. The SPWM technique considers each leg individually; therefore, it can be applied easily to converters. Fig. 2 shows carrier based PWM technique.

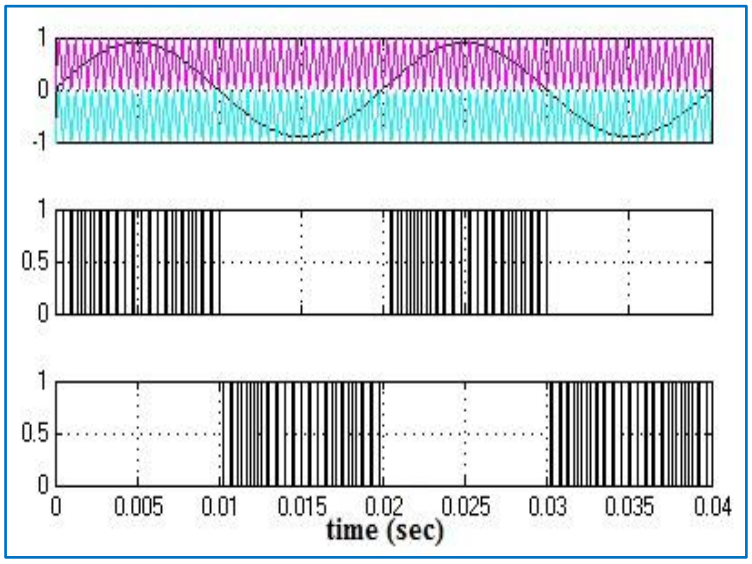


Fig. 2 Carrier Based PWM

For the three phase three level inverter there are three legs denotes each phase of three phase system. Each leg of inverter consists of four MOSFETs (M1-M4). For the generation of gate signal, sinusoidal PWM technique is used in which the carrier signal (triangular) and the reference signal (sinusoidal) are compared. For m-level inverter, the number of triangular wave is (m-1). So, there are two triangular waves one is upper half and another is lower half which is modulated with sine wave to get the gate signal. Fig. 3 shows the circuit for generation of gate pulse for inverter.

In SPWM modulating or reference waveform is a sine wave and is given by $V_m \sin(\omega t)$ and a triangular carrier signal vary between $+V_c$ and $-V_c$. The ratio the peak magnitude of modulating wave V_m and the carrier wave V_c give modulation index.

$$m = \frac{Vm}{Vc} \qquad (1)$$

The modulation index for this simulation is taken as 0.9.

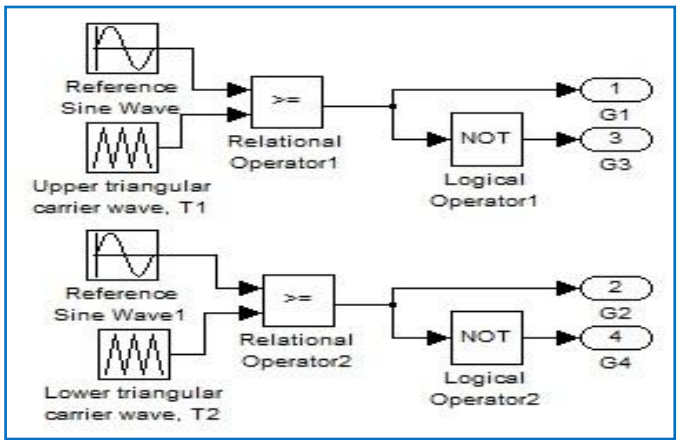


Fig. 3 Circuit Diagram for supplying Gate pulse to Inverter.

The gate pulse for G1 and G3 are compliment of each other.

Similarly, the gate pulse for G2 and G4 are compliment of each other.Similarly for other two phases in which reference wave (sine wave) is 120 and 240 degree phase shift with R-phase.Fig. 4 shows the modulation of a sinusoidal reference with two triangular carrier signals.

There are two triangular waves one is upper (T1) and the other is lower (T2) which is modulated with sine wave to get the gate signal. The gate signal generated on modulation with upper triangular and sine wave is given to G1 and G3. The gate signal of G1 and G3 are compliment of each other. Similarly the modulation of lower triangular wave and sine wave gives the gate signal for G2 and G4. The gate signal of G2 and G4 are compliment of each other. Same procedure of gate

signal is done for other phases. These modulating signals are used for triggering the switches of the inverter in the order to get three voltage levels.The output of the inverter is given to the three phase induction motor.
Each leg of the three level inverter contains four switching devices with diode clamped. Power electronics switches are switched in such a pattern to produce a staircase output voltages in three levels. Switching pattern to synthesize the three level are given in table1. State condition '1' denotes ON and state '0' denotes OFF state of switches.

TABLE1.

SWITCHING PATTERN

Output Voltage	**M1**	**M2**	**M3**	**M4**
$\mathbf{V_{dc}}$	1	1	0	0
$\mathbf{V_{dc}/2}$	0	1	1	0
0	0	0	1	1

IV. SIMULATION CIRCUIT

Fig. 4 shows the complete simulation circuit of three level inverter fed to induction motor drive [2], [3], [10]. Circuit parameters are giver in table 2. A three phase supply is rectified and then again inverted into controlled ac supply. This controlled output voltage is level voltage which has to be fed to induction motor.

TABLE 2.

CIRCUIT PARAMETER USED FOR SIMULATION

rms line-to-line voltage		400V
dc link capacitors	*C1, C2*	0.0085Ω, 0.045F
Carrier frequency	f_c	2KHz
Induction Motor		400V(rms), 4KW, 50Hz, 1430rpm
Modulating Frequency	f_m	50Hz

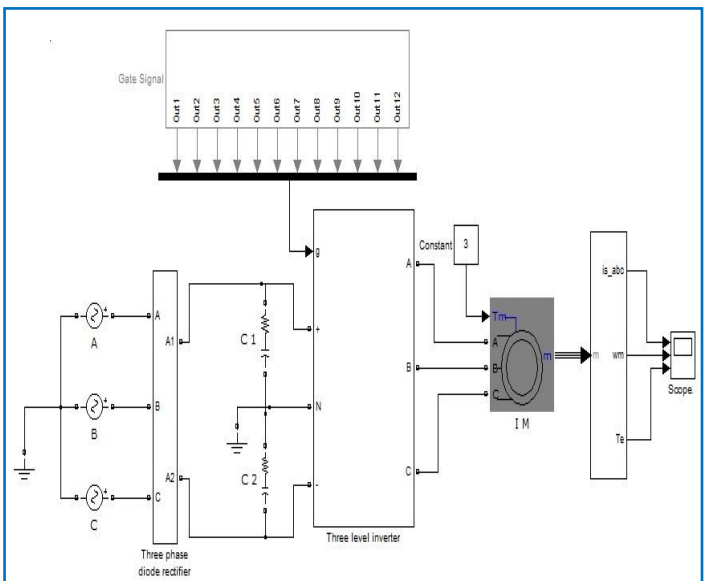


Fig. 4 Simulation circuit

V. SIMULATION RESULTS

A. *Line Voltage for 3-Level Inverter*

Fig. 5 shows the output line to line voltage of the three level three phase inverter. The output voltage is nearer to fundamental sinusoidal waveform, it means the harmonic level content in inverter output voltage is less.

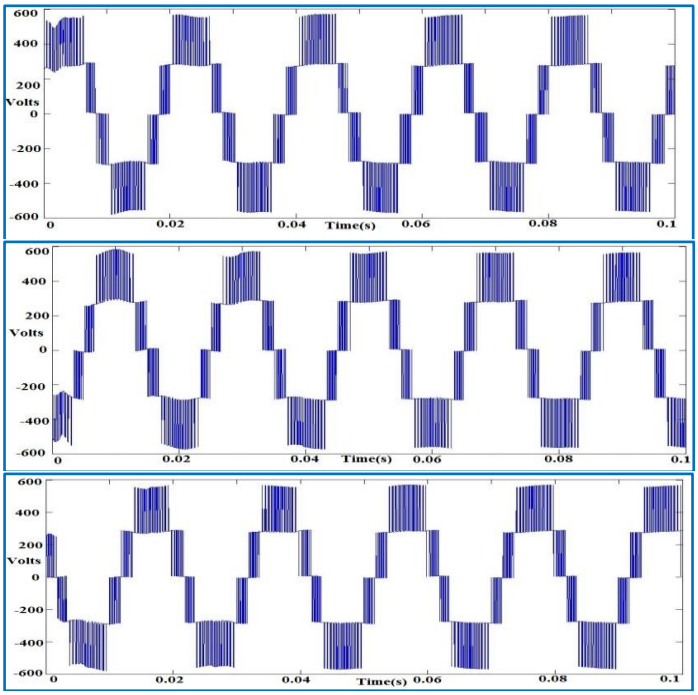
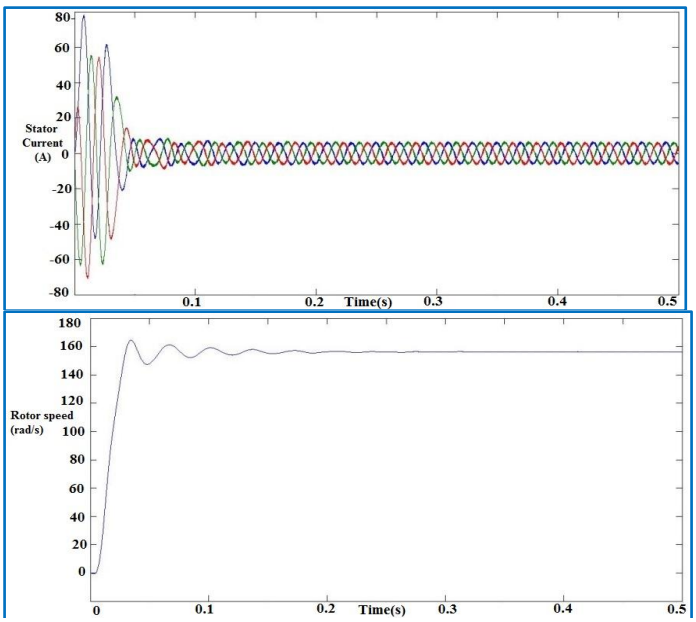


Fig. 5 The Line Voltage of Three-level Inverter V_{ab}, V_{bc} and V_{ca} respectively

B. Characteristics of Induction Motor

The output voltage of three level inverter is fed to induction motor and various parameters of induction motor has been studied. Fig. 6 shows the stator current, rotor speed and electromagnetic torque of IM.



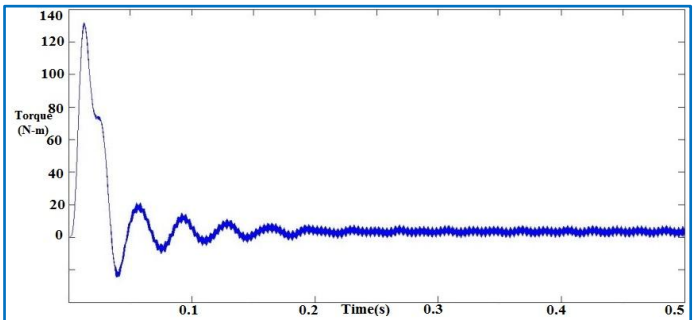


Fig. 6 shows the Stator Current, Rotor Speed and Electromagnetic Torque of Induction Motor respectively

C. FFT Analysis

FFT analysis of input voltage and stator current of induction motor has been performed. Fig. 7 shows the FFT analysis of line voltage and fig. 8 shows the FFT analysis of stator current. From FFT analysis of the output voltage of three level inverter it is observed. The Total HarmonicDistortion for a 3-level inverter (35.48 %). Further by using LC filter harmonics could be minimize. The harmonic level content in stator current is very low given by 4.31%.

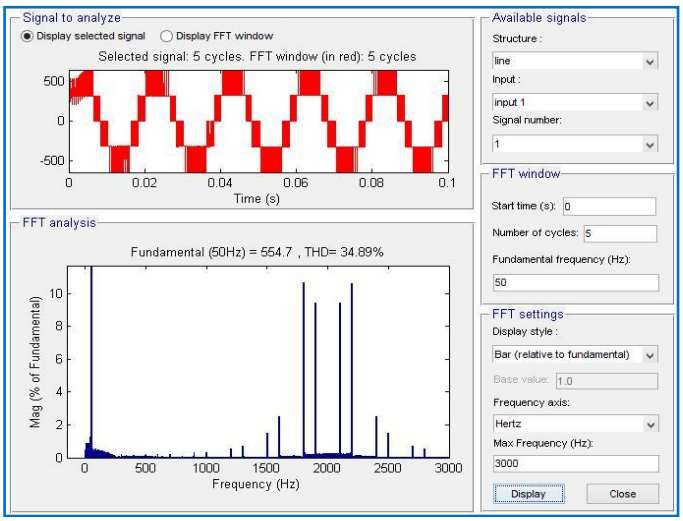


Fig. 7 FFT analysis for Line Voltage of Three-Level Inverter

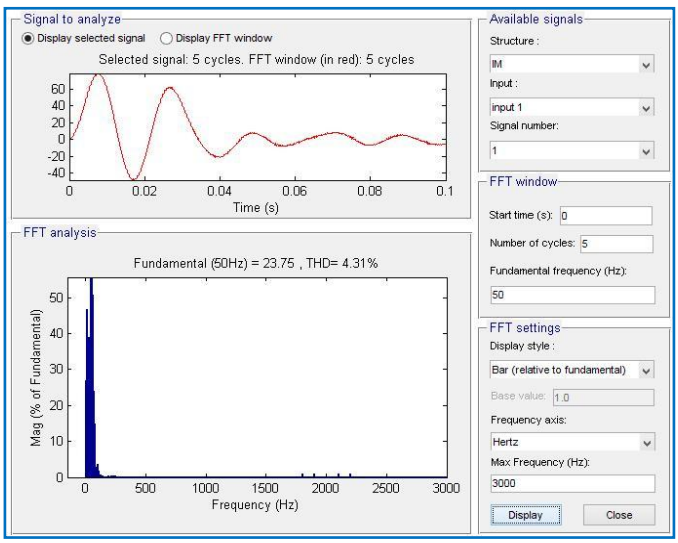


Fig. 8 FFT analysis for stator current of Induction Motor

VI. CONCLUSION

In this paper a three level neutral point diode clamped inverter is simulated and analyses. FFT analysis shows total THD in the output of Three-Level Inverter. From this, it is easily seen that Three-Level converter offers an output voltage with low THD. Multilevel converter can be applied to induction motor drives. As the results show, the harmonic content is low in stator current is also low. The proposed circuit is intended to effectively control the Drive Performance through reduction in Total Harmonic Distortion.

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