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All Digital Phase Locked Loop with High DCO resolution

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Abstract: *In this paper we propose a very high-resolution all digital phase locked loop (ADPLL). ADPLL is designed with the cell library and described in hardware description language (HDL). We design a digital controlled oscillator with 1.06 ps resolution for phase frequency detector minimized up to 5ps. So this ADPLL is suitable for system on chip application.*

Keywords: *All digital phase locked loop (ADPLL), Phase locked loop (PLL), Digital control oscillator (DCO),phase frequency detector(PFD)*

I. INTRODUCTION

Nowadays the phase-locked loops (PLLs) are widely used in various applications. For example, a chip embedded with its own clock generator to provide the high-speed clock signal, clock recovery, and synchronization of chips and jitter and phase noise reduction. Traditionally, the PLL is composed of some analog blocks, e.g., charge pump and voltage-controlled oscillator (VCO). The leakage problem will become increasingly serious in advanced CMOS processes. As a result, the difficulty and the complexity of designing an analog PLL increase as the technology process advances [1].

There are many advantages of the all-digital phase locked loop (ADPLL) over analog PLL. ADPLLs have better noise immunity, better testability, programmability, stability, and portability over different processes [4], [5], [6] and they can reduce the system turnaround time. The analog PLL suffers from reduced supply voltage and increased gate leakage as the CMOS scaling in nanometer. Also the difficulty and complexity of analog PLL increases as the technology process advances. The ADPLL reduce the sensitivity to process voltage temperature variations, area and power consumption.

The main building block of ADPLL is digital controlled oscillator (DCO). In the recent year design of DCO is improved with respect different specification needed by ADPLL. In the design of DCO the trade off is in the supply noise sensitivity, DCO resolution, frequency step size, frequency range, supply voltage.

In this paper the high resolution DCO is presented. Section II describes the basic architecture of ADPLL. Section III describes various components design of ADPLL and section IV presents the experimental result and section V discuss the conclusions.

II. ARCHITECTURE OF ADPLL

The basic architecture of ADPLL consists of phase frequency detector, ADPLL controller, digital controlled oscillator and frequency divider in the feedback loop. The major component of ADPLL is the digital controlled oscillator. For the different applications the design of digital controlled oscillator has to be changed. The parameters of digital controlled oscillator are the operating frequency range, maximum operating frequency, frequency resolution. General block diagram of ADPLL is shown in Fig.1.

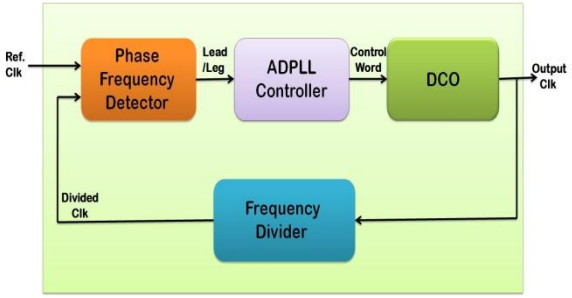


Fig.1 Basic block diagram of ADPLL

III. COMPONENTS OF ADPLL

The reference clock comes from internal clock generator. The divided_clk comes from the frequency divider. The Phase Frequency Detector (PFD) will generate the signal "lead" or "lag"

depended on the phase and frequency difference between the Ref_clk and divided_clk. If divided_clk leads Ref_clk, PFD generates a "lead" signal that will make the DCO frequency slow down. Conversely, then divided_clk lags Ref_clk, PFD generates "lag" signal to speed up the DCO frequency. When the ADPLL controller receives the "lead" or "lag" from the PFD, the ADPLL controller will change the DCO control code. Then DCO will generate the output clock. This clock is higher in frequency then the reference clock so it should be divided before applying it to the PFD. So frequency divider is used in the feedback loop. These blocks form a close-loop to achieve the "phase-locked" function. The design of ADPLL component is shown in the next section.

1. DESIGN OF PHASE FREQUENCY DETECTOR

The Phase/Frequency detector (PFD) detects the phase and frequency into difference between Ref_clk and Divided_clk, and then sends "lead" or "lag" signals to the ADPLL controller. The schematic of the PFD is shown as Fig. 2. When Divided_clk leads Ref_clk, "lead" will generate a high signal and "lag" remains low. Oppositely, When Divided_clk lags Ref_clk, "lag" will generate a high and "lead" keep low. In order to minimize the dead zone of the PFD, the pulse amplifiers are added into the PFD. The pulse amplifier circuit uses the chain of two-input AND gates to enlarge the pulse width applied to output registers. Since the pulse amplifier (Pulse Amp.) enlarge the phase difference between Divided_clk and Ref_clk, the following block can detect it.. From the simulation results, the minimum detectable phase error of the PFD is 5ps.

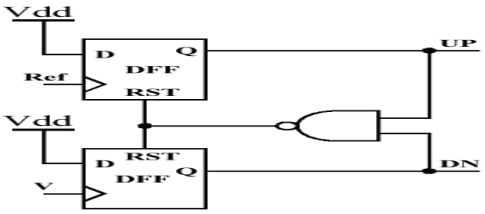


Fig.2 Phase frequency detector

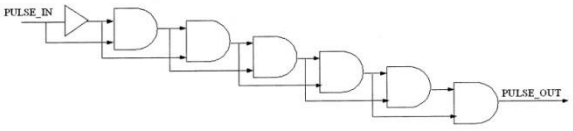


Fig.3 Pulse Amplifier

2. DESIGN OF ADPLL CONTROLLER

The ADPLL Controller has two operation modes: frequency acquisition mode and phase acquisition mode. Phase lock starts from the frequency acquisition mode. In the beginning, DCO oscillates at the middle operating range of the DCO, and the search step is one fourth of the DCO operating range. When the ADPLL controller receive the "lead" or "lag" signal from the PFD, the DCO control code will be decreased or increased respectively, and the frequency of DCO will be changed too. When the PFD output changes from lead" to "lag" (or vice versa), the search direction will be changed and he search step will be reduced to one half of previous step. After the search step reduces to one, the frequency acquisition mode completes Fig.3 shows the frequency acquisition mode operation of the ADPLL controller.

After the frequency acquisition mode completion, ADPLL enters the phase acquisition mode. The goal of his mode is to track phase of the reference clock. Fig.4 is the flow chart of phase acquisition operation. In the beginning of phase acquisition operation, the speed-up count (SPEEDUP_ COUNT) sets to zero. then the PFD output changes form "lead" to "lag" (or vice versa), that means the polarity changes, and then the search step will be reduced one half of the previous step. If the direction keeps the same way, he speedup count will add one. When the speed-up count equals to eight, the search step will be twice as the previous step. By increasing the search step, the phase racking accelerates.[7],[8]

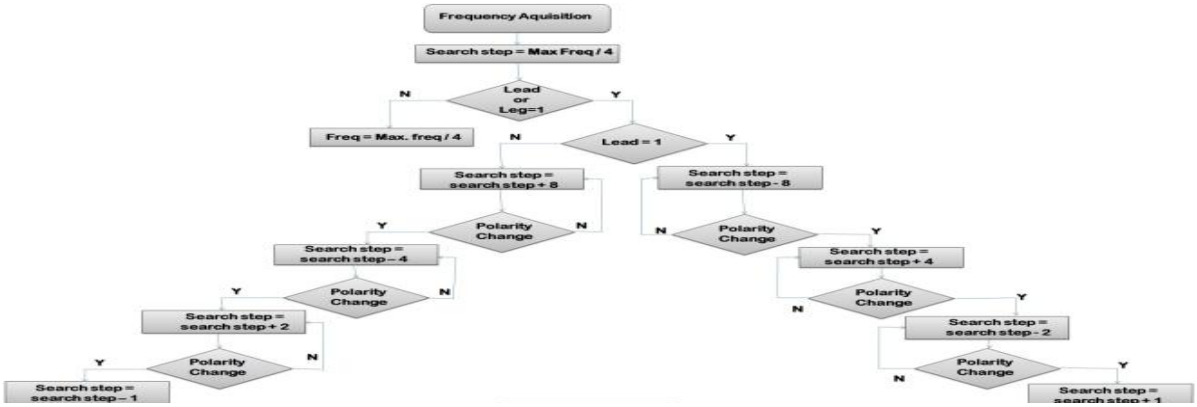


Fig.4 Frequency acquisition algorithm

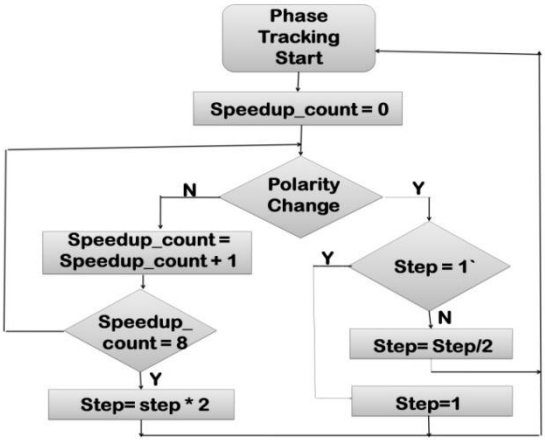


Fig.4 Phase acquisition algorithm

3. DESIGN OF DIGITAL CONTROLLED OSCILLATOR

The digitally controlled oscillator (DCO) is the heart of the ADPLL. DCO provides the ADPLL output clock signal. The frequency of DCO output clock is controlled by the DCO control code. Fig.5 shows the architecture of the proposed DCO. DCO is composed of three stages: coarse-tuning stage, 1st fine-tuning stage and 2nd fine-tuning stage. First, in the coarse-tuning stage, there are 128 different paths and only one path is selected by 128-to-1 path selection MUX. The tri-state buffers are used to construct path selection MUX. In order to reduce the loading capacitance in the path selection MUX output, the path selection MUX is divided into two stages. In the first stage, there are sixteen delay path groups (C1[0]-C1[15]), and each delay path group has eight different delay paths. Only one delay path in each delay group will be selected by the first stage selection signals (Con[0]-Con[7]). The second stage receives sixteen different delay paths from the first stage, and then it will select one of them by the second stage selection signals (Con1[0]- Con1[15]). From spice simulation, the resolution of the coarse-tuning stage is the delay time of one coarse delay cell, and it is about 60.71ps. Because there are 128 different delay paths, the controllable range of DCO is about 7.771ns (60.71ps * 128).Second, in order to increase the frequency resolution of the DCO, the 1st fine-tuning stage is added into the DCO design. Fig 5 shows the architecture of the proposed 1st fine-tuning stage. The 1st fine-tuning stage is composed of 32 shunted tri-state buffers and inverters. These tri-state buffers are controlled by the control signals (F1[0] F1[31]). The frequency of the 1st fine-tuning stage output depends on the number of "turn on" tri-state buffers. As the number of "turn on" tri-state buffers increasing, the output frequency increases. The controllable range of the 1st fine-tuning stage is 90.61ps and largest step is 17.74ps. Finally, in order to further increase the DCO resolution, the 2nd fine-tuning stage is added after the 1st fine-tuning stage. Fig 5 shows the circuit of the 2nd fine-tuning stage. The 2nd fine-tuning stage is composed of 32 three-input NOR gates to

improve the resolution. The basic concept of the 2nd fine-tuning stage is to control the gate capacitance of NOR gate with input state [7], [8].

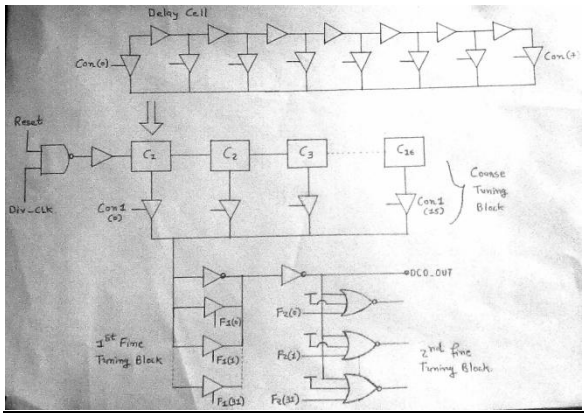
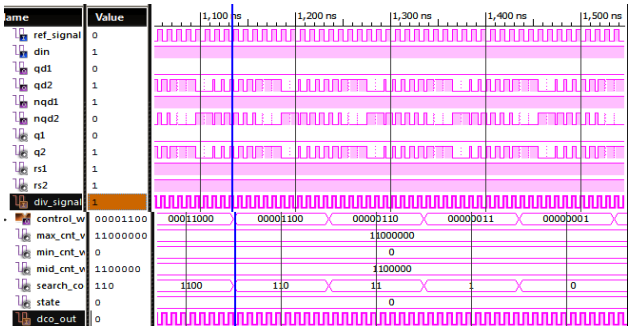


Fig.5 Digital Controlled Oscillator

The control signals (F2[0]-F2[31]) are used to control the input state of NOR gate. As the gate capacitance of NOR gate changing, the delay of the 2nd fine-tuning stage changes. From spice simulation, the controllable range of the 2nd fine-tuning stage is 34.06ps and step is 1.06ps. the OR gates chain to generate the duty cycle balanced clock signal.

IV. EXPERIMENTAL RESULTS

The proposed ADPLL is designed by cell-based design library. We use Hardware Description Language (HDL) to describe the ADPLL components .with 180nm CMOS process cell library. Finally, for operation stability, the power strip and ring should be added as many as possible. Fig.6 shows the simulation result of the proposed ADPLL. The core size of the ADPLL is 5001.tm x 5001Am, and the power consumption of the ADPLL is 4.22mW.



V. CONCLUSIONS

In this paper the new design of ADPLL is presented ith high resolution and wide operating range. The DCO has three controllable stages so we can achive high resolution DCO.also the proposed PFD has the minimazed dead zone due to use of pulse amplifier. The ADPLL is implemented in 180 nm cell library. Since all components are described using HDL language, it is easy to migrate different process technology. So it will reduce design time and complexity.

VI. ACKNOWLEDGEMENT

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