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# DESIGN & IMPLEMENTATION OF DIGITAL PHASE LOCKED LOOP USING FPGA

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***Abstract***— *Many circuits currently face the problem of reception of the clock with the same time at registers and flip-flops. This problem is sometimes known as clock skew. The main system clocks are generated with the help of oscillators and that clocks are distorted when reach at the registers and flip-flops. So there is requirement of a phase locked loop to address this problem. A phase locked loop looks for the matching of the clock frequencies seen at the clock inputs of various registers and flip-flops and the frequency generated by the oscillator.*

*This paper introduces designing of FM Receiver circuit inDigital environmentwhere Digital Phase Locked Loop (PLL) acts in the main role. The designing of FM Receiver circuit in digital environment requires behavior modelingin VHDL, then simulation result is analysed onModelSim SE 6.5b simulator. For describing timing and area constraintProject navigator Xilinx ISE 8.2i is used.Then circuitimplementation is done on FPGA.*

***Keywords***— DPLL, Loop filter, Phase detector, NCO,FIR,booth's algorithm.

## I. INTRODUCTION

Phase locked loop (PLL) is the heart of the many modern electronics as well as communication system. Recently stack of the researches have conducted on the design of phase locked loop (PLL) circuit and still research is going on this topic. Traditionally, PLLs have been developed in analog environment and since the development of the charge pump PLL is analog in nature, they have almost exclusively been analog. Recently, however, theresearchers have been focused on DPLLs because of their Power dissipation, flexibility,scalability, and higher noise immunity. Much research has conducted to realize alesser lock time PLL with higher lock range and have tolerable phase noise.

Clockgeneration and clock recovery is essential for networking, microprocessor and modern communication systems. The most versatile application of the phase locked loops (PLL) is Frequency synthesizers. Phase locked-loops (PLLs) are also used to generate well timed on-chip clocks in high-performance digital systems. Phase Locked Loop (PLL) mainlyprovides synchronization, clock synthesis and skew in modern wireless communication systems. Phase locked loops also find spacious range of application in several modern applications such as advance communication and instrumentation systems. Since PLL is a mixed signal circuit,designing ofPLL circuit involves many challenges at high frequency.

A phase locked loop looks for the matchingof the clock frequencies seen at the clock inputs of various registers and flip-flops and the frequency generated by the oscillator. The phase locked loop (PLL) plays a very important role for working of high performance microprocessors. Traditionally, a PLL is made to function as an analog building block, but integration of an analog PLL on a digital chip is difficult. Analog PLLs are also more convincible to noise and process variations. Faster lock time can be achieved withDigital PLLs which are attractive for clock generation on high performance microprocessors.

Since a DPLL network is a high order systemwith very complex nonlinear property, its system-level modeling is of paramount importance and behavioral modeling of such a system provides circuit level issues such as delay, possible metastability problems, etc. ,that is why VHDL-level modeling is a good candidate for designing of all digital FM receiver. This work targets the design and modeling of one simple DPLL with a FIR filter. This paper presents the result of VHDL modeling of anAll Digital FM Receiver circuit. In the context of the digital distributed clock generator, the following parameters of individual DPLL have an impact on the overall network performance:

- The DCO frequency resolution.
- The Phase-Frequency Detector (PFD) precision.
- The delays of logical elements.

## II. ARCHITECTURE DESCRIPTION

The system consists of a digital PLL cascaded with digital low pass filter acts as All Digital FM Receiver. The block diagram of system is shown in Fig. 1. The task performed by the PLL is to maintain coherence between the input (modulated) signal frequency, ωi and the respective output frequency, ωo via comparison of phases of input and output

signal.Since the system has self-correcting ability, the PLL can also track the frequency changes of the input signal once it is locked.

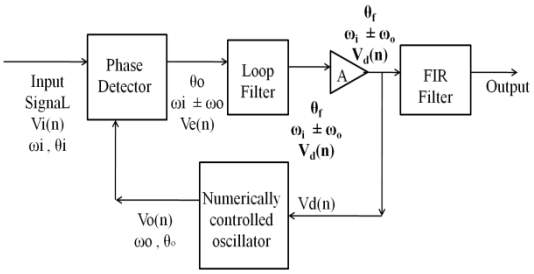



Fig. 1 Block diagram of FM receiver

A series of numerical values (digital signal) via 8-bit of analog to digital conversion (ADC) circuitis assumed asFrequency modulated input signal. The FM Receiver gets the 8 bit signal for every clock cycle and outputs the demodulated signal.

Digital PLL system is designed with the use of three basic parts: (1) Phase Detector (PD), (2) Loop filter, (3) Numerical-controlled oscillator (NCO).When inputsignalis not applied to the system, the NCO control voltage $V_d(n)$ is equal to zero. The NCO operates at a set frequency, $f_o$(or the equivalent radian frequency, ωo). This frequency is known as the free running frequency. At the time when an input signal is applied to the system, it is actually applied to phase detector. The phase detector compares the phase as well as the frequency of the input with the NCO frequency and generates an error voltage$V_e(n)$ that is related to the phase and the frequency difference between the two signals.

Beforeapplying to the control terminal of the NCO, this error voltage is filtered, amplified by factor of *A = 1/1024*. In this manner, this control voltage signal forces the NCO frequency to vary in such direction so that it reduces the frequency difference betweenωo and the input signal. If it is consider that the input frequency$\omega_i$ is sufficiently close to ωo, The NCO is synchronize or locked with the incoming signal because of the feedback nature of the PLL. Once in lock, the NCO frequency is identical to the input signal except for a finite phase difference.

This net phase difference of $\theta$e where

$$\theta e = \theta i - \theta o$$

is necessary to generate the corrective error voltage $V_d(n)$to shift the NCO frequency from its free-running value to the input signal frequency $\omega_i$and thus keep the PLL in locked stage. Theability of the system of being self-correct allows the PLL to track thefrequency changes of the input signal once it is locked, hence it can be act as FM demodulator in receiver system.

## III. VHDL MODEL

*1)Phase Detector*

Phase Detector (PD) detects phase error between input signal and output signal from NCO. Designing ofPhase Detector is done with the designing of a 2 input multiplier. Here one input is taken as frequency modulated signal, so this input signal (taken as $V_i(n)$) can be expressed as follows

$$V_i(n) = \sin(\omega_i n + \theta_i)$$

Feedback loop mechanism of the PLL will force NCO to generate sinusoidal signal$V_o(n)$ with the same frequency of$V_i(n)$, then

$$V_o(n) = \cos(\omega_i n + \theta_o)$$

Output of phase detector is product of these two signals, using familiar trigonometric identity we obtain

$$V_d(n) = K_d \sin(\omega_i n + \theta_i)\cos(\omega_i n + \theta_o)$$

$$= \frac{K_d}{2}\left[\sin(2\omega_i n + \theta_i + \theta_o) + \sin(\theta_i - \theta_o)\right]$$

$K_d$is the gain of the phase detector. In this eqthe first term and the second term contains high frequency componentandthe phase difference between$V_i(n)$ and $V_o(n)$respectively. By removing the first term through loop filtering, the phase difference can be obtained.The block diagram of phase detector is a multiplier shown in Fig.2.

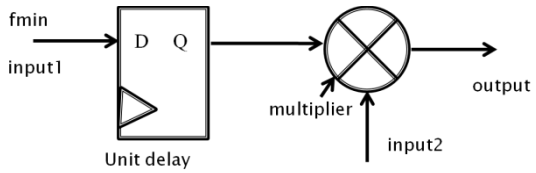



Fig. 2Phase Detector

Summary of operation:

• *input1*is fmin (modulated data), *input2* is taken fromthe output of NCO. Both the input areof 8 bitin 2's complement form, please see [2] for details.

• First Unit delay is given to FM modulated signal to synchronize operation.

• Then delayed FM modulated input signal is taken as multiplicand and *input2* is taken as multiplier.

•The output of PD will be of 16 bit,and thenby cropping the 8 most bits output is scaledand then takes as 8 bit output.

In the VHDL model, we use *Booth's Multiplication algorithm* [2] instead of simple signed arithmetic multiplier operation (denoted by ∗). Booth's multiplication algorithm for 8-bit multiplication is better approach which provides many advantages such as area consumption over Arithmetic multiplier. It only needs eight 8-bit adders which is much save in area consumption.

For this algorithm, the individual partial products determined from the multiplicand which may add to, subtract to, or may not change the final product at all based on the following rules:

• When in the multiplier's bit string first 1 is occurred, thepartial product is subtracted to themultiplicand.

• At the encounter of the first 0 when there was no previous 1 in a string of 0's in the multiplier, thepartial product is added to the multiplicand.

•If the bit of partial product is identical to the previous bit of multiplier,the partial product will not change

*2) Loop Filter:*

Loop filter will remove the high frequency component. Fig. 3 shows the block diagram of a first order loop filter used in the receiver system. In the VHDL model of loop filter, it is necessary to convert8 bit signalinto 12 bit (sign extension) and a multiplication by constant of 15/16.

Summary of operation:

• input*C* is multiplier's output of 8 bit. Output is *D1* of 12 bit. *D1* will be multiplied by 15/16 and then the product is summed back to *C*

• *dtemp*(12 bit) is internal signal which is the summing result of *C* and *D1*. *C* must be changed to (12 bit)before summation.

•*dtemp*will be assigned to *D1*. Then *dtemp x 15/16 = dtemp x (1 – 1/16) = dtemp – (dtemp x 1/16) = dtemp - E*

• *E =dtemp x 1/16*, in reality 1/16 multiply can be implemented by justshifting of binary data 4 bit to the right. So basically there is no need of multiplier to design of this block.

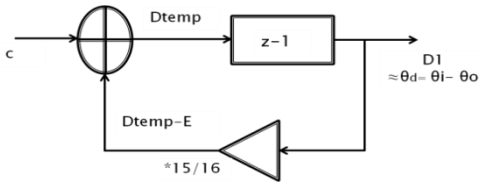



Fig. 3Loop filter

*3) Numerical Controlled Oscillator:*

Numerical Controlled Oscillator (NCO) receives the corrective error voltage from multiplier output, and then tries to shift the free-running frequency to the input signal frequency at the output of NCO, and thus make and keep the PLL in lock. The block diagram can be seen in Fig. 4 as follows,

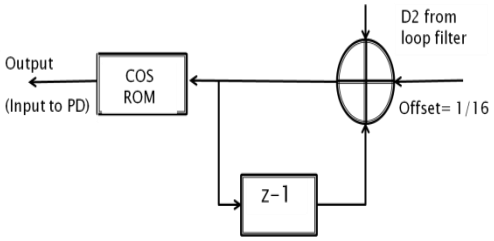


Fig. 4Numerical Controlled Oscillator (NCO)

Here it is assumed that the value of NCO free running frequency is 1 MHz and the system is worked on clock frequency of 16 MHz. With this assumption it is conclude thatin 1 cycle of free running frequencythere are 16 sampling points. When input is not applied to the system, NCO generates output frequency which is nothing but the free running frequency. Since 16 sampling points are taken in one cycle of free running frequency, so the offset must be chosen as 1/16. The output frequency is directly proportional to the input signal. The NCO can be understood as a simple integrator which builds up the input value and maps it into the predefined cosine ROM. All 1024 values were given (*file: cos.txt*) to define one cycle of cosine signal, but in reality no need to use all of these values. Since one particular cycle of any cosine data consist of four quarter, there is only need to map the first quarter with 257 values. For remaining quarters duplicated is taken from the first quarter, the fourth quarter is very similar to the first quarter; whereas the second and third quarter are opposite in sign with first quarter.

Summary of operation:

• receive the input from loop filter outputand then*offset* is added to it, here it is necessary to extent the signalinto 18 bitform 12 bit.

•the result of addition then given to modulo accumulator, here the 10 most bits of accumulated output is taken as ROM address.

• Address will be mapped to data values in ROM.

*4) FIR Filter:*

The very last task performed by the receiver system is shaping of signal. Herea 16 tap Finite Impulse Response (FIR) filter is used to perform as digital low pass filter. This filter is simply an average filter since it gives the output frequency equal to the average value of its input over the last *n*-tap samples, where *n* is number of tap used [3]. Here the configuration requires 16 constant coefficients, so for simplicity all of the coefficients are taken by assuming the same, 1/16. In reality multiplication of1/16 is just right shift operation of 4 bit. In this manner the use of multiplier is avoided.

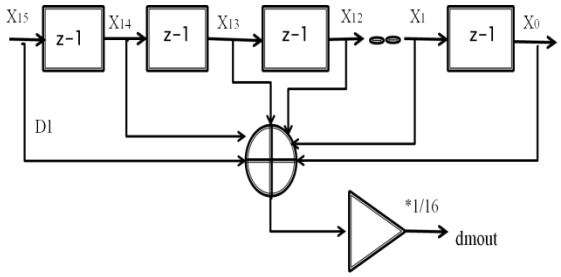
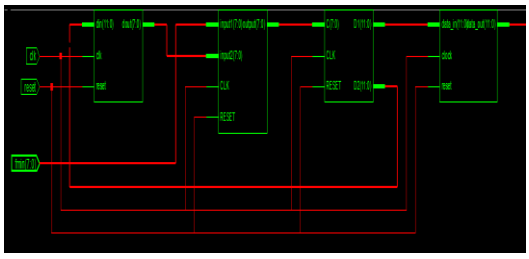



Fig. 5 FIR filter

The operation of the PLL can also be described in another manner. A PLL consists of a phase detector, which is in reality a 2 input multiplier circuit where the FM modulated input signal is mixedwith the NCO output signal. The mixed output produces the sum and difference frequencies($\omega_i \pm \omega o$) [1]. In lock stage of the loop, the NCO producesthe output signal similar to the input frequency which means difference frequency component ($\omega_i - \omega o$) is zero and the output of the phase comparator has only a DC component. The sum frequency component ($\omega_i + \omega o$) is removedby loop filter.Loop filter only passes the DC component which is then applied to the amplifier and then fed back to the NCO. Fig. 6 shows the schematic block diagram of system as shown at RTL schematic in synthesis report.Fig. 7 shows the functional block diagram of system.



. Fig. 6 Schematic block diagram

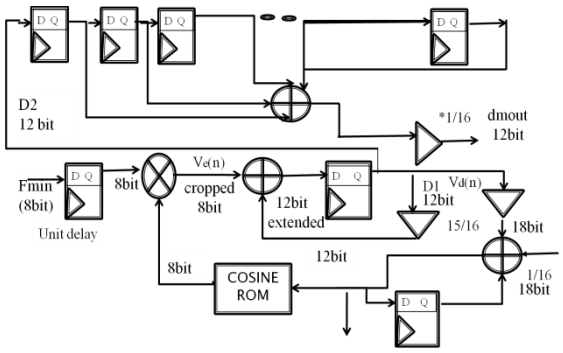



Fig. 7 Complete block diagram of all digital FM receivers

## IV. APPEALING POINT AND ORIGINALITY

The architecture used in this design has been explained in [1]. This architecture is good. Here the optimization of phase detector component is done to achieve better area constraint for system design. The modification of NCO component is also achieved.

Here the multiplication operationused in the phase detector componentis optimized. Arithmetic multiplier is replaced with some adders by the use of Booth's algorithm. This modification reduces the number of gate for this component from 689 gates decrease to 453 gates.

For NCO component, there is only need of 257x8- bit ROM rather than 1024x8-bit ROM since only one cycle of cosine wave is used to perform the operation as explained before. This modification optimized the use of ROM.

There was attempted to find another digital PLL architecture like one which was proposed in [5]. That proposed design was also good and easy to build, but it needs higher frequency of clock to drive the frequency divider (built by counter). Finally the implementationof design is done into FPGA, and then it is need to do real measurement. The result gives the correct demodulated output wave as expected.

## V. SIMULATION WAVEFORM

Fig.8 shows the simulation waveform for designed circuit subjected to cosine wave modulated data;the first row is Clock signal. The second row is reset signal. The third row shows the FM modulated waveform according to the sending data which can produce through matlab file. The fourth row shows the demodulated output. At the initial instant of time, the demodulated output is seem to have an overshoots since the phase synchronization is in convergence phase and then system is stable.

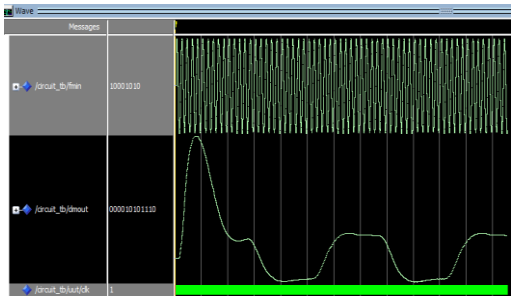


Fig.8Simulation waveform of the circuit, subjected to Cosine wave modulated input signal.

Fig.9 shows the simulation waveform for phase detector circuit where one input is taken as FM modulated signal and other is from output of NCO. The first row is $F_{min}$. The second row is output from NCO. The third row shows the mixing of two signals.

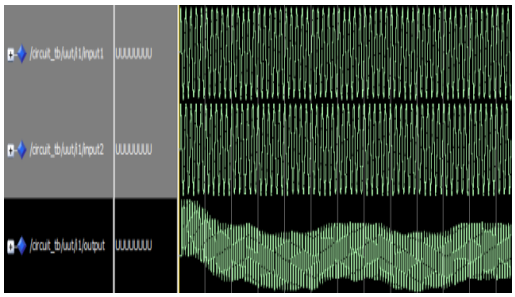


Fig.9 Simulation waveform for phase detector

Fig.10 shows the simulation waveform for loop filter through which mixed signal is passed.Loop filter removes the high frequency component from mixed signal. The first row is mixed signal. The second row and the third rowshow the filtered output.

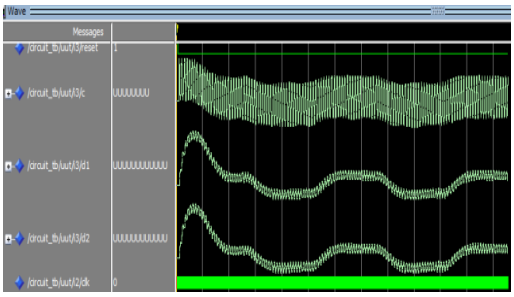


Fig.10 Simulation waveform for loop filter

Fig.11 shows the simulation waveform for NCO.NCO takes the error signal from loop filter and tries to generate the output frequency similar to the input frequency. The first row is error signal from loop filter. The second row shows the output.

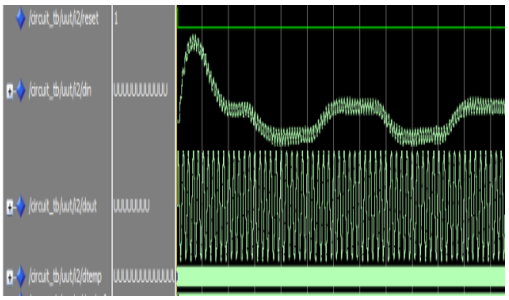


Fig.11 Simulation waveform for NCO

Fig.12 shows the simulation waveform for FIR.FIR takes the signal from loop filter and produces the output frequency, taken as average of the input frequency for n-tap. The first row shows the applied input taken from loop filter. The second row shows the demodulated output.

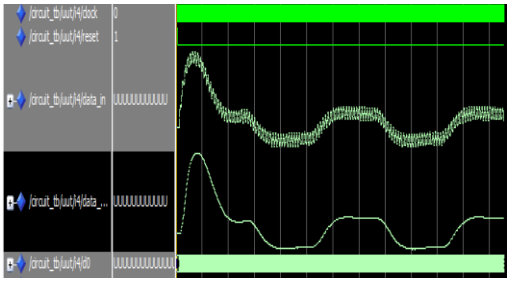


Fig.12 Simulation waveform for FIR

Fig.13 shows the simulation waveform for whole system with internally generated signal.

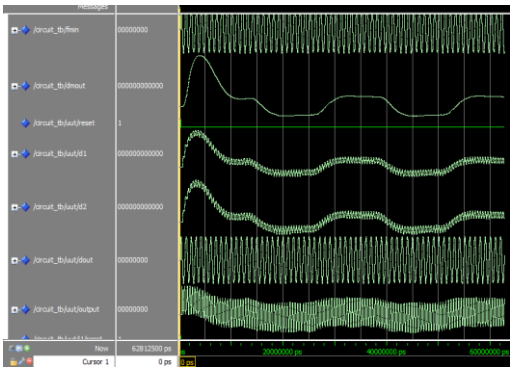


Fig. 13 Simulation waveform for system

## VI. FPGA IMPLEMENTATION

Here the implementationof the all digital FM receiver circuit designed into FPGA. Here we are using Virtex2 device from Xilinx with XC2S50 technology and PQ208 package.

Captured data is in signal form of 12-bit binary number as shown in Fig. 14. It can adjust how many samples needed to be captured; here it is captured 1024 samples output data, then it isplotted by ISE project navigator to obtain the actual demodulated signal view as shown in Fig.15.

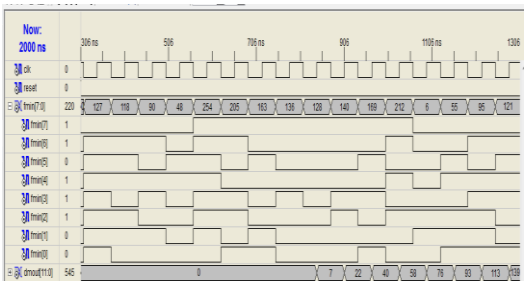


Fig. 14 Captured data and waveform of the input in Xilinx 8.3i.

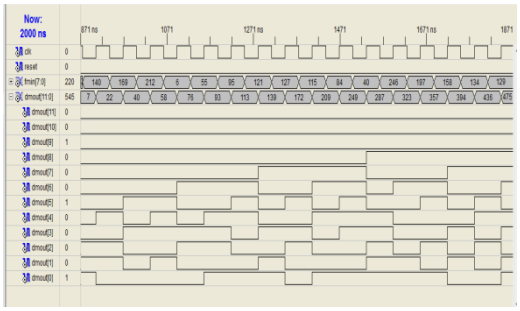


Fig. 15 Captured data and waveform of the input in Xilinx 8.3i.

## VII. CONCLUSION

PLL is widely used in wireless communicationsystems as well as telecommunication system.FPGA implementation ensures easy and computercontrol over the system. This paper has discussed thePLL basic structure and designed a PLL that can beused efficiently for FM demodulator signal generator purpose.

Xilinx is used for designing the schematic diagramusing the RTL logic. Modelsim 6.5b is used forobserving the timing diagram of the designated PLLwith synchronous reset. From the synthesis report, ithas been also observed that how many adder,flip flops, registers, comparators and multipliers areneeded to design.

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