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Simulation and Comparison of Multi Level Inverter Using H-Bridge Inverter Topology for Induction Motor Drive

Jayesh N. Patel[1],Sanket D. Patel[2],Krishna Vakharia[3]

[1]*P.G student,Electrical Engineering Department, SCET,Surat*
[2]*P.G student,Electrical Engineering Department, SCET,Surat*
[3]*Assistant Professor,Electrical Engineering Department, SCET,Surat,*

Abstract *— This paper presents a simulation of three phase cascaded H-bridge (CHB) multilevel inverter for induction motor drive system. Level-shifted (In phase disposition) multicarrier modulation technique is used to achieve minimum total harmonics distortion (THD) in the output voltage of multilevel inverters. A Comparison and analysis of the output voltage harmonics of 5-level cascaded H-bridge inverter, 3-level cascaded H-bridge inverter & 2-level inverter is also presented in this paper. The five-level inverter configuration supplying a 5hp four pole induction motor drive is tested in MATLAB (Simulink). From the result it is observed that when level is increased THD improves.*

Keywords*- Cascaded H-bridge inverter, MLI, IPD, SPWM, THD*

I. INTRODUCTION

For high power applications, voltages and currents must be pushed up. Hence, maximum ratings of power semiconductors become a real handicap. Multilevel Inverter can overcome this limitation.

Present day mostly Induction motor drives with voltage source inverters are used. Also the voltage waveforms of traditional two level inverter fed Induction motor shows that the voltage across the motor contains not only the required fundamental sinusoidal components, but also pulses of voltage with ripple voltage. The rate of change of voltage with respect to time i.e. dv/dt is very high. Although high voltage ratings of the power semiconductor devices are available, it is not advisable to retain the 2-level configuration for higher voltage motors. This is because high voltage pulses will be applied to the motor causing dv/dt stresses. Today, medium voltage induction motors rated at the MW level are generally controlled using three level inverters. The 3-Level inverter, on the other hand, allows the motor voltage to go up in steps. This reduces the dv/dt stress for the same DC bus voltage Vdc. Inverters of higher number of levels such as 5 and 7 level can also be constructed. However, the circuit assembly becomes very complex and issues such as keeping all the sections of the dc bus voltage equal have to be addressed [1]. Multilevel inverters include an array of power semiconductors and capacitor voltage sources, the output of which generate voltages with stepped waveforms. Fig. 1 shows a schematic diagram of one phase leg of inverters with different numbers of levels, for which the power semiconductors is represented by an ideal switch with several positions. A two-level inverter generates an output voltage with two values

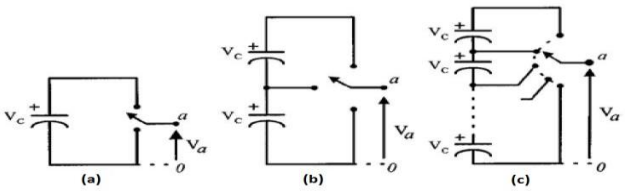

Fig.1 One phase leg of an inverter with (a) two levels, (b) three levels, and (c) n levels

(levels) with respect to the negative terminal of the capacitor [see Fig. 1(a)], while the three-level inverter generates three voltages, and so on.

Power dissipation is one of the most important issues in high power applications. By increasing the number of levels in the inverter, the output voltages have more steps generating a staircase waveform, which has a reduced harmonic distortion. However, a high number of levels increases the control complexity and introduces voltage imbalance problems. Three different topologies have been proposed for multilevel inverters: diode-clamped (neutral-clamped) [2]; capacitor-clamped (flying capacitors) [3]; and cascaded multicell with separate dc sources [3]. In addition, several modulation and control strategies have been developed for multilevel inverters including the following: Level-shifted multicarrier modulation (PWM), Phase-shifted multicarrier modulation (PWM), multilevel selective harmonic elimination, and space-vector modulation (SVM).

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II. BASIC OPERATING PRINCIPLE OF CASCADED H-BRIDGE MULTILEVEL INVERTERS (CHB-MLI)

The single phase 5-level Cascaded Multilevel Inverter consists of simple two H-bridge modules, whose AC terminals are connected in series to obtain the output waveforms Fig.2. shows the power circuit for a five level inverter with two cascaded cells. Through different combinations of the four switches of each cell, the inverter can generate FIVE different voltage outputs, +2Vdc, +Vdc, 0, -Vdc, -2Vdc. The number of voltage levels in a CHB inverter can be found from z = (2H+1) where H= is the number of H-Bridge cells per phase leg. The voltage level m is always an odd number for the CHB inverter. The total number of active switches (IGBT's) used in the CHB inverters can be calculated by Nsw = 3*2(z-1) =6(4) =24 switches (for three phase).where Nsw=number of switch [3],[6].

The resulting AC output voltage is synthesized by the addition of the voltages generated by different H-bridge cells. Each single phase H-bridge generates three voltage levels as +Vdc, 0, - Vdc by connecting the DC source to the AC output by different combinations of four switches, S11, S12, S13, and S14 as seen in Fig 1(c). The CHB-MLI that is shown in Fig. 2 utilizes two separate DC sources per phase and generates an output voltage with five levels. To obtain +Vdc, S11 and S14 switches are turned on, whereas -Vdc level can be obtained by turning on the S12 and S13. The output voltage will be zero by turning on S11 and S12 switches or S13 and S14 switches. If n is assumed as the number of modules connected in series, m is the number of output levels in each phase as given by z=2n+1. The switching states of a CHB-MLI (sw) can be determined by using Eq. sw= 3z [3],[7].

Considering the simplicity of the circuit and advantages, Cascaded H-bridge topology is chosen for the presented work. Table I shows the switching strategies used for single phase five level CHB-MLI.

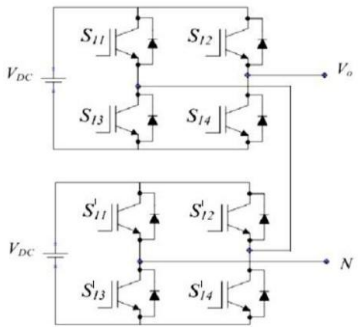

Fig. 2 Single phase five level CHB-MLI

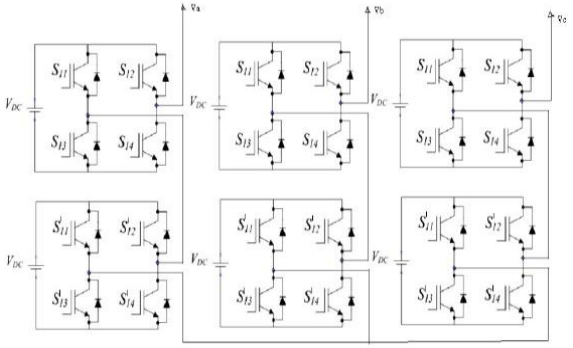

Fig.3 Three-phase five-level topology of Cascaded H-bridge multilevel inverter

The three phase 5-level cascaded H-bridge inverter topology is realized using MATLAB/SIMULINK. The use of CHB-MLI reduces the total harmonic distortion (THD) in the output current waveform by increase in the number of levels of the output voltage. We can further increase the no. of levels of the inverter to reduce the harmonics. Fig 3 shows the three phase connection of a Cascaded H-Bridge multilevel inverter.

Table 1.Switching Strategies

Switching State				V_{H1}	V_{H2}	Output Voltage V_{AN}
S_{11}	S_{31}	S_{12}	S_{32}			
1	0	1	0	V	V	2V
1	0	1	1	V	0	V
1	0	0	0	V	0	
1	1	1	0	0	V	
0	0	1	0	0	V	
0	0	0	0	0	0	0
0	0	1	1	0	0	
1	1	0	0	0	0	
1	1	1	1	0	0	
1	0	0	1	V	-V	
0	1	1	0	-V	V	
0	1	1	1	-V	0	-V
0	1	0	0	-V	0	
1	1	0	1	0	-V	
0	0	0	1	0	-V	
0	1	0	1	-V	-V	-2V

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III. CONTROL TECHNIQUES

SPWM technique is one of the most popular modulation techniques among the others applied in power switching inverters. In SPWM control, a sinusoidal reference voltage waveform is compared with a triangular carrier waveform to generate gate signals for the switches of inverter. The fundamental frequency SPWM control method is proposed to minimize the switching losses. The multi-carrier SPWM control methods increase the performance of multilevel inverters and are classified according to vertical or horizontal arrangements of carrier signal. The vertical carrier distribution techniques are defined as Phase Dissipation (PD), Phase Opposition Dissipation (POD), and Alternative Phase Opposition Dissipation (APOD) as shown in Fig 4[4],[5].

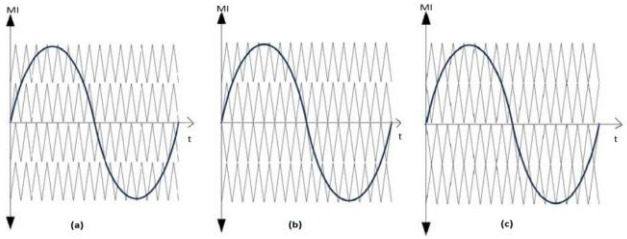

Fig 4 Multi-carrier SPWM control strategies: (a) IPD, (b) POD, (c) APOD

IV. SIMULATION AND RESULTS

In this section MATLAB SIMULATION of five level inverter topology with 5HP induction motor drive is carried out which is shown in Fig 5.

PARAMETER:
Supply frequency: 50 Hz
Input voltage: 120 v
Numbers of Pole: 4
Stator resistance: 1.405Ω
Stator inductor: 0.005839H

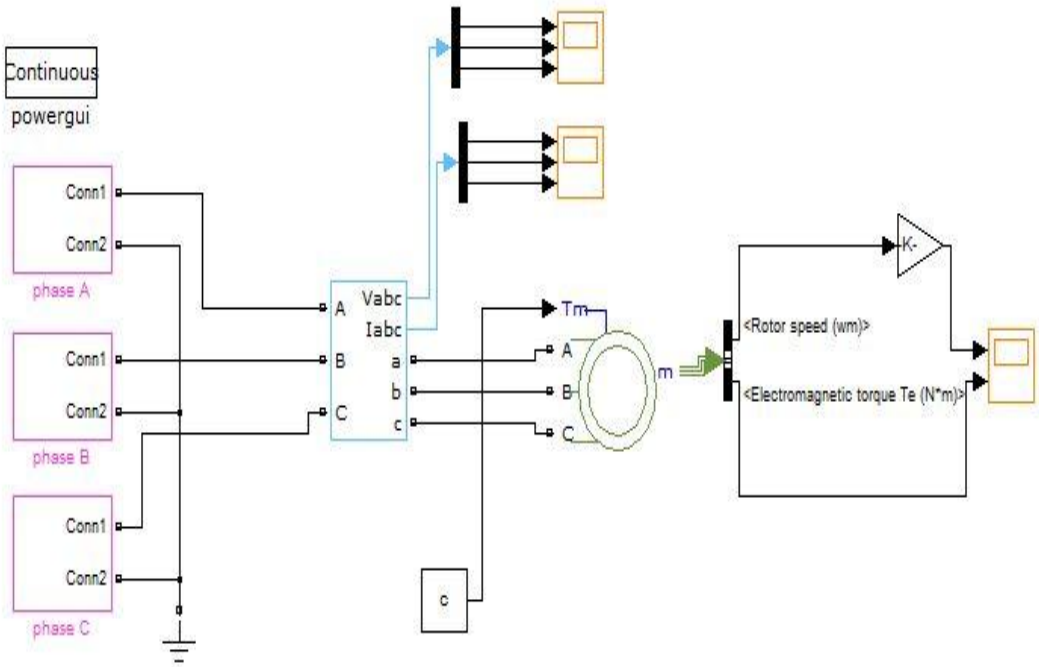

Fig.5 Simulink model of cascaded H-Bridge five level inverter

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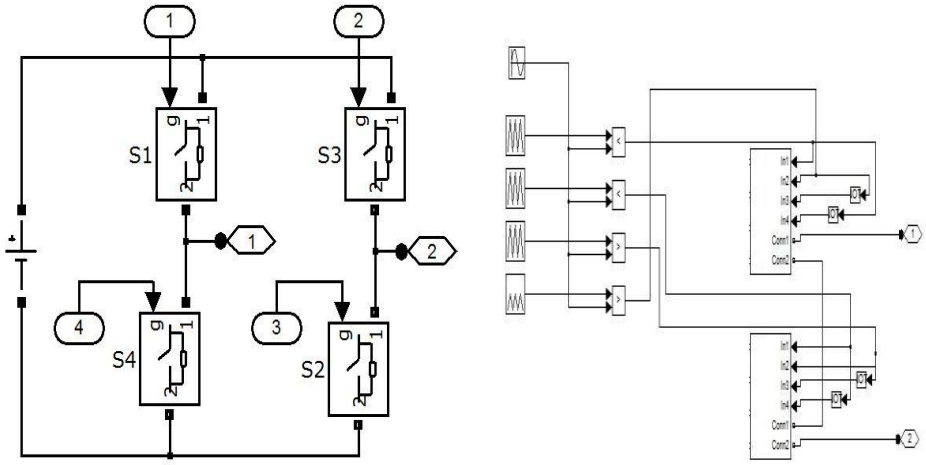

(a) *(b)*

Fig.6 Subsystem of (a)H-Bridge and (b)control technology

Level shifted (IPD) multicarrier technique is used to control the inverter output. In this IPD, triangular are compared with sine wave to generate this gate pulses. In this, frequency of triangular (carrier) wave is 1KHZ and frequency of sine wave is 50Hz taken.

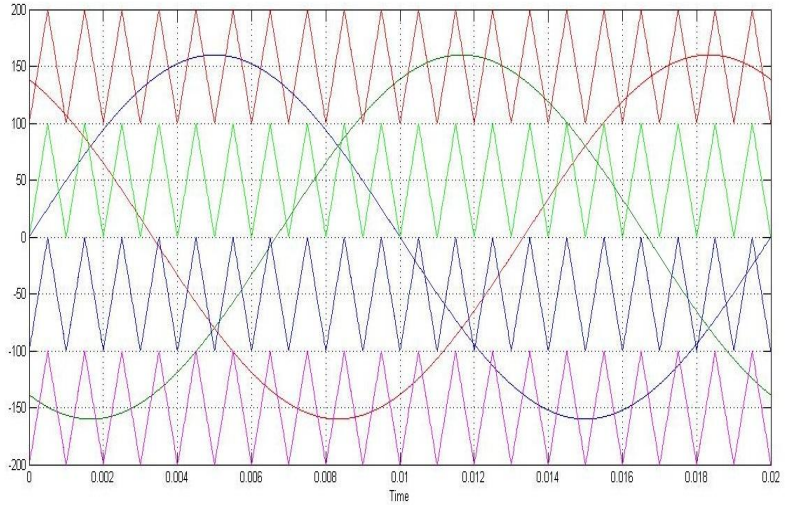

Fig.7 Simulation model for generation of pulses for one cycle (Ma=0.8, fm =50Hz, fcr =1 kHz)

The output of five level inverter is shown in Fig 8, Fig 9, Fig 10 and Fig 11.

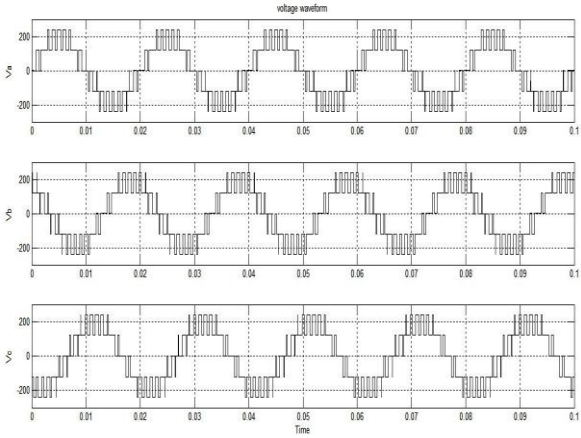

Fig.8 Phase voltage of five level inverter

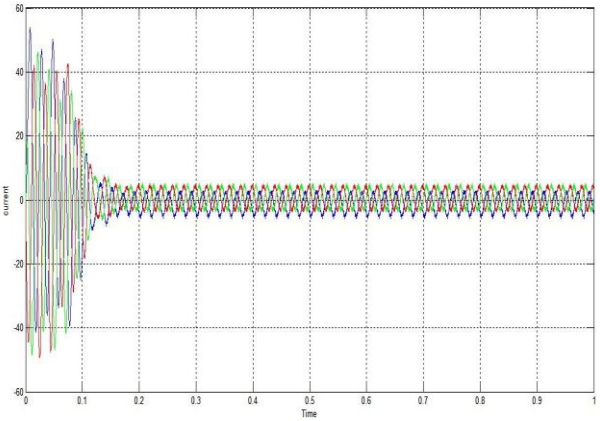

Fig.9 Output current of five level inverter

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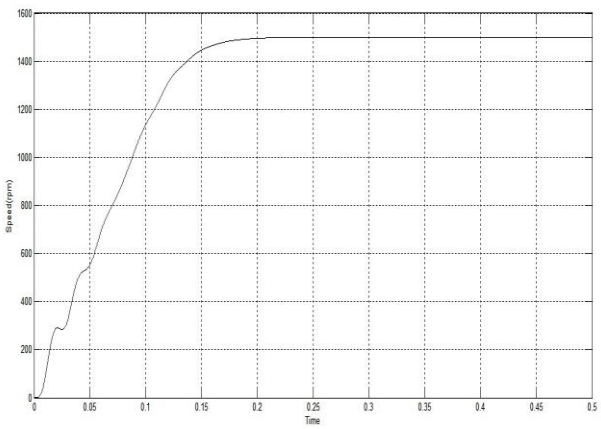

Fig.10 waveform of speed

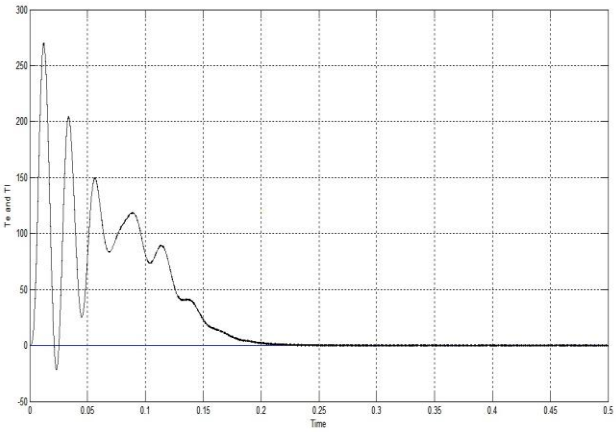

Fig.11 Waveform of Te and Tl

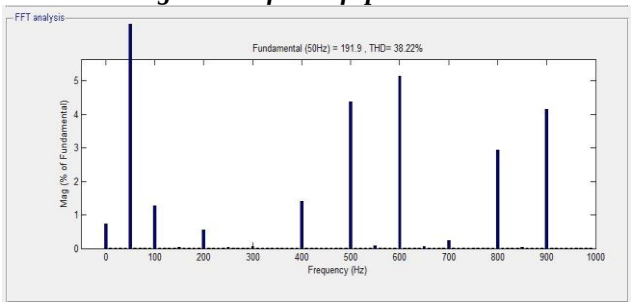

Fig.12 Voltage THD

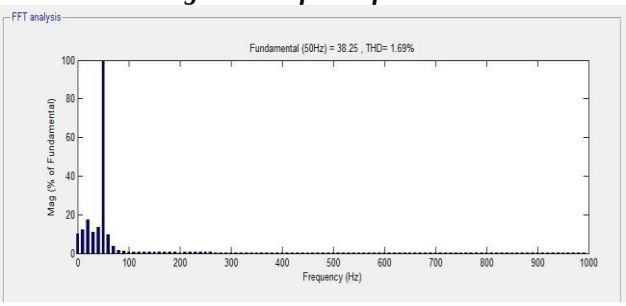

Fig.13 Current THD

From the result, voltage THD is 38.22% and current THD is 1.69% obtain .It is shown in Fig 12 and Fig 13 respectively. Table II shows the comparison of voltage THD for different multilevel inverter.

Table 2.comparison of Multilevel Inverter

LEVEL	VOLTAGE THD%
TWO-LEVEL	71.31
THREE-LEVEL	54.74
FIVE-LEVEL	38.22

V. CONCLUSIONS

Multilevel topology and SPWM both are used to improve THD. Multilevel topology is preferred for induction motor type drives. The simulation of cascaded H-Bridge five-level inverter was done by using MATLAB. The various voltage, current, speed and torque waveforms are carried out. From the results it can be concluded that when number of voltage level is increases THD is decreased.

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