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HIGH POWER FACTOR RECTIFIER BASED ON BUCK PFC CONVERTER OPERATING IN CRITICAL CONTINUOUS CONDUCTION MODE

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Abstract — *An improved buck power factor correction (PFC) converter topology is proposed in this paper. By adding an auxiliary switch and two diodes, the dead zones in ac input current of traditional buck PFC converter can be eliminated. An improved constant ON-time control is proposed and utilized in this improved buck PFC converter to force it that operates in critical conduction mode (CRM).With optimal control parameters, nearly unit power factor can be achieved and the input current harmonics can meet the IEC61000-3-2 class C standard within the universal input voltage range. Moreover, the efficiency of the proposed converter is not deteriorated compared to the conventional buck converter. Detailed theoretical analysis and optimal design considerations for the proposed converter are presented and verified by a 100-W lab made prototype*.

Index Terms—*AC–DC, buck power factor correction (PFC), class C, high efficiency, high power factor (PF).*

I. INTRODUCTION

Nowadays, most ac/dc power converters are forced to reduce the harmonic current to meet the IEC61000-3-2 limits [1]. Some special power products such as lighting equipments should meet the stricter IEC61000-3-2 class C limits. Power factor correction (PFC) is a good method for providing an almost sinusoidal input current. The boost converter is the most popular topology for PFC applications due to its inherent current shaping ability [2]–[4]. However, with universal input, usually a 400 Vdc output voltage is required for the boost PFC. The boost PFC cannot achieve high efficiency at low line input because it works with large duty cycle in order to get high-voltage conversion gain. Therefore, it is hard to increase the power density of boost PFC converter due to the thermal concern at low line input.

THE Sepic converter [5], [6] and quadratic buck-boost [7], [8] can achieve high power factor (PF) and reduce the output voltage stress. But the voltage stress of switch in these two topologies is much higher than that in the boost PFC converter that reduces the efficiency and increases the cost.

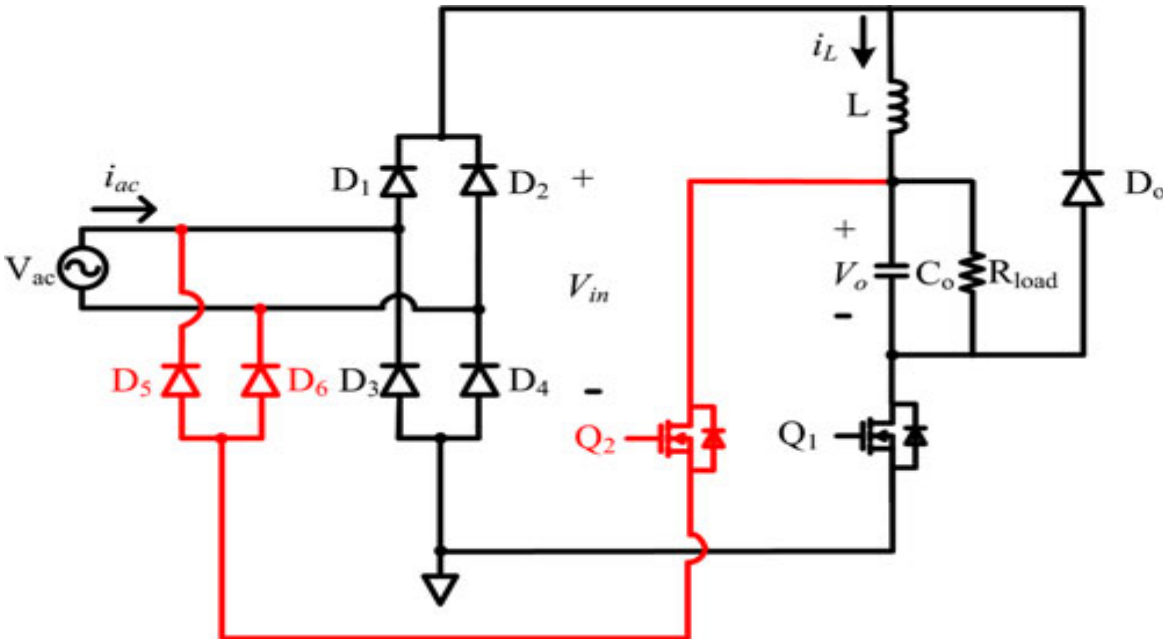


Fig.1. Proposed improved buck PFC converter.

The buck PFC converter has some attractive merits. First, the output voltage of buck converter is always regulated lower than the boost converter. Second, the voltage across the main switch of the buck converter is almost clamped to the input

voltage. Therefore, the buck PFC converter can achieve relatively high efficiency within the universal input voltage range and it has drawn more and more attention in the past years [9]–[25]. However, if the buck converter operates in hard switching mode, the switching loss especially at high input will be large, which deteriorates the merit of the buck converter [9]–[18]. The buck dc–dc converter operating in critical continuous conduction mode(CRM) can eliminate the reverse recovery loss in diode and achieve zero voltage switching (ZVS) for the switch [19], [20]. The constant ON-time (COT) control for CRM buck PFC converter is introduced in [21]–[23]. With COT control, the peak current in the switch is almost proportional to the input voltage, and then high PF can be achieved. However, it is still difficult to pass the IEC61000-3-2 criteria due to the dead zones in the input current that appears when the input voltage is lower than output *Vo* . An improved COT control is introduced in [24]. This improved COT control can help improve the PF of the conventional buck PFC converter. However, this improved COT control method needs careful parameters design. Even so, it is still hard to meet the limits imposed by IEC61000-3-2 class C Criteria at the low line input voltage. In this paper, an improved buck PFC converter is proposed, as shown in Fig. 1. Compared with the conventional buck PFC converter, an auxiliary switch and two diodes are added in the improved buck PFC converter. The proposed converter has two different operation modes in a line period. When the input voltage is higher than the output voltage, the proposed converter operates in buck mode, which is same as the conventional buck converter. When the input voltage is lower than the output voltage, the proposed converter operates in buck-boost mode. Hence, there are no dead zones in the input current. The PF can be improved obviously, and then the proposed converter can meet IEC61000-3-2 class C criteria easily with enough margins. Moreover, the efficiency of the proposed converter is very close to the conventional buck converter. The proposed converter is suitable for the PFC front stage of ac/dc converter and LED drivers with the power range from 60 to 300 W.

II. PRINCIPLE OF OPERATION

In this section, the proposed converter operates in CRM will be analyzed in detail. To simplify the analysis, the transitions between the switches and the output diode *Do* are omitted. After that, there still exist eight operation stages in a line period. Fig. 2 shows the equivalent circuits of the stages.

A. Positive Buck-Boost Operation Mode

When the input voltage *V*ac is in positive half cycle and the magnitude of *V*ac is smaller than *Vo*, the proposed converter operates in buck-boost mode. During this mode, switch *Q*1 keeps OFF and switch*Q*2 keeps switching. There are two stages when the proposed converter operates under this mode:

Stage 1: When switch *Q*2 is ON, the proposed converter operates in stage 1. The equivalent circuit of this stage is shown in Fig. 2(a). The inductor *L* is charged by *V*ac through *D*1 and *D*6, and *iL* increases during this stage.

Stage 2: When switch *Q*2 is OFF, the proposed converter operates in stage 2. The equivalent circuit of this stage is shown in Fig. 2(b). The inductor *L* is discharged by *Vo* through *Do*, and *iL* decreases during this stage.

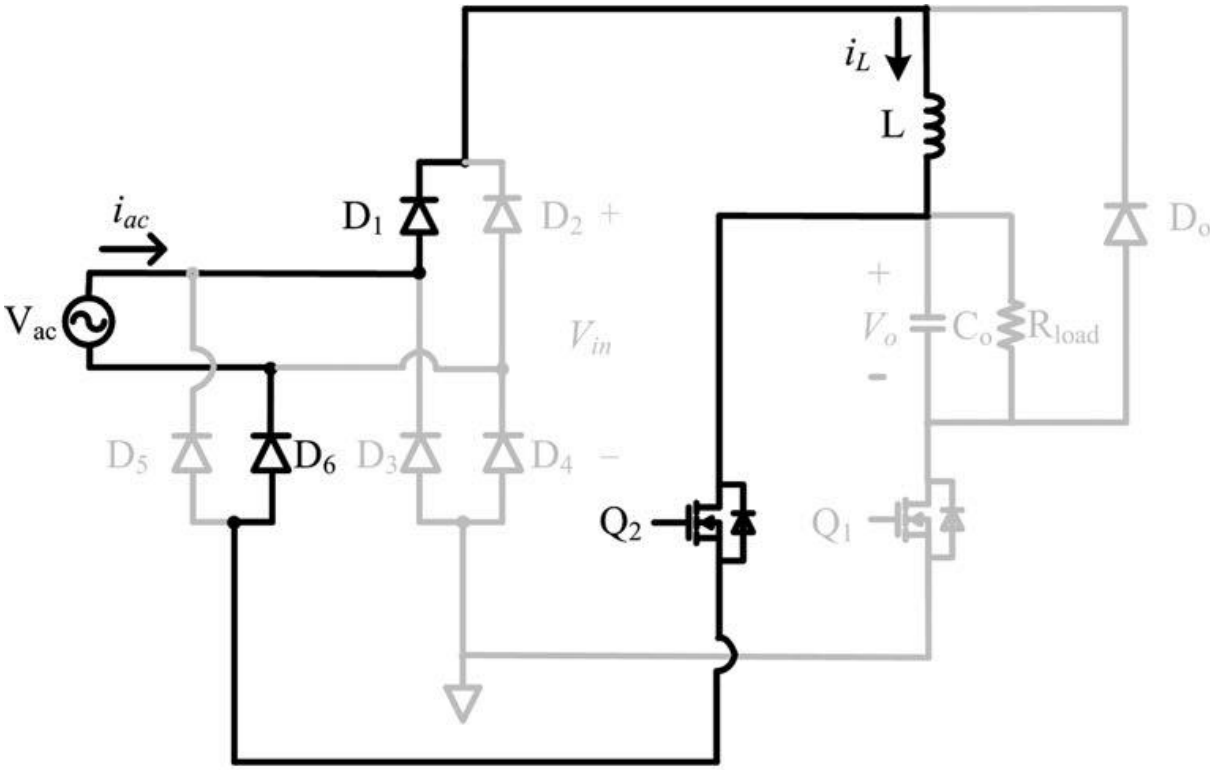
B. Positive Buck Operation Mode

When the input voltage *V*ac is in positive half cycle and the magnitude is larger than *Vo* , the proposed converter operates in buck mode. During this mode, switch *Q*2 keeps OFF and switch *Q*1 keeps switching. There are two stages when the proposed converter operates under this mode:

Stage 3: When switch *Q*1 is ON, the proposed converter operates in stage 3. The equivalent circuit of this stage is shown in Fig. 2(c). The inductor *L* is charged by *V*ac−*Vo* through *D*1 and *D*4, and *iL* increases during this stage.

Stage 4: When switch *Q*1 is OFF, the proposed converter operates in stage 4. The equivalent circuit of this stage is same as that of stage 2, as shown in Fig. 2(b). The inductor *L* is discharged by *Vo* through *Do*, and *iL* decreases during this stage.

When the input voltage *V*ac is in negative half cycle, there also exist two operation modes of negative buck-boost operation mode and negative buck operation mode of the proposed converter. The negative operation processes can also be separated into four operation stages defined as stages 5–8, and the equivalent circuits include Fig. 2(b), (d), and (e). The negative half cycle operation processes of the proposed converter are similar to those of the positive half cycle. For simplicity, the negative operation processes are not depicted in detail here.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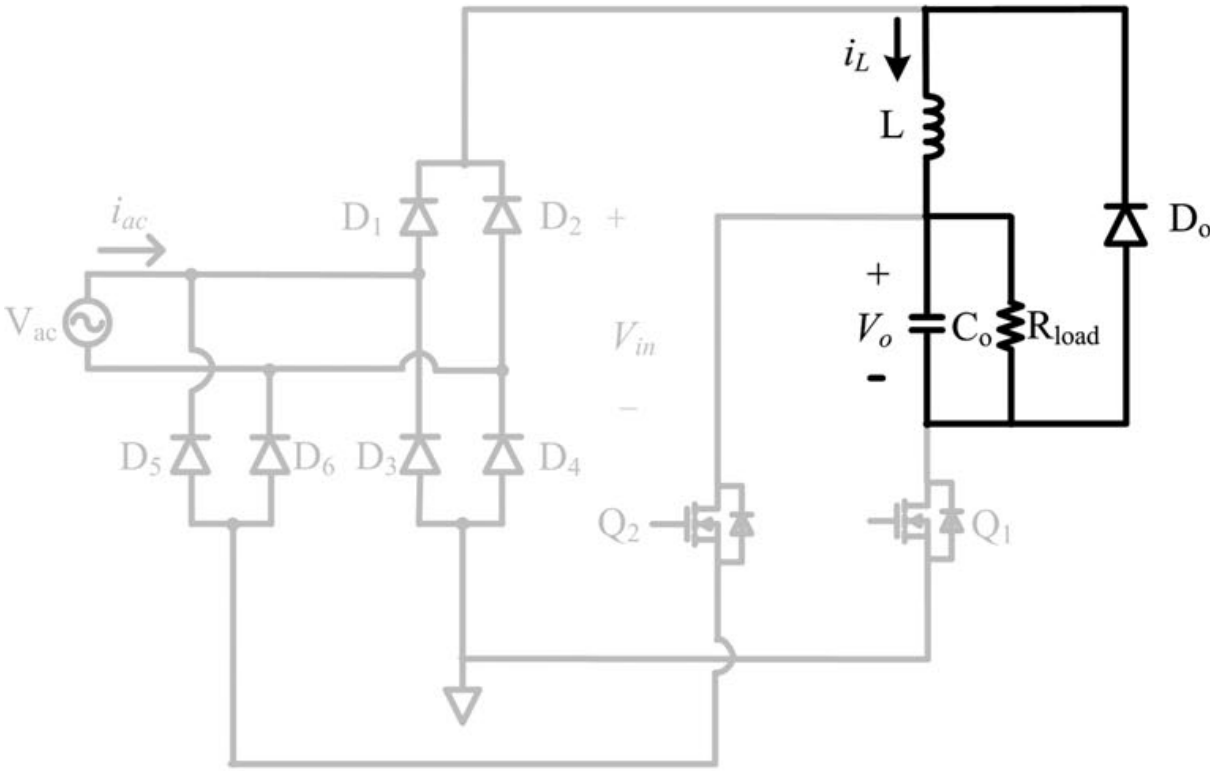
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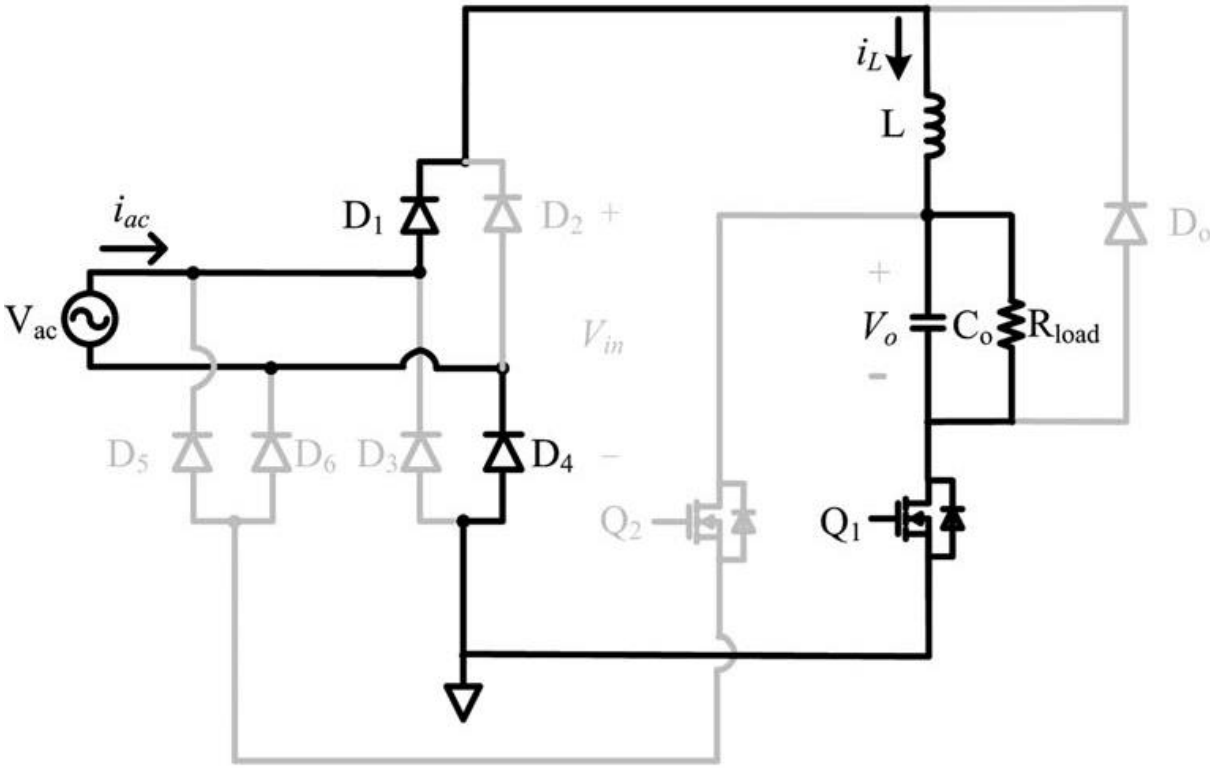
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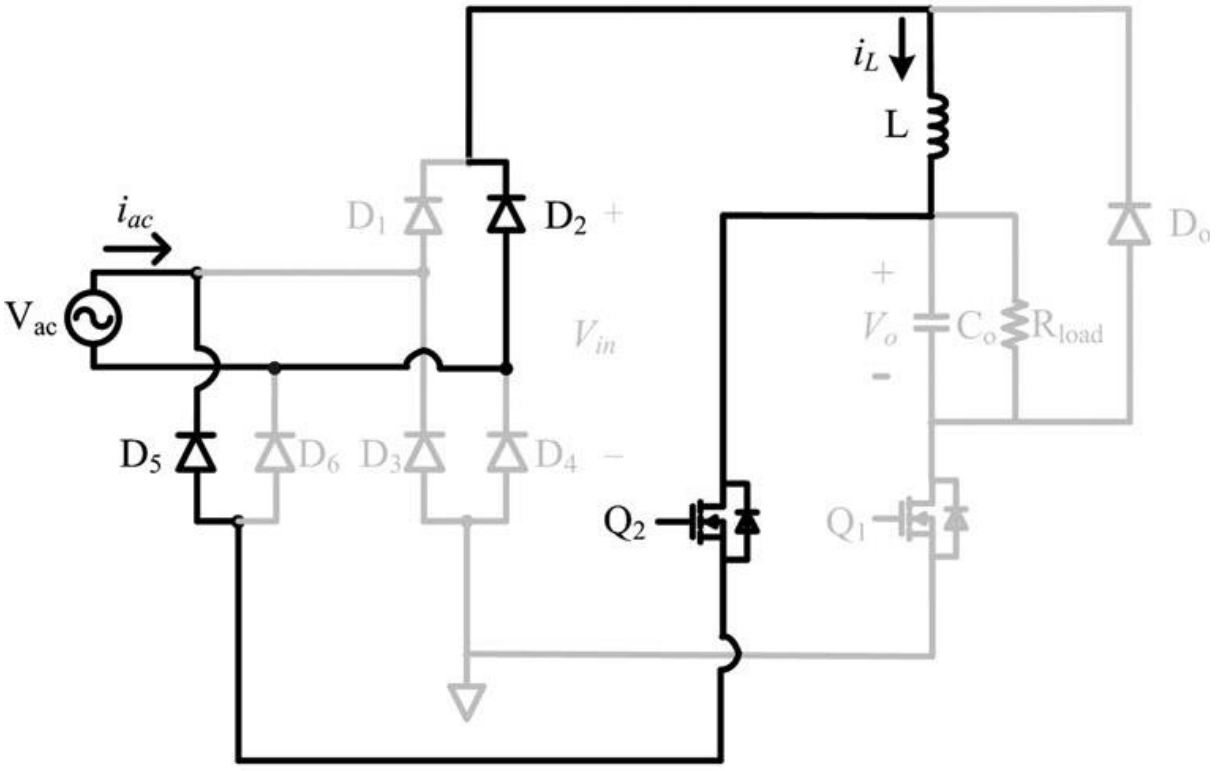
(c)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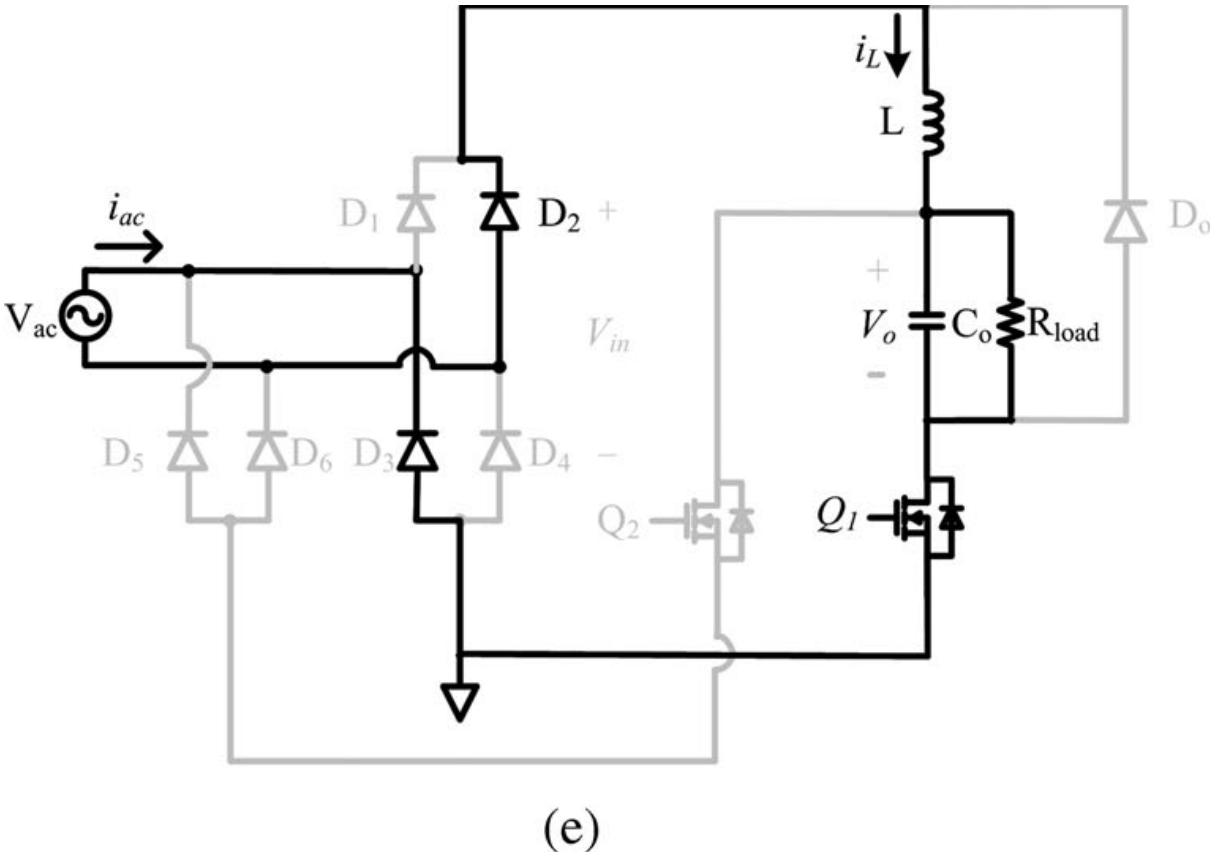
(d)



(e)

Fig.2. Equivalent circuits of the proposed converter in eight stages.

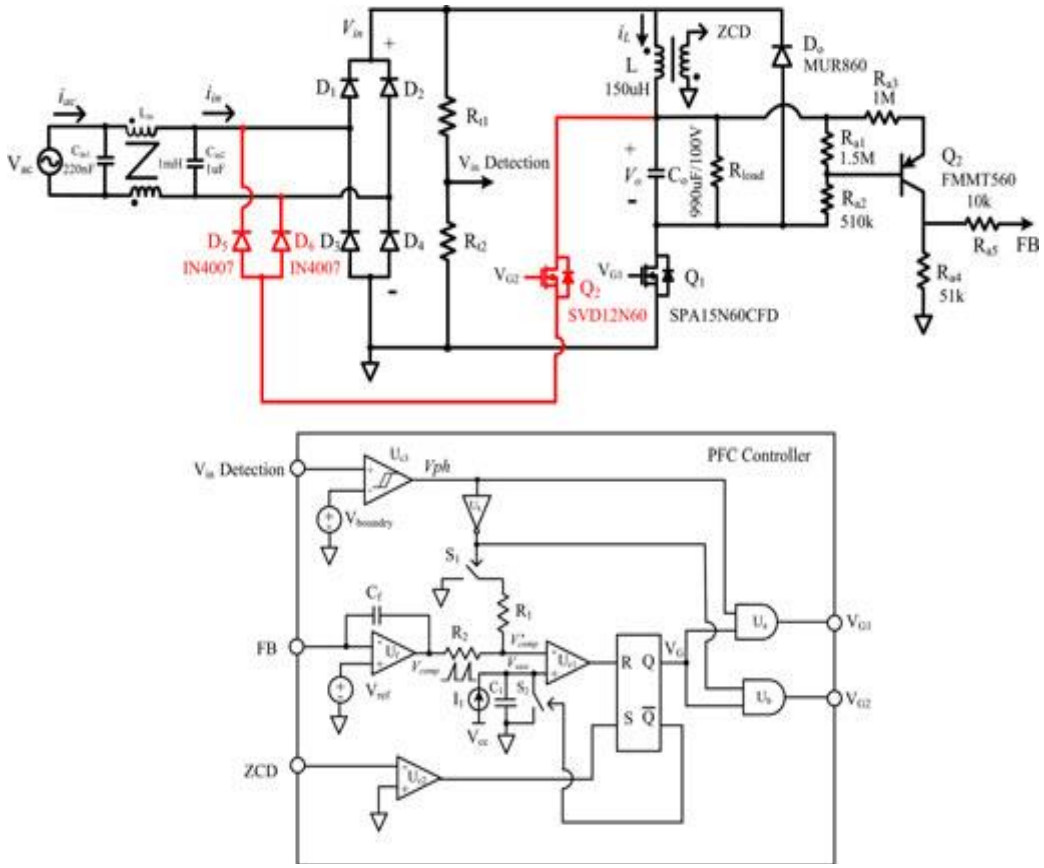


Fig.3. Schematic of the proposed buck PFC converter with an improved COT control.

An improved COT control is applied for the proposed buck PFC converter to force it that operates in CRM, as shown in Fig. 3. The output voltage is detected with a level-shift circuit formed by a high-voltage transistor $Q2$ and the resistors $Ra1 \sim Ra4$. Some key waveforms are shown in Fig. 4.

As shown in Fig. 3, the control signal Vph used to control the converter either in buck mode or buck-boost mode is achieved by comparing the detected Vin signal V _in with a voltage reference Vboundry . Usually, Vboundry is set to reflect the output voltage Vo with the same ratio as that V _in reflects Vin . Vph is high logic when V _in is higher than Vboundry and is low logic when V _in is lower than Vboundry . The detected output signal VFB is sent to the negative input of the error amplifier Uf . The error between VFB and the set reference Vref is amplified by the compensation networks Cf and an amplified error signal Vcomp is achieved. The dc voltage signal Vc_omp applied to control the conduction period TON is achieved from Vcomp through a control networks formed by resistors $R1$ and $R2$ and switch $S1$. Switch $S1$ is controlled by the control signal Vph. The proposed converter operates in buck mode when $S1$ is OFF and operates in buckboost mode when S1 is ON. Vc_omp is a step function controlled by Vph, as shown in (1)

$$V\text{c\_omp} = \begin{cases} V\text{comp} & V\text{in} > Vo \\ k \cdot V\text{comp} & V\text{in} \le Vo \end{cases} \qquad (1)$$

where k is a coefficient equal to $R1$ /($R1$+$R2$). Similar to the conventional COT control, a constant current source $I1$, capacitor $C1$, and switch $S2$ are used to generate a sawtooth waveform Vsaw. When Vsaw reaches Vc_omp, the output of comparator $Uc1$ jumps from low level to high level. This level transition resets the driving signal from high level to low level.

The zero-crossing point of the inductor current iL is detected by the auxiliary winding of the inductor L. This inductor current zero-crossing detection signal VZCD can be applied in both buck and buck-boost modes. When the inductor current iL falls to zero, the output voltage auxiliary winding VZCD starts to fall. Once VZCD falls to zero, the output of comparator $Uc2$ jumps from low level to high level. This level transition sets the driving signal from low level to high level.

According to the aforementioned analysis, the rising slope of Vsaw is constant due to the constant current source $I1$ charging during the whole line period. Therefore, the ON-time (TON) of the switches is determined by V _comp proportionally. Smaller value of k leads to smaller TON and smaller peak values of iL when the proposed converter is operating in buck-boost mode.

As shown in Figs. 3 and 4, the driving signals $VG1$ and $VG2$ are controlled by Vph for the different operation modes alternately. Different coefficient k results in the different PF correction performance and the overall efficiency.

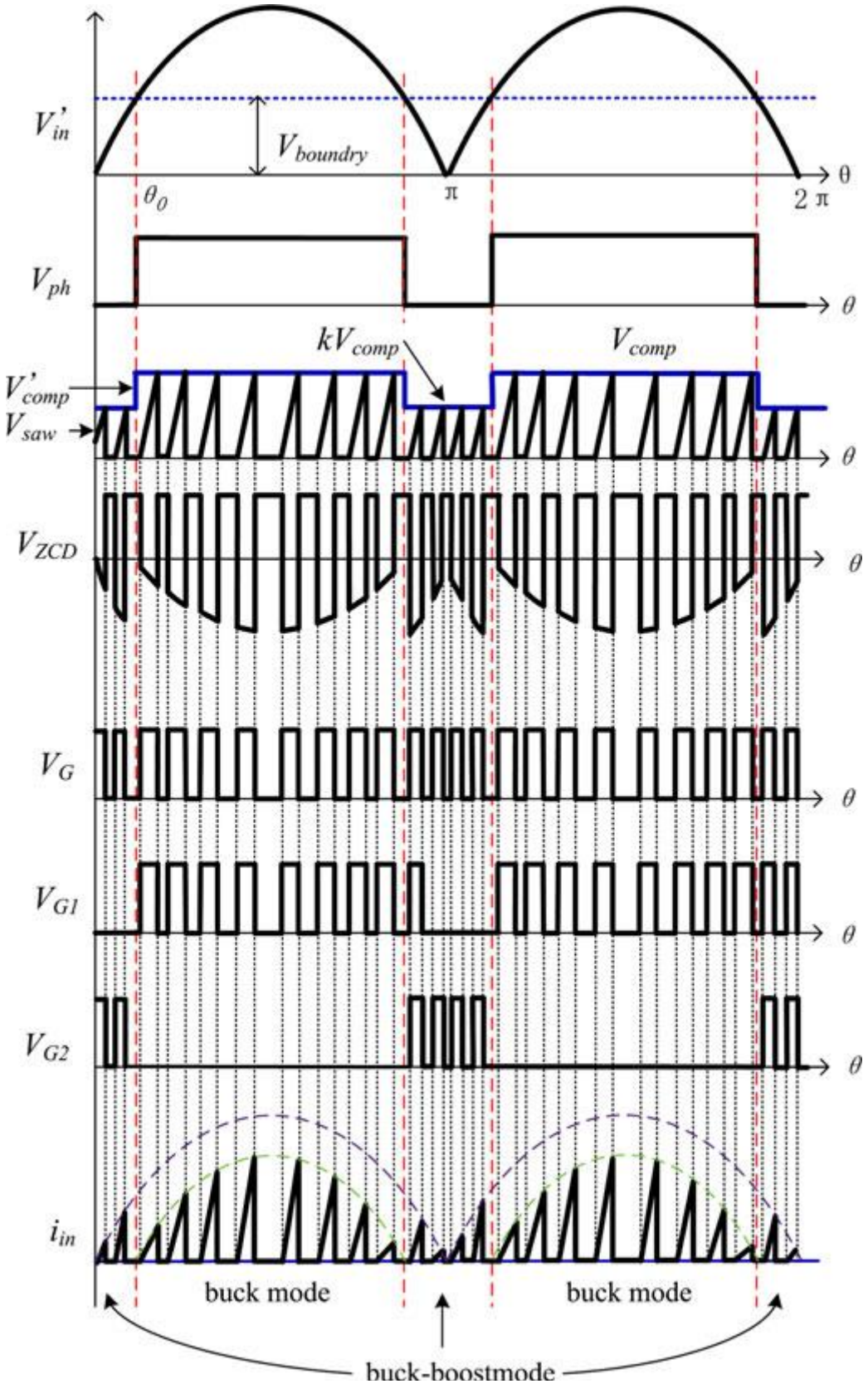


Fig.4. Key waveforms in the improved COT control diagram.

III. EXPERIMENTAL RESULTS

A 100-W lab-made prototype with universal input and 80 Vdc output is built up to verify the proposed buck PFC converter. The schematic of the prototype is shown in Fig. 3 with the key parameters. The improved COT control shown in Fig. 3 is applied for the prototype and the control circuit is realized with discrete components. The coefficient *k* is set

to 1/4 by the network of *R*1 and *R*2. For comparison, a 100 W prototype of the traditional buck PFC converter is also built up.

Measured input voltage and input current waveforms of the conventional buck PFC converter with full load at 90 Vac input are shown in Fig. 10. Measured input voltage and input current waveforms of the proposed buck PFC converter with full load at 90 Vac input are shown in Fig.5.

Measured PF at different input voltage with full load of the buck PFC converter and the proposed converter is shown in Fig.6. Obviously, the proposed converter can improve the PF greatly especially at low line voltage.

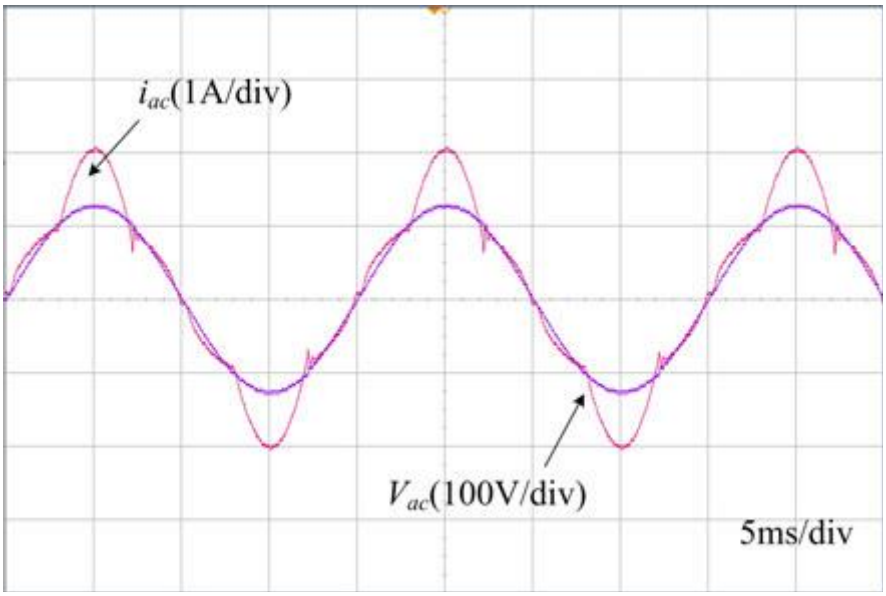


Fig.5. Measured input voltage and input current waveforms of the proposed converter (90 Vac and full load).

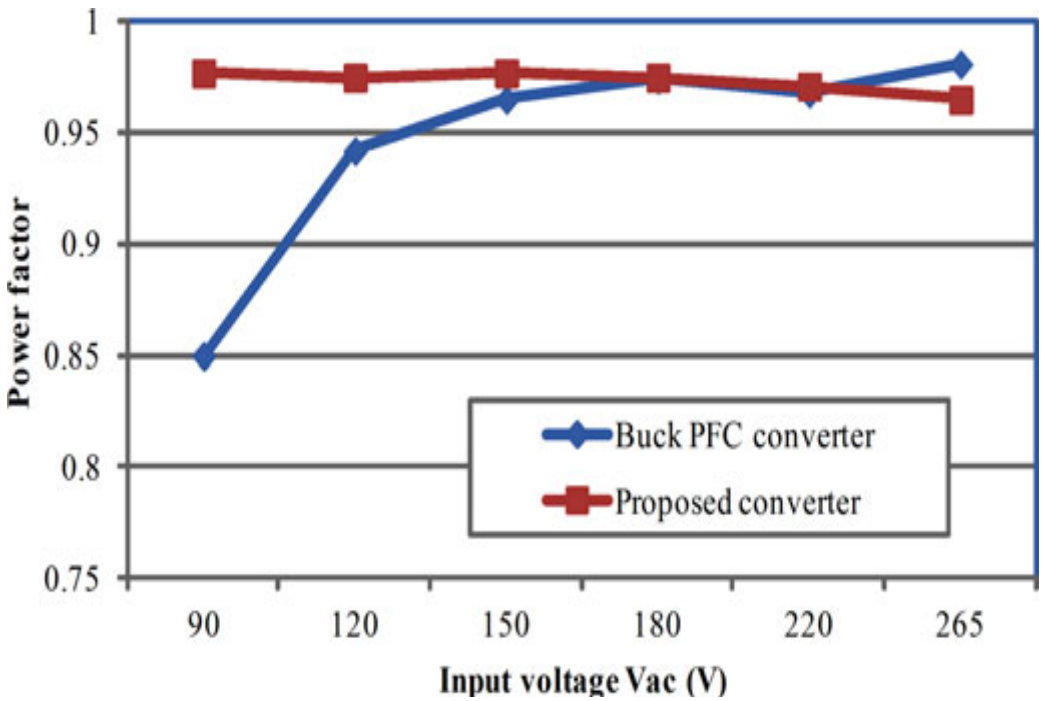


Fig.6. Measured PF at different input voltage with full load.

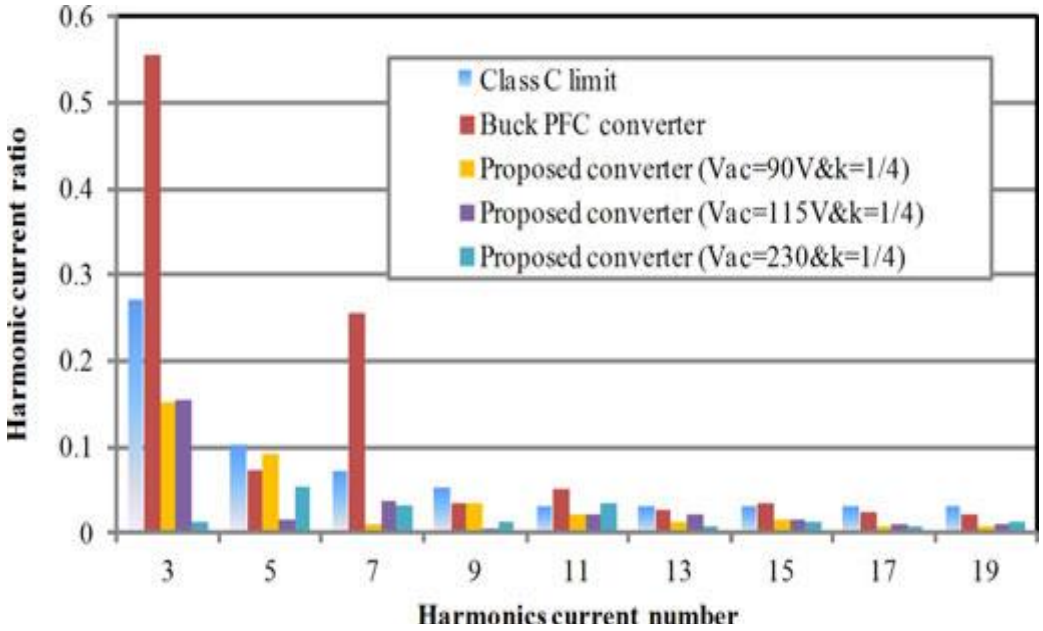


Fig.7. Measured harmonic contents of the line current under full load.

The measured total harmonic distortion (THD) of the buck PFC converter at 90 Vac input is 58%, while the THD is reduced to 18% at 90 Vac in the proposed converter. Measured harmonic contents of the line current under full load of the buck PFC converter and the proposed converter are shown in Fig.7. It can be seen that the proposed converter meets the IEC6000-3-2 class C limit with enough margins. Measured efficiencies of the buck PFC converter and the proposed converter at different input voltage with full load are shown in Fig.7.The measured efficiency curve shows that these two prototypes have the same efficiency at 90 Vac input. When input voltage increases, the efficiency of the proposed converter is a little bit lower than that of the buck PFC converter at the same input voltage due to the increased switching losses caused by switch *Q*2. However, it can be seen that the efficiency curve of the proposed converter is over the lowest efficiency point of the buck PFC converter at 90 Vac in the whole input voltage range. Therefore, the thermal design for the proposed converter is not turned worse compared to the conventional buck PFC converter. Because it is difficult to achieve very accurate loss models of the core loss of the inductor and the switching losses, there is a little deviation between the measured efficiency and the calculated efficiency.

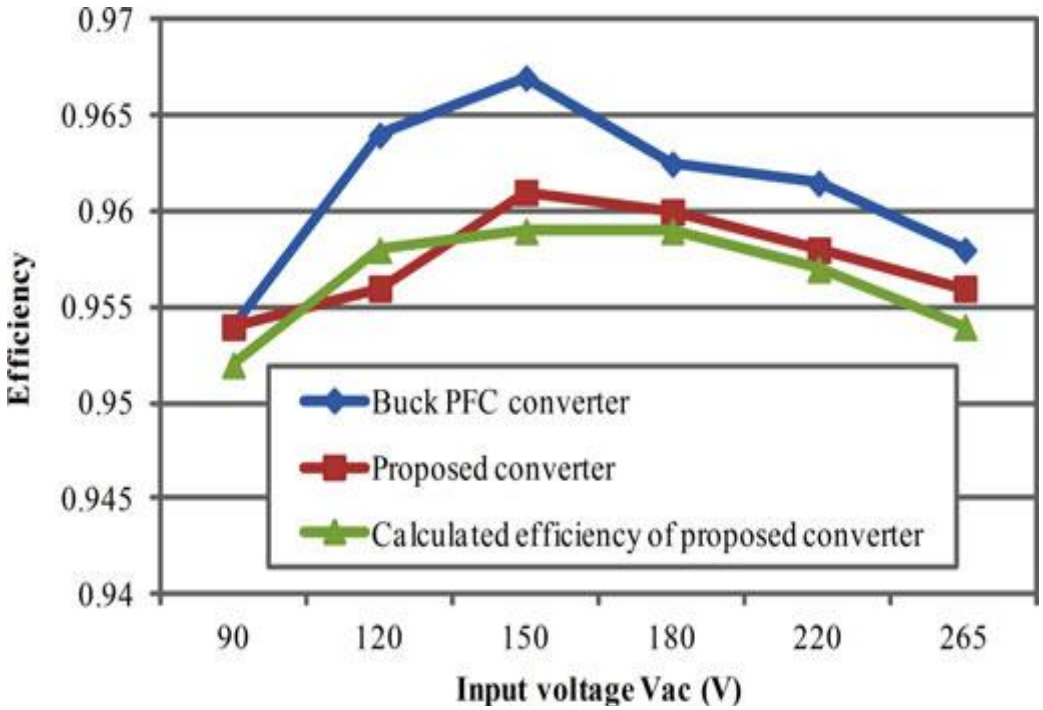


Fig.8. Measured efficiencies at different input voltage with full load.

PROPOSED WORK:

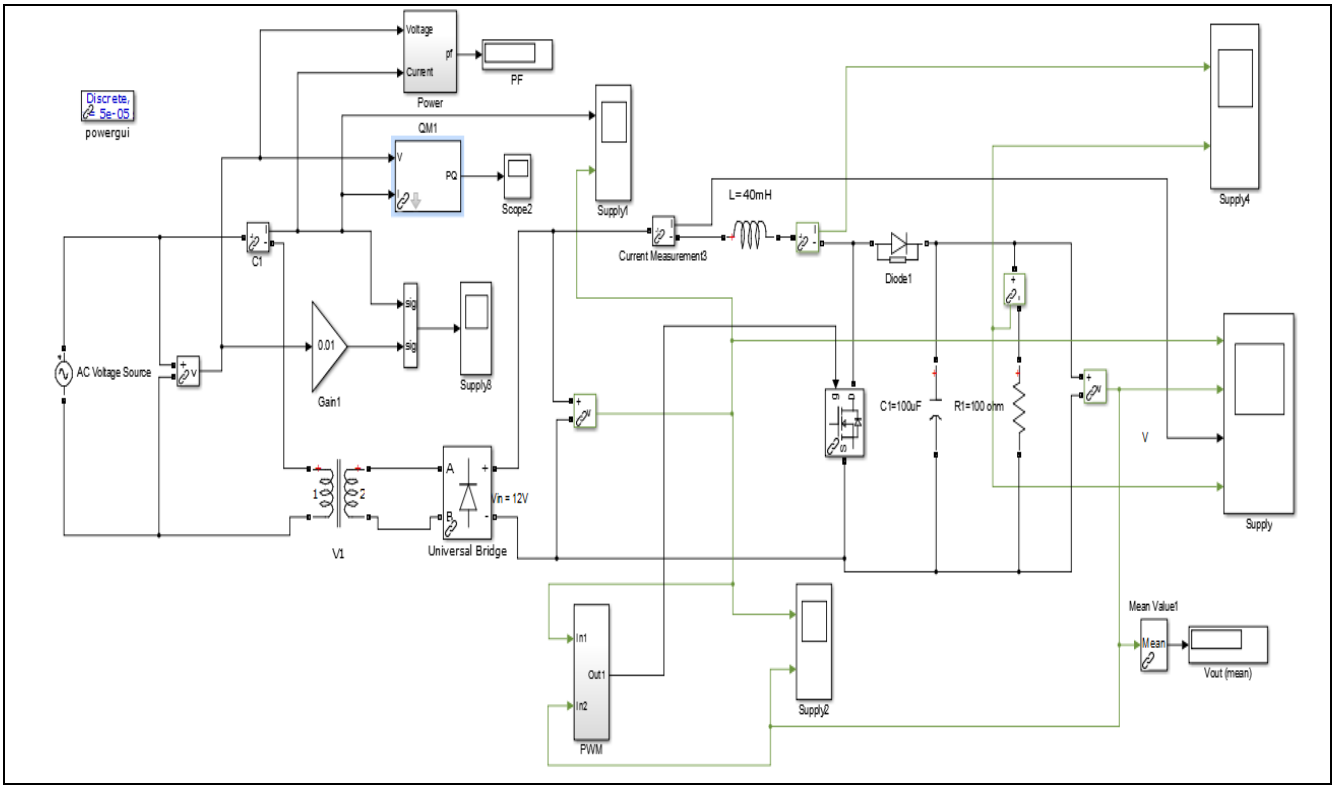


Fig.9:Simulation Model Of Proposed Buck PFC Converter

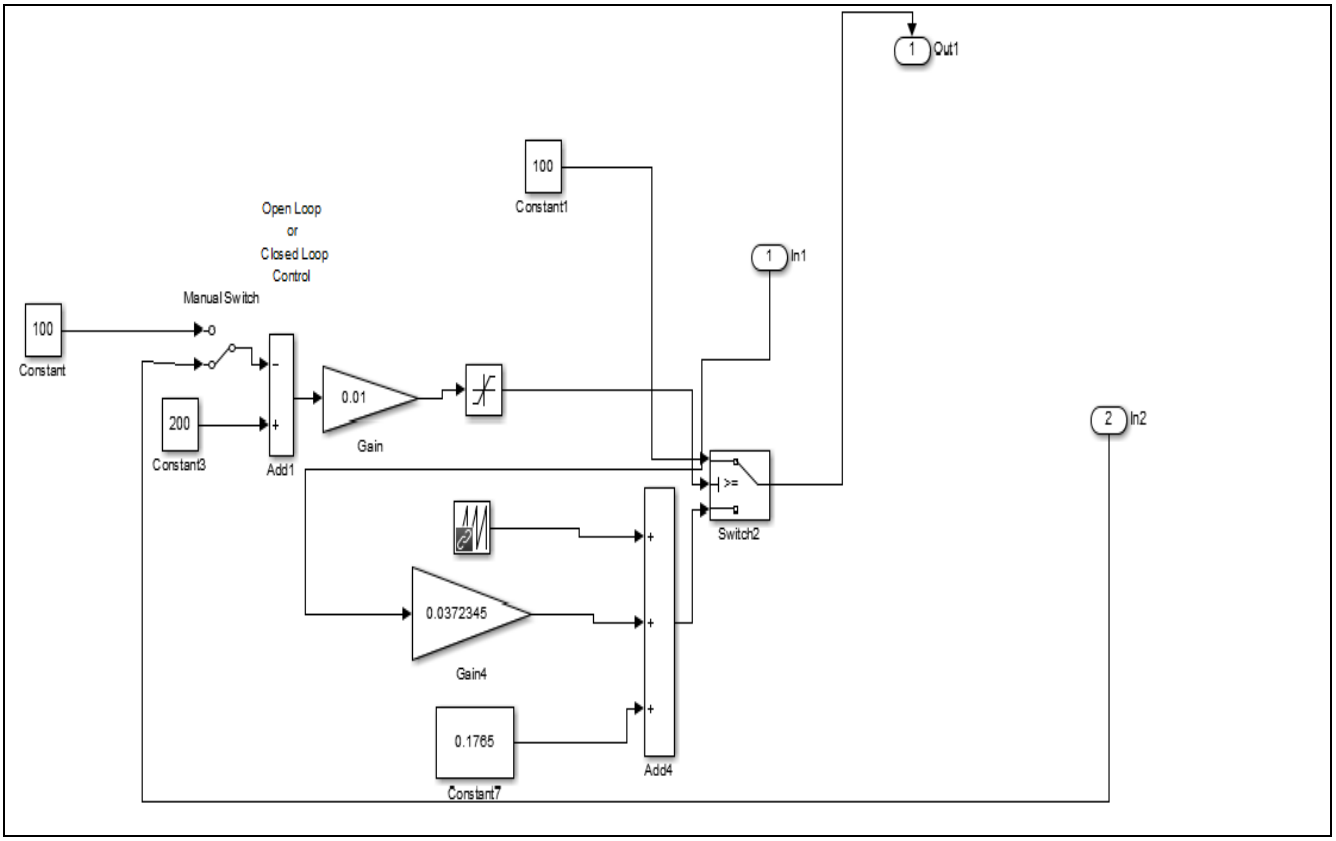


Fig.10:Simulation Model Of PWM

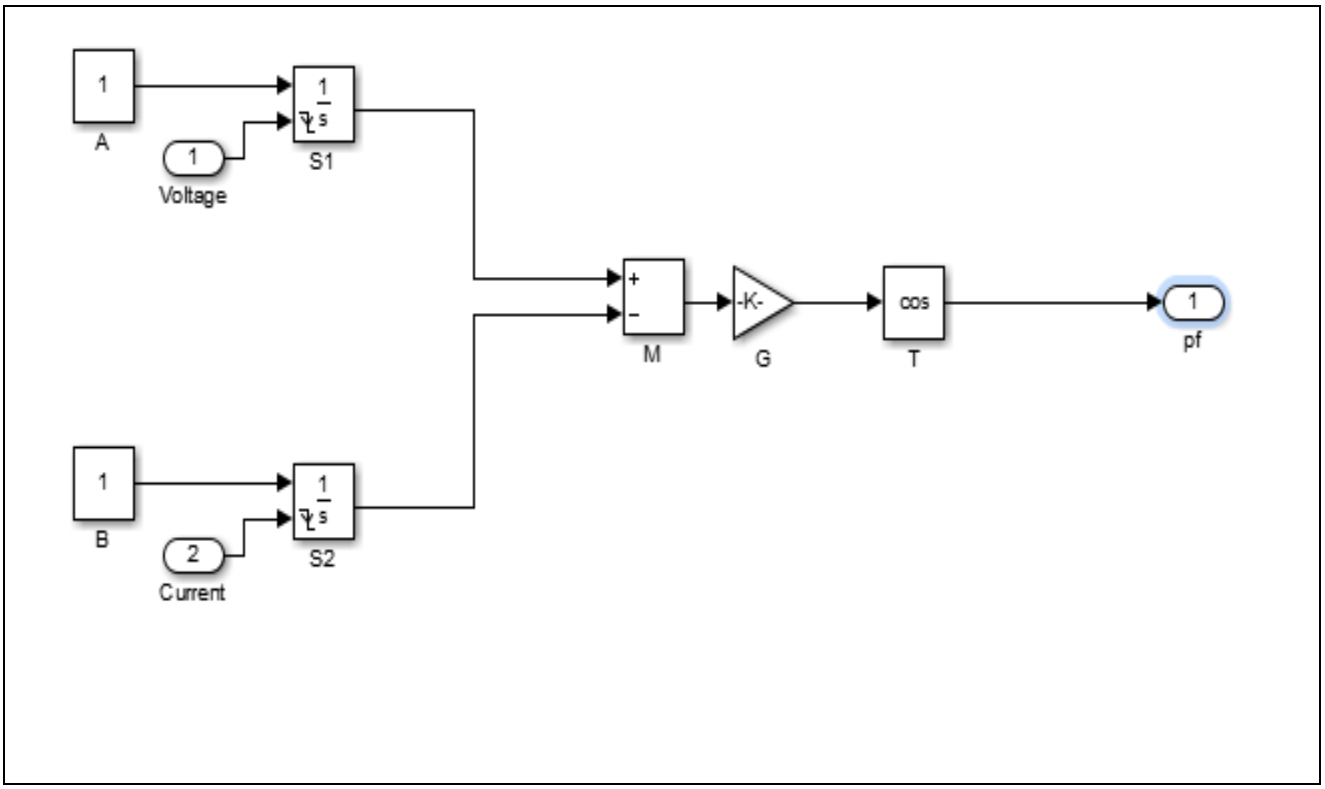
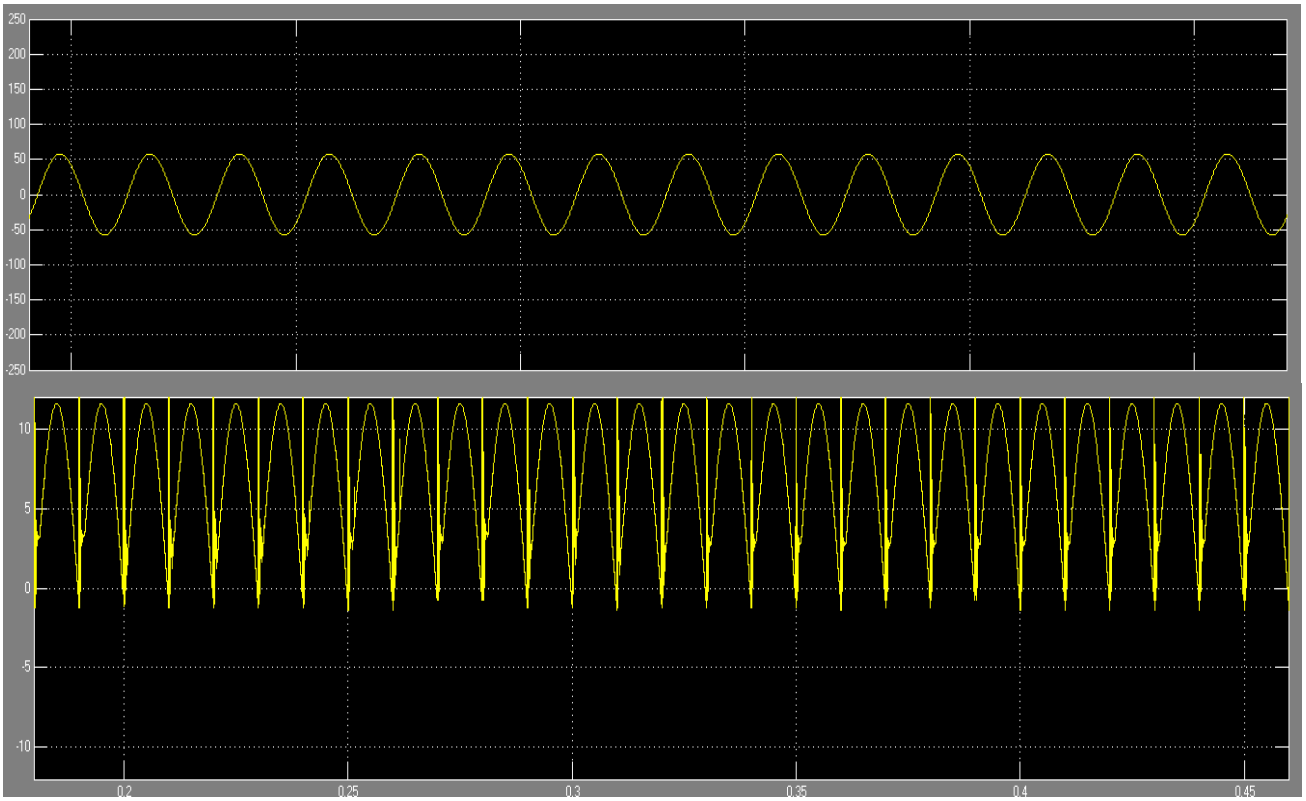
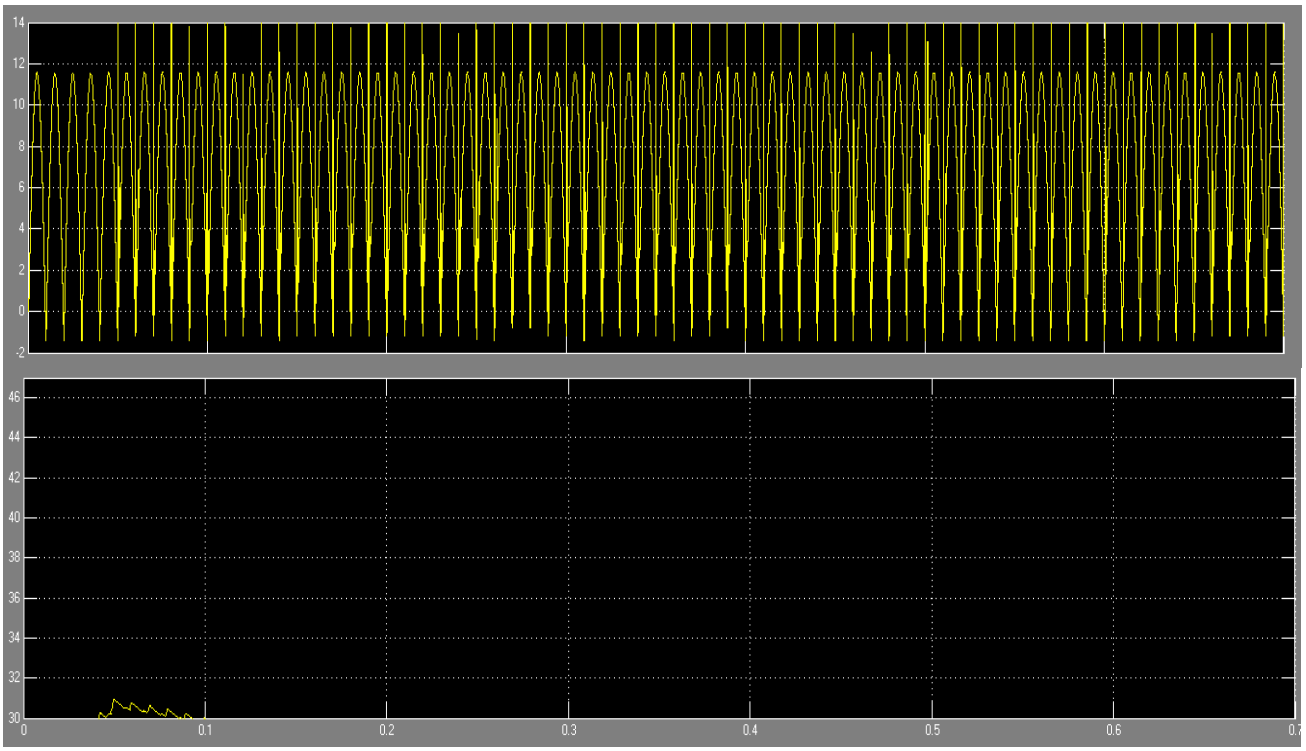


Fig.11: Simulation Model Of Power

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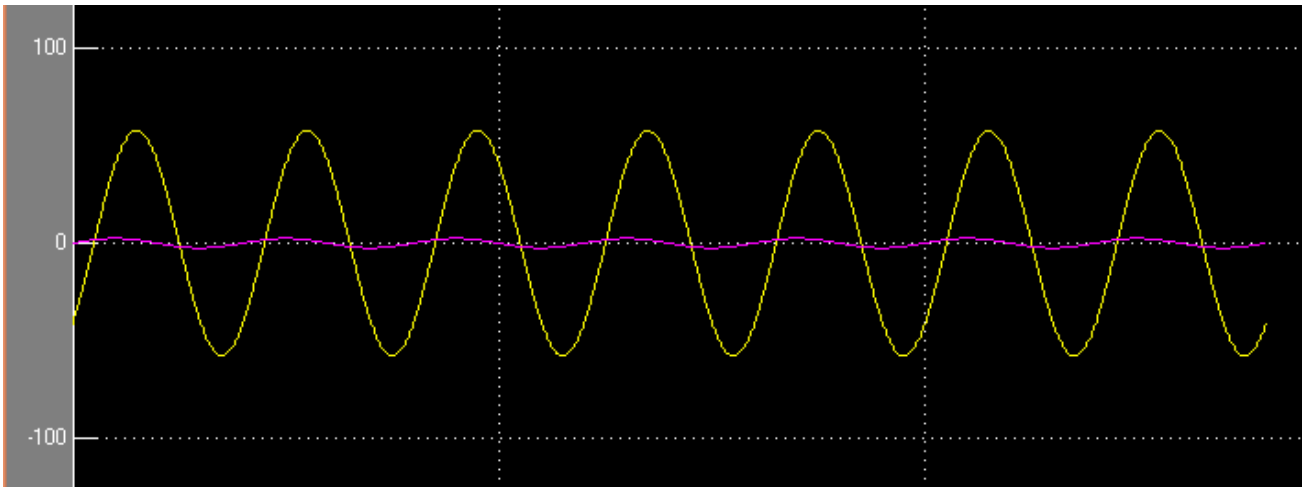
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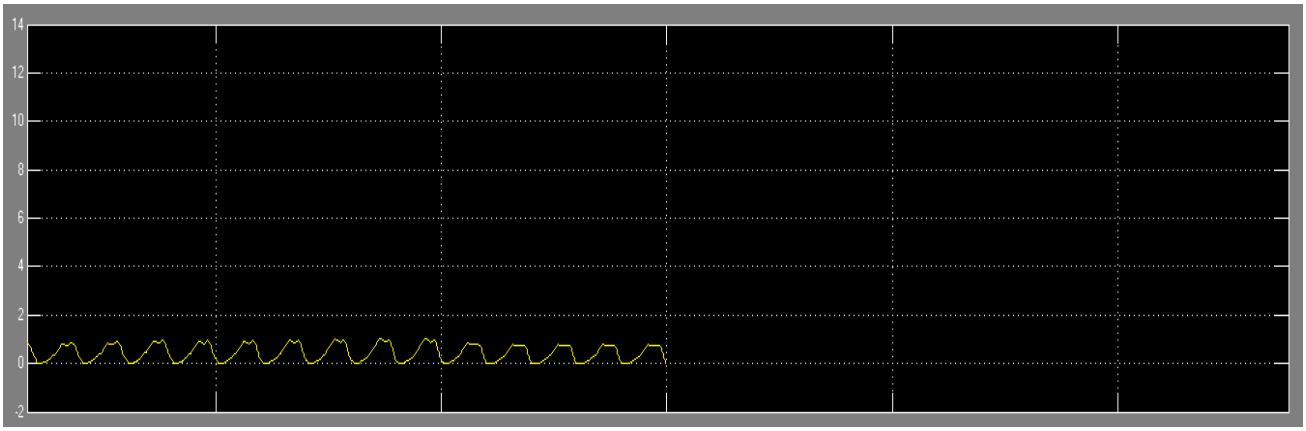
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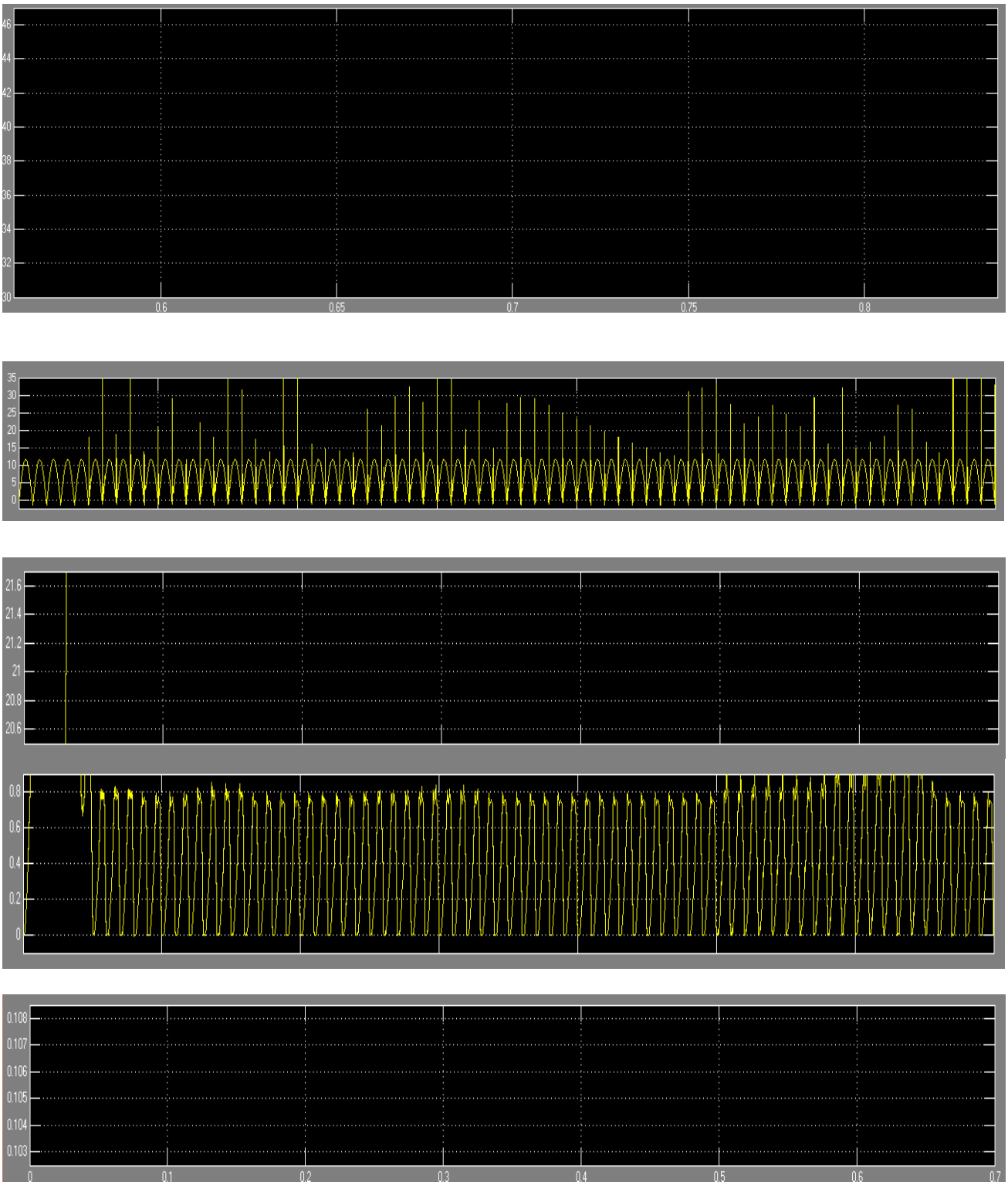

IV. CONCLUSION

The improved buck PFC converter topology proposed in this paper is easy to achieve as the structure of the topology is simple. To operate in CRM, an improved COT control is proposed. Nearly unit PF can be achieved and the input current harmonics can meet the IEC61000-3-2 class C standard within the universal input voltage range, whereas the efficiency is not deteriorated compared to the conventional buck converter. The main disadvantage of this proposed topology is that two diodes and a switch are required and the added switch needs a floating driving circuit. However, the cost and size increase little compared to the whole cost and size. Detailed theoretical analysis and design considerations of this proposed converter have been presented and the theoretical analyses are verified by a 100-W experimental prototype. In conclusion, this proposed converter is very suitable for industrial applications.

REFERENCES

[1] *Electromagnetic Compatibility (EMC), Part 3-2: Limits–Limits for Harmonic Current Emissions (Equipment Input Current≤ 16 A Per Phase),* International Standard IEC 61000-3-2, 2005, 2013.
[2] E. L. Huber, B. T. Irving, and M. M. Jovanovic, "Effect of valley switching and switching-frequency limitation on line-current distortions of DCM/CCM boundary boost PFC converters," *IEEE Trans. Power Electron.*, vol. 24, no. 2, pp. 339–347, Feb. 2009.
[3] L. Huber, J. Yungtaek, and M. M. Jovanovic, "Performance evaluation of bridgeless PFC boost rectifiers," *IEEE Trans. Power Electron.*, vol. 23, no. 3, pp. 1381–1390, May 2008.
[4] Y. Fei, R. Xinbo, Y. Yang, and Y. Zhihong, "Interleaved critical current mode boost PFC converter with coupled inductor," *IEEE Trans. Power Electron.*, vol. 26, no. 9, pp. 2404 2413, Sep. 2011.
[5] M. Mahdavi and H. Farzanehfard, "Bridgeless SEPIC PFC rectifier with reduced components and conduction losses," *IEEE Trans. Ind. Electron.*, vol. 58, no. 9, pp. 4153–4160, Sep. 2011.
[6] E. H. Ismail, "Bridgeless SEPIC rectifier with unity power factor and reduced conduction losses," *IEEE Trans. Ind. Electron.*, vol. 56, no. 4, pp. 1147–1157, 2009.
[7] M. A. Al-Saffar, E. H. Ismail, and A. J. Sabzali, "Integrated buck–boost quadratic buck PFC rectifier for universal input applications," *IEEE Trans. Power Electron.*, vol. 24, no. 12, pp. 2886–2896, Dec. 2009.
[8] J. M. Alonso, J. Vi˜na, D. Gacio, L. Campa, G. Mart´ınez, and R. Osorio, "Analysis and design of the quadratic buck-boost converter as a highpower- factor driver for power-LED lamps," in *Proc. IEEE IECON*, Nov. 2010, pp. 2541–2546.
[9] H. Endo, T. Yamashita, and T. Sugiura, "A high-power-factor buck converter," in *Proc. IEEE Power Electron. Spec. Conf. (PESC)*, Jun./Jul. 1992, pp. 1071–1076.
[10] L. Yen-Wu and R. J. King, "High performance ripple feedback for the buck unity-power-factor rectifier," *IEEE Trans. Power Electron.*, vol. 10, no. 2, pp. 158–163, Mar. 1995.