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Digital Controlled Oscillator of ADPLL designs -A Review

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Abstract: *In this Brief, the basic architecture of ADPLL is discussed. And the advantage of ADPLL over analog PLL is discussed. A review of various approaches to design the digital controlled oscillator of all digital phase locked loop (ADPLL) is presented. Today the most challenging task for designing the phase locked loop (PLL) is to achieve fast locking time and low jitter. In analog design the design complexity is increased. In this paper, advantages and disadvantages of this approaches to design the digital controlled oscillator of all digital phase locked loop (ADPLL) is presented.*

Keywords: *All digital phase locked loop (ADPLL), Phase locked loop (PLL)*

I. INTRODUCTION

Nowadays the phase-locked loops (PLLs) are widely used in various applications. For example, a chip embedded with its own clock generator to provide the high-speed clock signal, clock recovery, and synchronization of chips and jitter and phase noise reduction. Traditionally, the PLL is composed of some analog blocks, e.g., charge pump and voltage-controlled oscillator (VCO). The leakage problem will become increasingly serious in advanced CMOS processes. As a result, the difficulty and the complexity of designing an analog PLL increase as the technology process advances [4].

There are many advantages of the all-digital phase locked loop (ADPLL) over analog PLL. ADPLLs have better noise immunity, better testability, programmability, stability, and portability over different processes [6], [7], [8] and they can reduce the system turnaround time. The analog PLL suffers from reduced supply voltage and increased gate leakage as the CMOS scaling in nanometer. Also the difficulty and complexity of analog PLL increases as the technology process advances. The ADPLL reduce the sensitivity to process voltage temperature variations, area and power consumption.

The main building block of ADPLL is digital controlled oscillator (DCO). In the recent year design of DCO is improved with respect different specification needed by ADPLL. In the design of DCO the trade off is in the supply noise sensitivity, DCO resolution, frequency step size, frequency range, supply voltage.

In this paper the review of various design approach of DCO is presented. Section II describes the basic architecture of ADPLL. Section III ,IV, V describes various approaches of design of DCO for ADPLL and section VI compares this approaches and section VII discuss the conclusions.

II. ARCHITECTURE OF ADPLL

The basic architecture of ADPLL consists of phase frequency detector, digital loop filter, digital controlled oscillator and frequency divider in the feedback loop. The major component of ADPLL is the digital controlled oscillator. For the different applications the design of digital controlled oscillator has to be changed. The parameters of digital controlled oscillator are the operating frequency range, maximum operating frequency, frequency resolution. General block diagram of ADPLL is shown in Fig.1 [5].

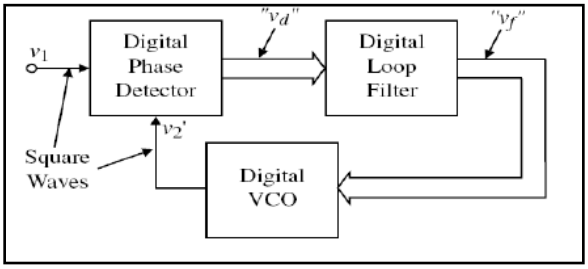

Fig.1 Basic block diagram of ADPLL [5]

III. SEVEN STAGE RING OSCILLATOR WITH PARALLEL TRISTATE BUFFER DCO

This[1] is the standard digitally controlled oscillator, which consists of a seven stage ring oscillator. it is implemented in 0.25 micron technology with an inverter delay close to 20ps and the frequency of 1.4 GHz. Also 21 tristate buffers are parallel to

each inverter. The ring oscillator contains a NAND gate which is used to control the DCO. The implementation of DCO circuit is easy to build using standard cells

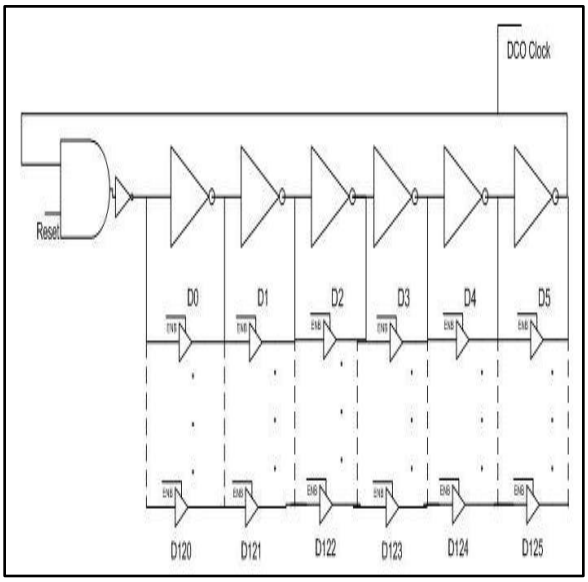

Fig.2 seven stage ring oscillator with parallel tristate buffer DCO [1]

IV. COARSE AND FINE TUNING DCO

This DCO[2] is implemented with CMOS standard cell library. It is divided into two stages: a course- tuning stage and a fine-tuning stage. The coarse-tuning stage is implemented using tristate buffer with 64-to-1 select-path architecture to provide different delays for coarse tuning. This architecture has minimum intrinsic delay time in the path selector to improve operating frequency of the DCO. Also it can be easily modified to meet different specifications for different applications. To avoid a large loading capacitance appearing in the path selector's output, the path selector is partitioned into two stages. In the first stage, every 16 coarse-tuning delay blocks will select a partial output, and the second-stage path selector will select the final output. The coarse tuning delay stage has 300ps frequency resolution. To increase the frequency resolution of the DCO, a fine-tuning delay cell is added after the coarse-tuning. The fine-tuning delay cell consists of an AND-OR-INV (AOI) cell and an OR-AND-INV (OAI) cell which are shunted with two tristate buffers. In the fine-tuning delay cell, in total 6 bits (EN1, A1, B1, EN2, A2, B2) can be controlled So fine tuning delay stage has 5ps frequency resolution.

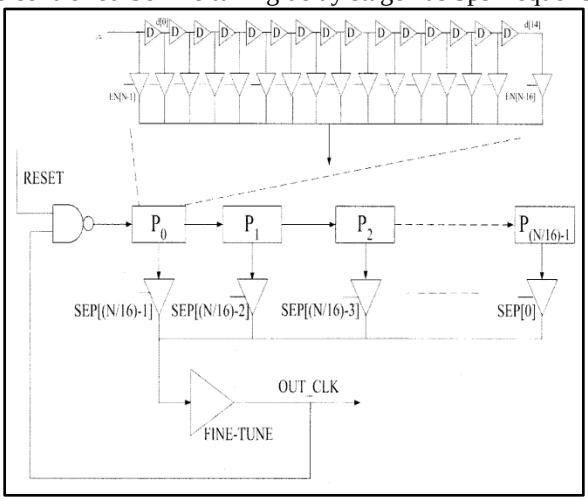

Fig.3 coarse and fine tuning delay stage DCO [2]

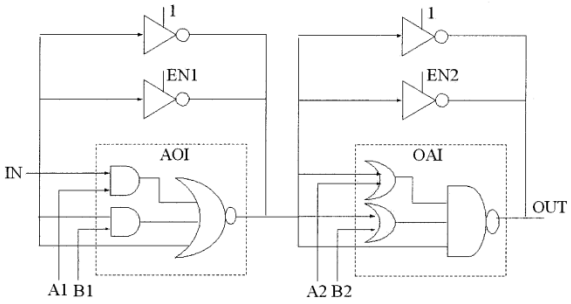

Fig.3 AOI cell and OAI cell of fine tuning delay stage [2]

V. PARAMETERIZED DCO

Parameterized DCO[3] is formed with a loop including two parts the coarse tuning block (β-part) and the fine tuning block (γ-part). During frequency acquisition β-code selects the frequency and during phase acquisition γ-code decides the final output. In the coarse tuning block N tri-state buffers are connected in parallel to one buffer in each tunable delay-stage. When the numbers of enable tri-state buffers increases driving current to the tunable delay-stage. So the overall delay of the delay chain will decrease. In Fine-Tuning Block two-input NAND gate array is attached to the output node of β-part in each tunable delay-stage, which can slightly adjust the output frequency of DCO by controlling the number of turned-on NAND gates. A β-range is the range of the DCO's clock periods spanned by varying the γ -code under a specific coarse-tuning β-code. During the DCO's frequency locking step, we only need to decide the best initial β-code. As for the fine tuning of γ -code within the selected β-code, we then decide it in the phase-locking step. This architecture of the DCO is very flexible and easy to change to meet various specifications due to its large configuration space.one configuration of DCO is decided by the combination of the following five parameters: 1) the type of the buffer; 2) all sorts of combination of the driving-strength-tuning block (i.e., the parallel-connected tri-state buffers); 3) the number of loading gates used in the fine-tuning block; 4) the number of delay stages; and 5) the number of startup gates to meet the application and specification.

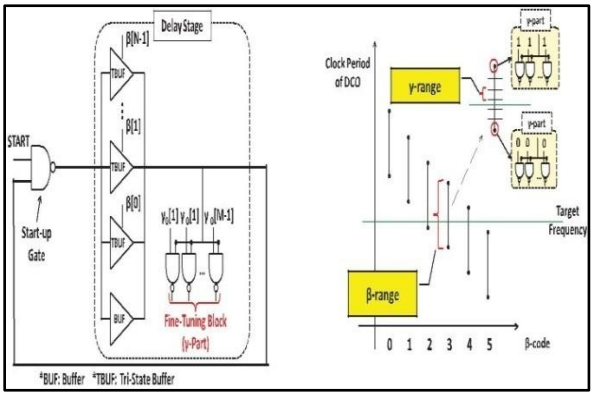

Fig.5 Parameterized DCO [3]

VI. COMPARISON

	Advantages	Disadvantages
[1]	Simple structure, lock time is 105clock cycle,	Higher power consumption, frequency operating range is small, jitter is high
[2]	Higher frequency resolution, rms jitter is less than 22 ps. lock time is 46 clock cycle,	100mW power dissipation
[3]	Higher operating frequency range, higher resolution, rms jitter is 4.3 ps	frequency operating range is small

VII. CONCLUSIONS

In this paper the review of Digital controlled oscillator of ADPLL is presented. For increase the frequency resolution of DCO the coarse and fine tuning stage is implemented. But it consumes more power than simple ring oscillator structure

presented in [1]. Parameterized DCO can generate more than 1GHz frequency with increased frequency resolution. Also it consumes low power but it has narrow operating range of frequency

VIII. ACKNOWLEDGEMENT

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