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A Review on Application Specific Wireless Sensor Nodes using FPGA

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Abstract— Nowadays in embedded systems technology, energy efficient sensor nodes are the most growing application. Basically wireless sensor nodes contain the Sensing unit, Data acquisition unit, Transceiver unit, Power unit. In data acquisition unit processing part contains mostly programmable micro-controller and digital signal processing, but this result in higher power consumption than actually needed by application specific sensor node. The current research work shows that flash FPGA technology can be implemented for precisely application processing for sensor nodes with efficiency of energy and upgradability towards its application. That rivals to the general purpose processor solutions. This will save the materials of hardware and also a workload of software. As the same hardware chip is use for the processing unit and transceiver unit. So this result gave the way for the new type of self-powered sensor nodes, which can be configured according to their specific application.

Keywords- Spartan III FPGA development board, Xilinx 12.2, Modelsim 6.3c, JTAG cable, and power cable.

I. INTRODUCTION

A wireless sensor network (WSN) is a collection of nodes organized into a cooperative network. Each node consists of processing element such as memory (program, data and flash memories), RF transceiver (usually with a single Omni directional antenna), power source (e.g., batteries and solar cells), and various sensors and actuators. The sensor nodes communicate through wireless channel and often self-organize after being deployed in an adhoc fashion. Systems of 1000s or even 10,000 nodes are anticipated. These systems can revolutionize the way we live and work.

Currently, wireless sensor networks are beginning to be deployed at an accelerated pace. We should not surprise to expect that in coming years the world will be covered with wireless sensor networks and we with access them via the Internet. This can be considered as the Internet becoming a physical network [1]. This new technology existing with unlimited potential for numerous application areas including environmental, medical, battle field surveillance, targeting, transportation, entertainment, critical situation management, homeland defense, and smart spaces, auto motive applications, vehicle tracking and detections, home and office automation. Apart from the increasing demands in traditional applications, new ones have shown up related to, environment, surveillance, communication security, tracking algorithms, etc. [2]. All of these applications require much more powerful processing units to deal with huge amounts of data and complex calculations. These high performance applications are normally related to the use of precision agriculture, video cameras, data encryption, data compression, audio applications, large deployments, tracking algorithms, latency restrictions and synchronization, big memory usage etc. That is the reason why new WSN architectures must be studied to be able to face these new complex operations.

The majority of them are multimedia applications that include the use of low-power video cameras and microphones. These applications are known in the state of the art as Wireless Multimedia Sensor Networks (WMSN). These applications can be categorized in surveillance, traffic monitoring and enforcement, personal and health care, gaming and environmental and in industries. Surveillance is probably the best example of the increase of complexity in traditional WSN applications. Applications related to environmental care and industrial monitoring can be also faced and improved by means of using these high performance networks. For instance, full manufacturing processes including quality control can be monitored relying on artificial vision techniques [2] [3].

However, the increase of complexity requires higher resources to cope with these new applications. This extra computing power can be achieved by means of either using more powerful microcontrollers or any other solution capable of accelerating task execution. Normally the increase of the node capabilities implies an increment of the energy consumption so that new energy saving policies must be taken into consideration.

The first solution could be the inclusion of more powerful microcontrollers. This solution can be suitable for some applications, since they offer a very intensive tasks, the computing time can be very high leading to a non-efficient solution in terms of energy consumption. A better solution can be achieved using Digital Signal Processors (DSPs), however, even though the computing time can be reduced compared to standard microcontrollers, it is still high so it is difficult to keep power consumption in acceptable levels for WSN standards

II. RELATED WORK ON SYSTEM ARCHITECTURE

As FPGAs and ASICs can do their tasks in parallel so they can provide the high speed processing. But this will decrease the computing time very sharply so the node can remain in sleep mode for longer periods of time. So due to the lack of flexibility and the huge design time we are not using ASICs in WSNs. So to overcome this, FPGAs are presented as a very suitable solution for high performance WSN applications.

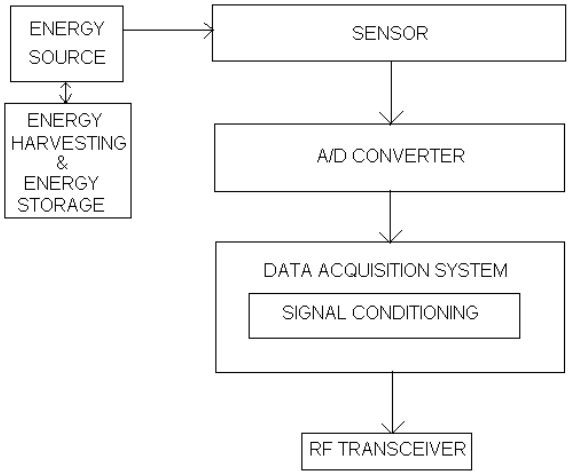

Figure 1. Block diagram of a typical wireless sensor node

The Sensor Node Components are:

- Sensing Unit
- Data acquisition Unit
- Transceiver Unit
- Power Unit

A typical low cost wireless sensor node is illustrated in Fig.1. The sensing unit, data acquisition unit, and radio transceiver unit are used to implement the processing, control, and communications functionalities, respectively. Sensing unit contains real time sensors for specific any industrial application and data acquisition unit contains FPGA along with the memories to store programs and sensor's data, where transceiver unit contains any communication module like RF module, zigbee module. In addition, the WSN has a power supply unit that supply energy from a battery, or an energy harvesting unit [3].

The data acquisition Unit has a number of functions including:

- Collecting data from the sensors and manage them.
- Management of power consumptions.
- Interfacing the sensor data to the physical radio layer.
- Managing the radio network protocol.

A key aspect of any wireless sensing node is to minimize the power consumed by the system. Usually, the radio subsystem requires the largest amount of power. Therefore, data is sent over the radio network only when it is required. An algorithm is to be loaded into the node to determine when to send data based on particular the sensed event. Furthermore, it is important to minimize the power consumed by the sensor itself.

The multiple sensors and measurement channels may come from the application needs, such as disturbance cancellation to dig up the signal of interest. Multiple sensors may also be employed to compensate

for the mediocre performance of the low cost sensors, and even to provide for redundancy needed in simple self-diagnostics [4].

Our design approach relies on exploiting genuine parallel processing for the measurement channels to reduce software testing and development effort. Thanks to the reconfigurable system platform, a mix of applications from signal processing to baseband processing can be supported on a single chip [5].

III. RELATED STUDY ON POWER CONSUMPTION

Very few sensor nodes give the constant performance on data processing. On the field with some application there are long idle periods. During these, sensor nodes should switch to the low power mode to save the consumption of unnecessary energy. After that sensor nodes should expeditiously recover back from the low power mode. By using FPGA this can be possible in approximately microseconds [6].

Decreasing the energy during operation of system energy efficiency of the sensor nodes will increase the life of the sensor nodes. To implement such concept there are types of processor architectures called heterogeneous multiprocessor. In this sensor node is design with two controllers, one is the low work load phase and another is high end embedded processor. In normal condition sensor uses the low work load phases and when it detects the activity from the field the high end processor is awaked and processing is done on the given activity. And once that activity is over sensor again transit from the high end processor to the low end microcontroller and high end processor is shutdown.

Just like a conventional multiprocessor system where the processor works on parallel manner in this technique one of the two processor is worked at time and another remains in sleep mode .but the challenge is, when and how much time to switch from the one processor to the another[6] .

Up till now whatever power management system we have seen is based on the changing in hardware or software part of sensor nodes. But for a while now we will focus on the energy supply system and battery system for the sensor nodes. As the batteries has the limited energy storage capability. A new emerging technique to overcome this limitation is environmental energy sources.

The solar energy harvesting uses photo voltaic conversion to provide the highest unlimited power supply, but the limitation of this solar energy is it will not give the energy constantly. It increases the energy level at the day time and lowering at the night [6] [7].

As known, one of the major factors of the any embedded system is the program code and its size as well. As the program code increases, size and cost of the memory also increases, which in turn ultimately burden to the power consumption. This is the major problem mostly with Very Large Instruction Word (VLIW) architectures [8].

So to overcome this problem dictionary compression programming technique is used. The Dictionary compression is most commonly used because of its simplicity and less code density. In this technique instruction words which is frequently used in programming is stored in dictionary and then whenever this instruction word is used in actual program it will be replaced by its code words. In this bit toggling information was used to restore the original instruction. Dictionary contains number of code words which is allocated to each substrings .As the code words is smaller than the original substrings and the compression is achieved [8] [9].

Like a dictionary compression another method to increase the code density is the entropy encoding which states that some symbols we mostly used than the rest, so replaced them by the shortest code.

IV. PROPOSED WORK

As a Discussed above FPGA based sensor nodes design is very universal design which can be applied at any of the wide range of area of applications. It is also useful where the processing of the system requires fast operation with less energy consumption. And this design gives the optimal solution to the requirement of the precision processing at moderate cost.

In near future we are going to implement above used technique for the health care application along with the EEG transmission sensors.

A Brain computer interface (BCI) is system which is works as the medium between the brain and the computer. The BCI is the system which have made possible of the external devices can be controlled trough your brain. For this electroencephalogram (EEG) is the main sensing device. This sensor is use for the medical diagnosis and neurobiological research. EEG tool reacts in milliseconds. Hence it becomes the more popular than any others. As EEG is the signal to communicate between the computer and brain like brain waves. Human nervous system can produce an electrical signal which is invented years ago. As the electrical signals

from the variation of the surface potential distribution on the scalp reflects functional activities emerging from the brain. This variation in surface potential can be recorded by fixing the array of electrodes to the scalp and this data between these pair of electrodes measured in voltage. This is called the EEG which is in micro volts. BCI amplifies them approximately ten thousand times to record them. This technology strongly depends on the positioning of the electrodes and its contact [10].

As this technology is used at sensing unit this collects the brain waves and amplifies them to convert into the digital signal which is then processed by the data acquisition unit. These signals are transmitted using any communication module, which can be selected as per the required distant.at the receiver end we can control any device by connecting these signals to actuator or connect it to the Pc using hyper terminal for monitoring from remote location. We can also observe that signals on MATLAB using its GUI function. This will become the wireless platform for the specific application of EEG Signals. Just like BCI system we can also make Heart computer interface (HCI).for this we are using electrocardiograph (ECG) signal for monitoring the pulse rate of heart.

This sensor nodes will be very helpful to the physically disable patient for continual monitoring health from remote location as well and other Health application. Other advantages of the system come in complementary.

V. CONCLUSIONS

Implementations of FPGA over conventional devices in wireless sensor nodes accomplish or go beyond the energy efficiency. A new data acquisition unit including FPGA will fulfill the requirement of complex powerful processing and high speed operations with more power efficiency. In case of the hardware based solution a significant reduction of the energy consumption is observed, while the speed of processing is much higher. The Quality of Service reduces cabling and installation costs, possibilities of breaking cables, less trouble with the connectors, and hence this system provides more mobility, error control schemes, hybrid wired and wireless system, security and privacy, upgradability, scalability, accurate handovers under real time.

This system can be used with number of nodes at a time. Future scope for this work is to focus on problem of recognizing activity of one particular sensor.

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