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IMPLEMENTATION OF 2GBPS CLOCK AND DATA RECOVERY CIRCUIT USING PLL WITH HIGH JITTER TOLERANCE

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Abstract: *The data integrity that the SerDes offers is predominantly due to the Clock and Data Recovery Circuit (CDR) employed within the design. The CDR takes the incoming data and generates a clock using the data specs which can then be used by the deserializer to sample the data accurately. This paper looks into the basic principles of operation of Phase Locked Loops, Clock and Data recovery circuits and their building blocks for a 2 Gbps SerDes link with high jitter tolerance. Implementation of differential mode VCO with low gain to reduce the jitter. It summarizes the challenges in design and also presents a Cadence approach to the circuit design in 180 nm CMOS technology.*

Keywords*-Phase Locked Loop (PLL), Phase Detector (PD), Charge Pump (CP), Loop Filter, Voltage Controlled Oscillator (VCO),Frequency Divider, Lock-in range, Lock time.*

I. INTRODUCTION

Clock and data recovery (CDR) has been widely used in data communication systems, including optical communication, backplane routing, chip-to-chip interconnects, and disk drive read channels. Binary data is commonly transmitted in the "nonreturn-to-zero" (NRZ) format[1-4]. The ability to regenerate binary data is an inherent advantage of digital transmission. To perform this regeneration with the fewest bit errors, the received data must be sampled at the optimum instants in time. Since it is generally impractical to transmit the requisite sampling clock signal separately from the data, the timing information is usually derived from the incoming data itself. The random data received in these systems are both asynchronous and noisy, requiring that a clock be extracted to allow synchronous operations.[2-8] The recovered clock both removes the jitter and distortion in the data and retimes it for further processing. It is called clock and data recovery.

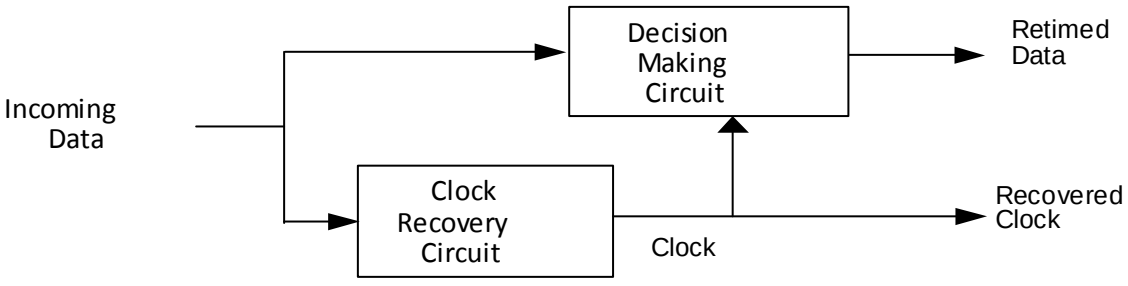

Fig. 1. Simplified block diagram of a digital receiver

The clock generated in the circuit must satisfy the following conditions:

- The frequency of the clock must be equal to the data rate.
- The clock must have appropriate timing with respect to the data, allowing optimum sampling of the data by the clock; if the rising edges of the clock occur in the midpoint of each bit, the sampling occurs farthest from the data transitions, providing maximum margin for jitter and other time uncertainty.

- The clock must exhibit a small jitter since the jitter of the clock contributes to the retimed data jitter

II. IMPLEMENTATION OF THE CIRCUIT

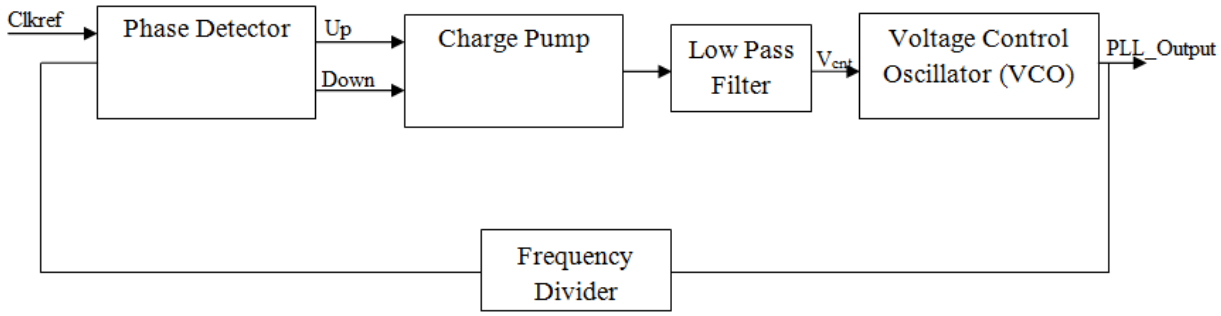

Fig.2. PLL Block Diagram.

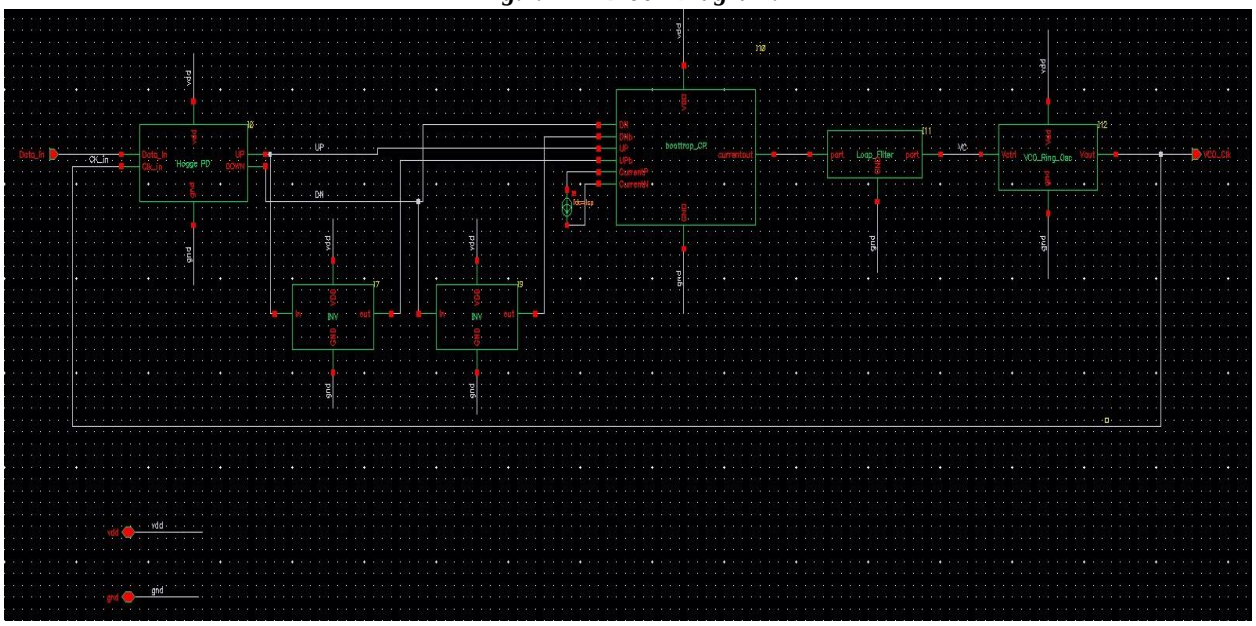

Fig.3. CDRImplemented Diagram

HOGGE PHASE DETECTOR:PD compares the incoming signal with the PLL output and generates the phase difference as an error signal. The PD circuit should consume low power and have a minimum dead zone. Dead zone is a region wherein a PD fails to detect small phase errors. This occurs when there is very small phase difference between the reference signal and VCO output signal. It generates UP and DOWN pulses based on the frequency.The Hogge PD is a linear phase detector. The PD makes use of the VCO output to sample the data. It consists of two D Flip flops and a XOR gates put together as shown.

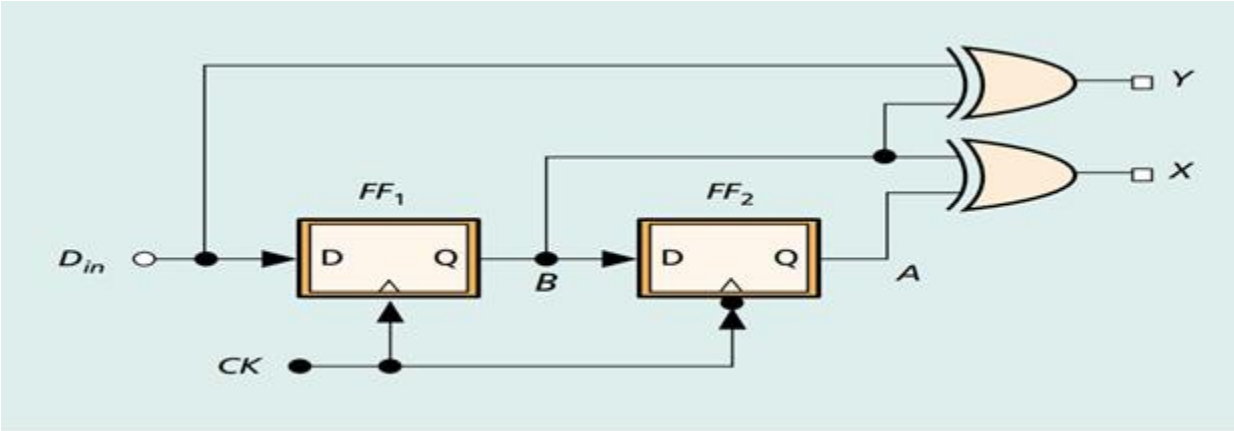

Fig.4. Hogge Phase Detector

CHARGE PUMP (CP) AND LOW PASS FILTER (LPF): The function of a charge pump and low pass filter is to take the outputs UP and DOWN signal from the PD and convert them into an analog control voltage (V_{cnt}). Fig 3.11 shows the simplest CP and LPF circuit.

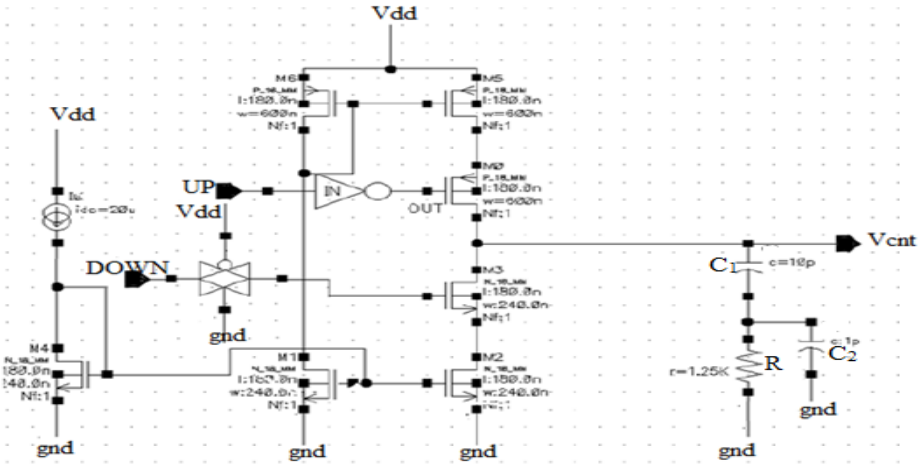

Fig. 5 Charge pump and Low pass filter

Charge Pump Design

$$Vc(t) = \frac{\text{Icp}}{2\pi \text{Ccp1}} \text{t}.\Delta\emptyset$$

Where,
V_C (t) = control voltage.
I_{cp} = output current.
C_{cp1} = output capacitance.
$\Delta\emptyset$ = phase difference between the two signal.

VOLTAGE CONTROLLED OSCILLATOR (VCO) : A simple oscillator produces a periodic output, usually in the form of voltage. As such the circuit has no input while sustaining the output indefinitely. A Voltage Controlled Oscillator or VCO is a circuit whose output frequency is linear function of its control voltage

The applied control voltage determines the instantaneous oscillation frequency. Consequently, modulating signals applied to control input may cause frequency modulation (FM) or phase modulation (PM). A VCO is a part of a phase-locked loop.

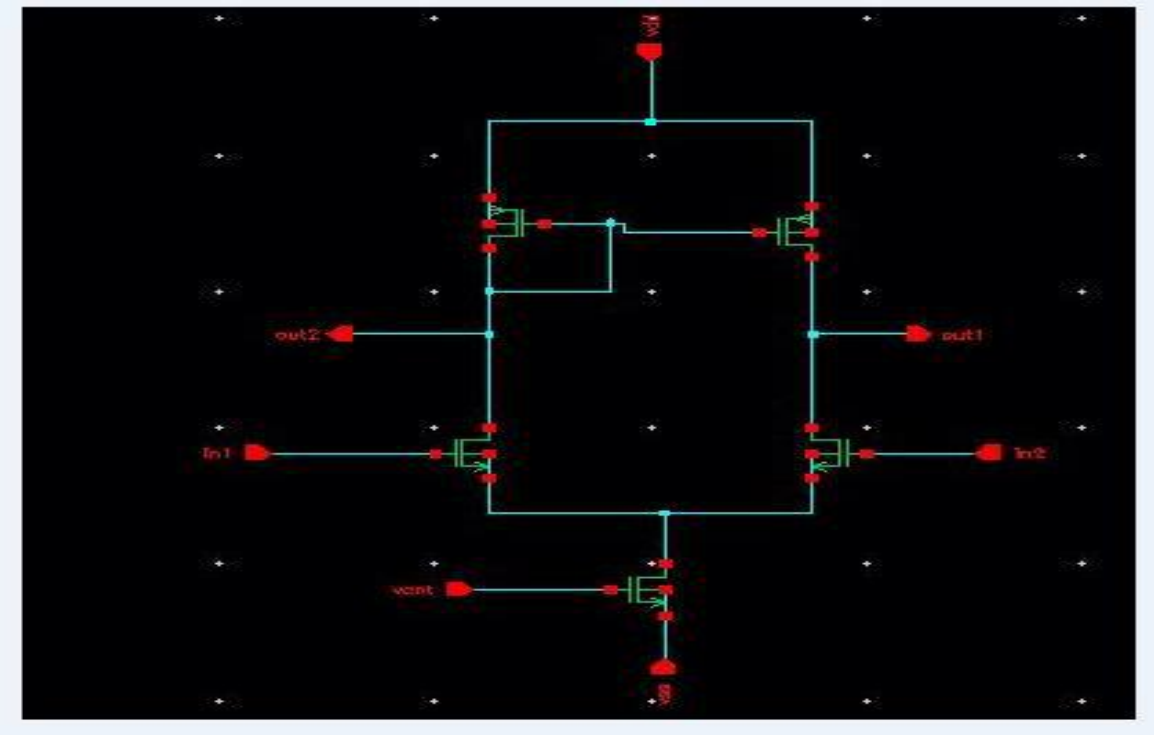

Fig.6. Differential Amplifier

Differential Amplifier: The above fig 6 shows the differential amplifier circuit then designing a symbol and four blocks are design from the amplifier connecting all the blocks in the form of a ring to ensure that we get a phase difference of 180 degrees, and to achieve desired frequency. The major tuning parameters are the gm (or W/L) of load for the required frequency and the gm (or W/L) of the input NMOS to get the required gain greater than unity. VCO circuit is shown in Fig According to design specification of 2496MHz oscillation frequency has been achieved.

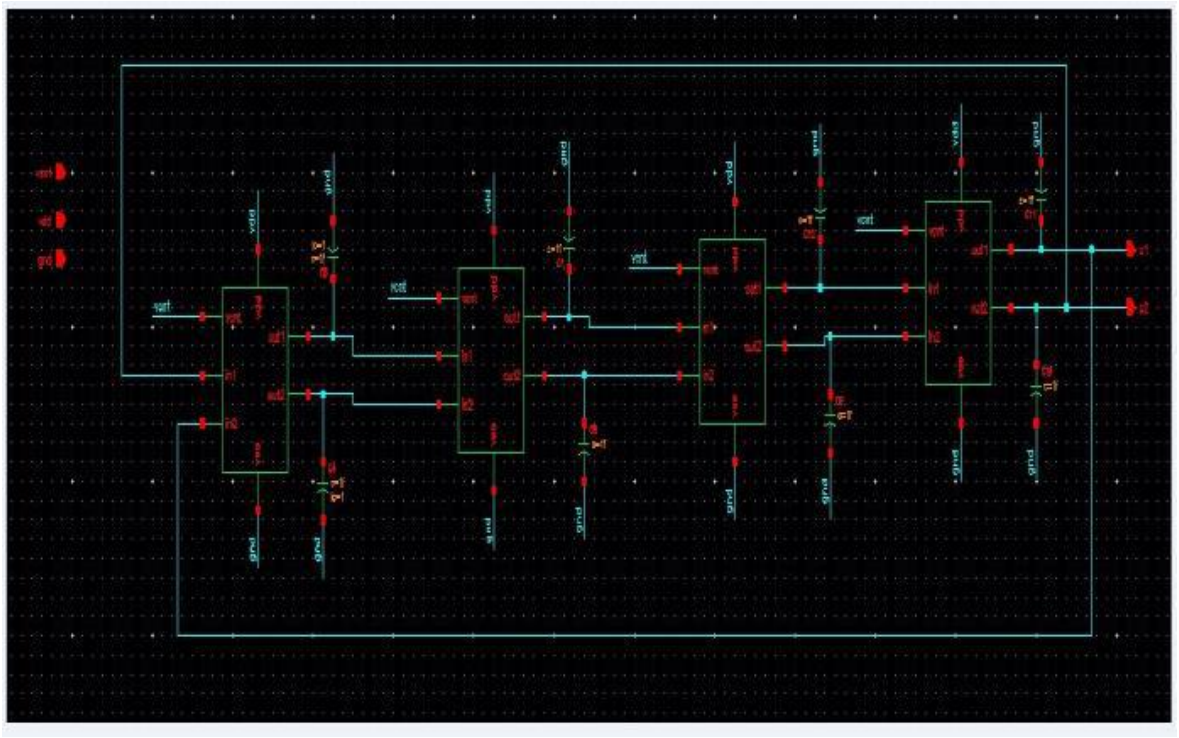

Fig. 7, VCO Design

FREQUENCY DIVIDER: Frequency divider circuit is a VLSI phase scaling circuit. It is responsible to down-convert the frequency of an input signal to a lower value. We can achieve programmability in the output frequency by using a programmable frequency divider circuit. Phase-locked loop frequency synthesizers make use of frequency dividers to generate a frequency that is a multiple of a reference frequency. In our case a 1\4 frequency dividers that operate for a supply voltage of 1.8V are used.

We have used the Positive edge D flip flops for the design of the flip flop present in the frequency divider. Positive edge D flip flop is insensitive to clock overlaps or skew. Therefore, the possibility of sampling error due to timing variation of clock edge of flip-flop in high speed operation is eliminated.

The architecture becomes simple compared to flip-flop or SR latch using one with lower power consumption and area. In our Design, the frequency division factor depends upon Rate select signal. Based on the output frequency we have designed 1/4 dividers. We have used the D flip flop based designed for all the frequency dividers. Divide by 4 are implemented using 2 individual frequency dividers namely ½ schematics as shown below Fig 8.

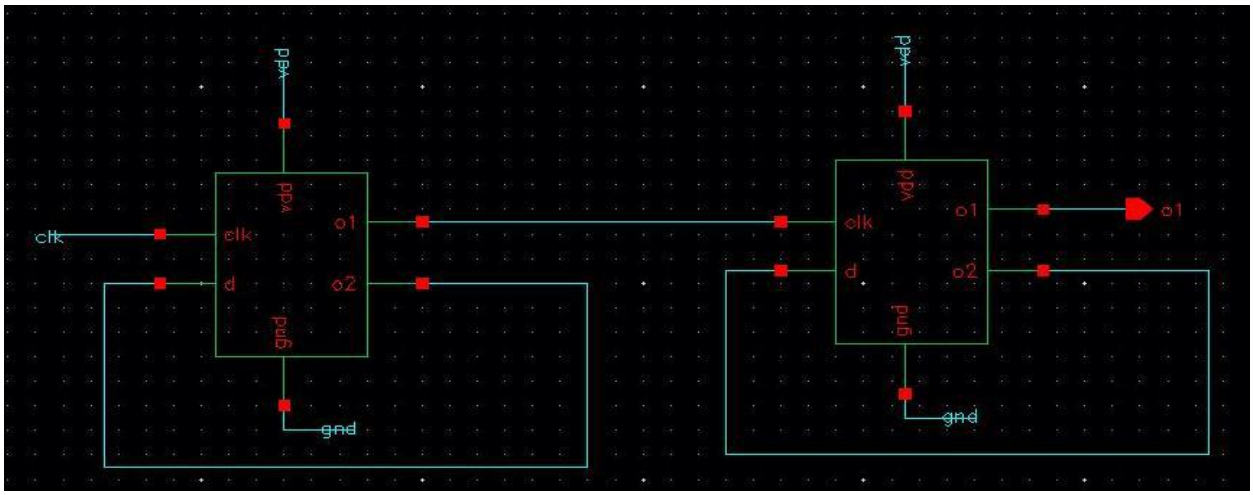

Fig 8, Frequency Divider

III. SIMULATION RESULTS

The proposed PLL system is simulated in CADENCE 180nm Technology. The output clock generated for a frequency of 2496MHz is shown in Fig.8. The time taken for the PLL to lock to the reference frequency is 4.199us. The control voltage for this frequency is 1.4 V and is stable in the acquisition period.

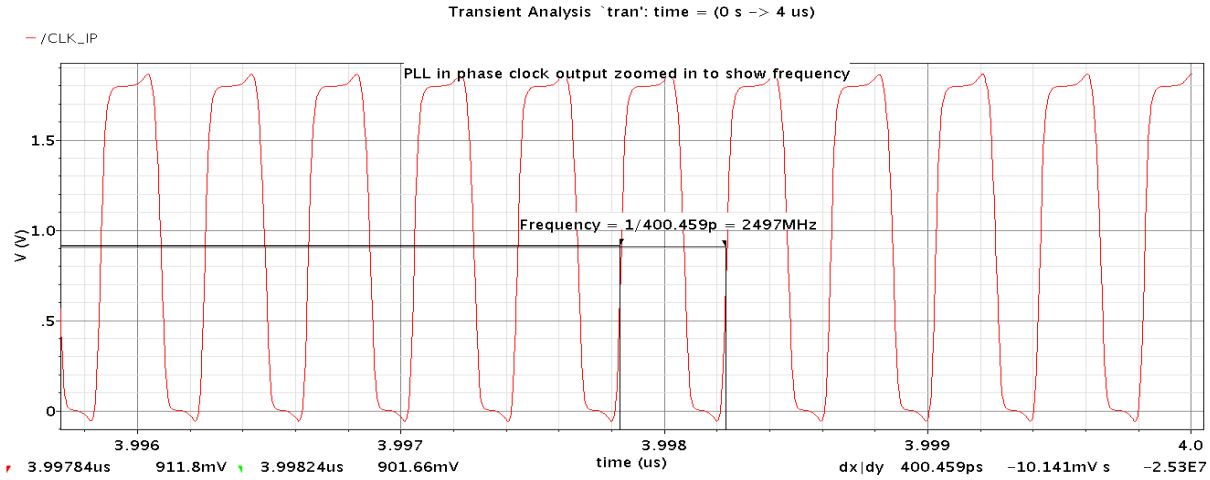

Fig. 9 PLL output

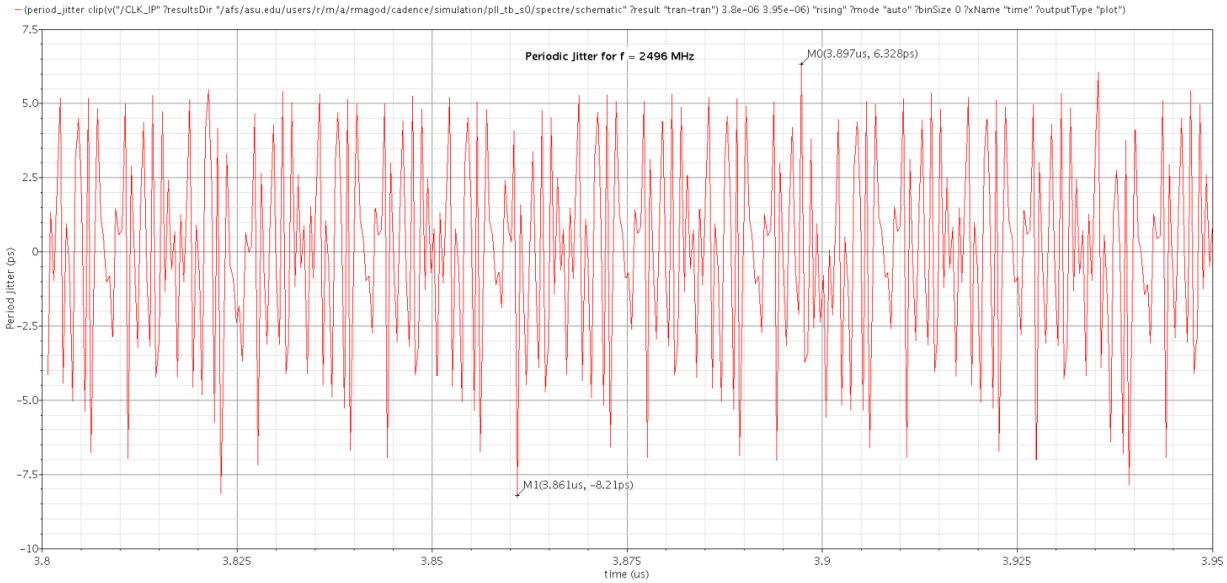

Fig. 10 , Periodic Jitter ---- Maximum → 8.21ps, RMS →3.42ps

Phase spacing error

Clock phase (in deg.)	Correct phase	Obtained phase	Phase error
0	3.991897us	Reference	
180 (rising)	3.992097us	3.992051us	46ps
90	3.991997us	3.991999us	2ps
270 (rising)	3.992197us	3.992199us	2ps

IV. CONCLUSION

The focus of this project is to design a 2Gbps speed CDR with high jitter tolerance. A telescopic differential amplifier with low gain is used to implement VCO which improves the lock-in range and make the PLL operate at high frequency. A conventional charge pump is designed and the problems of current mismatch between the charging and discharging current are minimized. This improves the performance and Hogge PD using D flip flop and XOR, and passive loop filters are used to reduce the overall power consumption and improve the system stability. The major jitter contributor block in the proposed system is VCO. The system is simulated in CADENCE 180nm technology and the results obtained shows that the lock-in range is 2496 MHz and maximum lock range of 4.199us with 5mW power consumption.

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