Scientific Journal of Impact Factor (SJIF): e-ISSN (O): 2348-4470

International Journal of Advance Engineering and Research Development

Volume 4, Issue 12, December -2017

A SURVEY OF OPERATIONAL TRANSCONDUCTANCE AMPLIFIER AND ITS TECHNIQUES IN CMOS TECHNOLOGY

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Abstract:*This paper discusses the various types of operational transconductance amplifier designs for the amplification of ECG signals fabricated using CMOS technologies. The Tran conductance amplifier play an important role in Biological signal measuring electronic equipment like EEG Electroencephalography (EEG), Electrocardiography (ECG), and electromyography (EMG) systems which measure the health and activities of brain, heart, Muscle etc. The amplifiers are surveyed based on different techniques used for circuit design and fabrication methodologies. The different techniques such as level shifting, cascading and multistage amplifiers have been used to reduce the power consumption.*

Keywords: *Amplifier, CMOS technology, ECG, EEG, EMG.*

1. Introduction

The field of biomedical signal analysis or processing has advanced to the stage of practical application of signal processing and pattern analysis techniques for efficient and improved noninvasive diagnosis and online monitoring of critical patients. Filtering of power line interference is very essential in the measurement of biomedical events recording, particularly in the case of recording signals as weak as the ECG (clinical tool for investigating the activities of heart). The most common bottlenecks in biomedical signal or event recording are power line interference and baseline drift [1]. The ECG system is portable in the sense, it probably consist of wireless transceiver in the system. The wireless link is connected between the ADC unit and display unit [2]. The universal connectivity allows the system to connect it to a wide range of area. The analog-to-digital conversion is done for the biomedical signals less than 1µw and the ADC consumes only less power. Design of analog front end (AFE) amplifier mainly focuses on power consumption and noise. The use of feedback or loop technique eliminates noise and maintains CMRR to the allowable level.

When harmonics of a certain frequency or some frequency components are coupled into the circuit or the signal transmission line of an instrumentation system, the data acquired may suffer from harmonic interference. The power line interference is a typical type of interference for various types of signals such as biomedical signals. There are basically two components in power line interferences, namely, electric field interference and magnetic field interference. Electric field interference generates spikes at 50/60 Hz frequency, whereas magnetic field interference is generated due to the transformer in the power supply which causes interference and stimulates to generate harmonic frequencies of the fundamental [3].

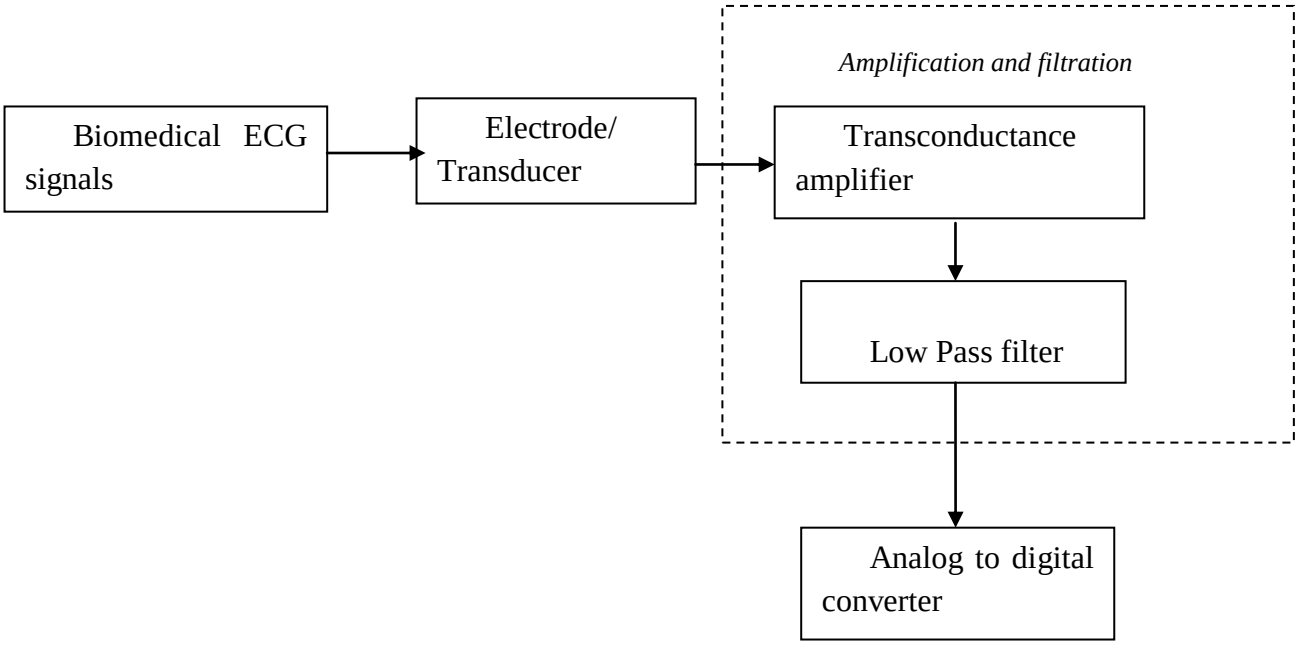

Figure-1: Block diagram of ECG

Adding to this, the sources of these interferences are present in the entire clinic, where a number of biomedical instruments run on AC power line. Hence a physiological signal gets corrupted by power line frequency and its harmonics. The interference may be removed by both digital and analog filtering techniques .Operational amplifiers are the most popular building blocks for analog circuit design. However, op-amp has limitations in bandwidth and slew rate which lead the analog designer to search for other possibilities. Recently operational transconductance amplifier (OTA) has been found to be one of the most significant building blocks in analog signal processing. In high-frequency continuous-time filters, OTA-C filters have often been employed since OTAs provide high bandwidth, high slew rate, and a transconductance gain which can be electronically controlled using a bias current. Hence the circuits developed using OTAs are most likely to possess intrinsic electronic control of parameters such as the cutoff frequency, quality factor, gain of a filter or frequency of oscillation, and the condition of oscillation of an oscillator.

Designing high performance analog integrated circuits in low power applications with reduced channel length devices is becoming increasingly exigent with the relentless trend toward reduced supply voltages. A large part of the success of the MOS transistor is due to the fact that it can be scaled to increasingly smaller dimensions, which results in higher performance. On the other hand for different aspect ratio, there is a trade-off among speed, power, gain and other performance parameters. Thus realization of a CMOS OTA that combines a high linearity, considerable dc gain with high unity gain frequency would be a constraint in circuits and systems design task [4].

As the feature size of CMOS processes reduces, the supply voltage for it also has to be reduced for the reduction of power dissipation per cell. Supply voltage reduction guarantees the reliability of devices as the lower electrical fields inside layers of a CMOS produces less risk to the thinner oxides, which results from device scaling. However, the reduction in supply voltage leads to degraded circuit performance in terms of available bandwidth and voltage swing. Scaling down the threshold voltage of the CMOSs reduces the performance loss (degraded bandwidth, low voltage swing etc.) to some extent but there is increase in the static power dissipation. The performance of digital circuits is improved by scaling but the analog cells benefit marginally because minimum size transistors cannot be used due to noise and offset requirements. To date, with much effort dedicated by analog IC researchers and the continuous scaling down on commercial semiconductor technologies, the reported OTAs can work up to several hundred MHz [5]. The current trends in continual scaling down of transistor gate lengths and reduction in supply voltage have further added to the design challenges of analog circuits. A direct consequence of this has been a performance investigation of transconductance circuits using advanced CMOS process technology. This work deals with the survey of various existing Operational transconductance amplifier techniques in CMOS technology

2. Survey of Operational Transconductance Amplifier:

Currently research studies are focussing on designing high performance analog circuits at reduced power and supply voltage. The transconductance amplifiers remain as the key element in various analog integrated circuits. The realization of the OTA in low power circuits to achieve high DC gain and high gain bandwidth is a difficult task.

The two stage operational transconductance amplifier described by Behzad Razavi (2002) achieves high gain and voltage swing due to the presence of two stages in the circuit. This helps in obtaining good signal to noise ratio and dynamic range. However, this amplifier also requires a miller compensation to maintain stability, which reduces unity gain bandwidth and speed. Yet again, the power consumption is increased due to increased area [6]. So, single stage amplifiers are the best choice to work in reduced voltage and power circuits

Hernes and Sansen (2005) discuss the classification of single stage, two stage and three stage structures based on harmonic distortion. A performance comparison of single stage amplifier and two stage amplifier shows that single stage amplifier works well at high frequency while two stage amplifier is good at mid frequency range. The study also assures that noise level is maintained low for differential amplifiers with an increases in common mode rejection ratio and power supply rejection ratio[7]. The input stage transistors affect the overall operation of a circuit at high frequencies and output transistors at low frequencies.

Palumbo et al (2006) designed the single stage Telescopic OTA structure which proves to achieve high gain and unity gain bandwidth. But, the structure attains less output voltage swing and the input common mode level should be maintained to match the output common mode level. This affects the linearity of the circuit. Furthermore telescopic structures cannot be implemented as a unity gain buffer. This inhibits its performance in practical applications. The performance of a Folded Cascode OTA alleviates the drawbacks of the Telescopic structures and attains comparable gain and unity gain bandwidth with a greater output swing. Additionally, the dynamic range is improved as the input and output common mode level need not to be matched. It can also be easily configured into a unity gain buffer. Thus, the folded cascode architecture remains as a perfect choice in the implementation of a Gm-C filter for communication receivers, despite its disadvantages such as increased power consumption and noise[8].

3. OTA in ECG application:

Mohseni et al presented a bandpass operational amplifier for neural recording with low noise and low power consumption. A gain of 39.3 dB at 1Hz is achieved with two stages of CMOS amplifier in a closed loop resistive feedback circuit. The circuit is implemented with AMI 1.5µm double-poly double-metal n-well CMOS process[9].

Baghini et al[10] designed a chip fabricated with 0.35µm mixed mode CMOS TSMC process to present a three channel low power analog processor for ECG monitoring devices. By using the current balancing technique, analog signal conditioning functions are implemented in the Instrumentation amplifier. With the low power supply of 3V, it achieves CMRR of 100 dB with the gain of 600V.

The amplifier designed by Zhang et al [11] provides low dc offset at the skin electrode interface and also has low power consumption. The IC consists of a low offset op-amp along with a current reference circuit. This design is implemented in SMIC 0.18µm IP6M CMOS technology.

Goel et al's [12] amplifier contains 2 amplifiers at the input and a Folded Cascode amplifier at the output. Gain is increased by the usage of the folded cascade amplifier . It has been implemented in the 0.18µm CMOS technology, providing a gain of 67dB and a CMRR of 92dB. It exhibits power consumption of 263µW, which is lower when compared to other amplifiers also being an ideal condition for bio-medical application.

A CMOS amplifier with differential input and output was designed by Hsia et al[13]. The circuit is implemented in the 0.35µm CMOS technology. 3 stage of amplification has been employed to increase the gain and the CMRR. The first stage provides a high CMRR, second and the third stage have been used to increase the voltage gain. Both the common and the differential modes have been employed to increase the overall performance of the amplifier.

Chuan-Yu et al., (2016) designed a fifth-order Butterworth operational transconductance amplifier-C (OTA-C) low-pass filter (LPF) with multiple-output differential-input (MODI) OTA structure and metal–insulator–metal capacitors for electrocardiography applications. The current division technology is used as an alternative output pair to provide multiple

outputs and achieve high linearity. A MODI OTA-C circuit architecture to reduce power consumption via the system-level derivation described here with the lowpower technique. This technique reduces the number of OTAs of the fifth-order LPF from 11 to 6 as compared with the conventional structure[14]. The design issue of linearity is also considered in the implementation of MODI OTA. The proposed filter is fabricated in a 0.18 µm complementary metal–oxide– semiconductor technology with an area of 0.12 mm^2. The LPF achieved a total harmonic distortion of 49.8 dB under a bandwidth of 50 Hz and input voltage of 86 mVpp at a 1 V supply voltage. The total power dissipation is 350 nW.

Jinghao Feng et al., designed a novel low-power low-noise amplifier for transconductance electrocardiogram (ECG) signal recording applications. The presented circuit contains a chopper-stabilized amplifier and a second-order continuous time Gm-C low pass filter (LPF) using very small Gm OTA. The circuit totally consumes 6.37J.lW with a single supply voltage of 1.2V. It achieves an AC gain of 40dB in mid-band, the input-referred integrated noise of 1.08J.lVrms (0.1Hz-150Hz) and a high common-mode rejection ratio (CMRR) of 130dB in bandwidth[15].

The basic topology using differential input single output OTA is simulated in TSMC 90nm CMOS process technology. The simulation results indicate high bandwidth, greater than 10GHz with 0.721mW power consumption and the transconductance of - 69.78dB. The total harmonic distortion for 100mV input at a frequency of 1MHz is found to be 1.54% [16].

4. Survey of various techniques in OTA:

Guglee [17] proposed operational transconductance amplifier which is the combination of source degeneration using MOS transistor and class AB linearization technique which is based on standard 0.25µm CMOS technology with supply voltage of 1.27V and power consumption of 25µw. The total harmonic distortion (THD) is also low with 60dB at 5MHz for 0.6Vp-p. This type of OTA is suitable for GmC filter implementation.

To reduce the THD, X.Zhu and Y.Sun [18] proposed another modified OTA in 2008 where the total harmonic distortion is brought down below 1% upto 0.85Vpp. As the available voltage headroom becomes limited, many existing circuit techniques in the analog domain cannot be applied. Very often large-gate source voltages are required in order to improve linearity but the supply voltage limit this. So the authors [18] use flipped voltage follower (FVF) to reduce power supply and source degeneration techniques to optimize power consumption and linearity. Here differential pair in the input stage with source degeneration is used and the output stage consists of four current mirrors.

To decrease the transconductance, Jun-Yen Lin, Wein-Hsin Chang and Chung-Chih Hung [19] proposed an OTA design, where the Gm value ranged from 60µS to 130µS. This OTA design combines the techniques of the double differential pairs (DDP) and source degeneration current mirror. As the value of source degeneration resistor R increases, the value of Gm reduces; which implies low operational speed therefore, double differential pair is used to improve linearity. But in DDP, the resistor value must be tuned first, which may lead to degradation of linearity.

Lewinsk et al.,[20] proposed a fifth-order 30-MHz integrated low-pass filter with 65-dB spurious-free dynamic range. The topology is based on an operational transconducatance amplifier (OTA)-C ladder configuration implementing an elliptic transfer function. High linearity and low noise are achieved by using polysilicon resistors and efficient highly linear transconductors based on a proposed nonlinear source degeneration technique. The linearity of a typical source degenerated structure is improved by more than 10 dB while the small-signal transconductance is reduced by less than 1 dB; the additional power needed by the auxiliary circuitry is less than 10% that of the OTA's power, and the noise level increases by no more than 1 dB.

Reetesh V. Golhar et al.,[21] designed highly linear Operational Transconductance Amplifier (OTA) that combines two linearization techniques, one with adaptive biasing of differential pairs and second with resistive source degeneration. The Operational Transconductance Amplifier has ±0.9v power supply. Operational Transconductance Amplifier has been simulated with TANNER 0.18µm CMOS technology.

Song Han et al., [22] A new tunable transconductance amplifier is proposed for the programmable analog signal processing or low power filter applications. The transconductor linearization is based on the compensation of nonlinear behaviour by two MOS transistors. The transconductance amplifier in this brief exhibits the good common-mode dynamic range and the voltage-controlled transconductance.

Morozov et al., [23] proposed a new CMOS transconductance amplifier with low-harmonic distortion The used technique is based on the parallel connection of two amplifiers. The first transconductor is working in the triode region, the

other one is in the saturation. Compared to the known method, the realization of the discussed circuit provides a good value of parameter and lower power consumption. An estimation indicates that 15% power saving can be achieved. A special current-biasing block and large size MOS transistors will not be required.

A design methodology of a CMOS linear transconductor for low-voltage and low-power filters is proposed by Yodprasit et al.,[24]. It is applied to the analog baseband filter used in a transceiver designed for wireless sensor networks. The transconductor linearization scheme is based on regulating the drain voltage of triode-biased input transistors through an active-cascode loop. A third-order Butterworth low-pass filter implemented with this transconductor is integrated in a 0.18µm standard digital CMOS process. The filter can operate down to 1.2-V supply voltage with a cutoff frequency ranging from 15 to 85 kHz. The 1% total harmonic distortion dynamic range measured at 1.5 V for 20-kHz input signal and 50-kHz cutoff frequency is 75 dB, while dissipating 240 W. This linear transconductance leads to better filtration with more consumption of DC voltage.

Soliman et al.,[25] presented the design of an operational transconductance amplifier-C (OTA-C) low-pass filter for a portable Electrocardiogram (ECG) detection system. A fifth-order Butterworth filter using ladder topology is utilized to reduce the effect of component tolerance and to provide a maximally flat response. The proposed filter is based on a novel class AB digitally programmable fully differential OTA circuit. Based on this, PSPICE simulation results for the filter using 0.25-µm technology and operating under ±0.8 V voltage supply results in more harmonic distortion.

Table-1 Comparison of various techniques in terms of power and DC gain

Author	**Technology**	**Technique**	**Power**	**DC gain**
Nguyen and Guglee [17]	0.25µm	Source degeneration and class AB technique	25µW	91dB
X.Zhu and Y.Sun [18]	0.18µm	Source degeneration and flipped voltage follower	11.8mW	68dB
Lin, Chang and Hung [19]	0.18µm	Source degeneration and double differential pairs	1.21mW	49dB
Lewinsk et al.,[20]	0.18 µm	Linearization Technique	27 µW	71dB
Reetesh V. Golhar et al.,[21]	0.15 µm	adaptive biased transconductor	2.14 mW	87dB
Song Han [22]	0.18 µm	balanced transconductance amplifier	10.5mW	77dB
Morozov et al.,[23]	0.8 µm	one-polarity CMOS transconductors	1.21mW	54dB
Yodprasit et al., [24]	0.5 µm	Cascode Transconductor	240 W	75dB

5. Problems identified:

It should have high input impedance. The skin electrode interface has equivalent impedance which may be high within the bandwidth. To be able to transfer the ECG signal without any attenuation, the analog interface should have high input impedance.

It should have a high CMRR to reject common mode interference. This is typically achieved using a fully differential amplifier. However in most fully differential biopotential amplifiers, mismatches degrade the CMRR. In most recent techniques, the current feedback approach has been used to greatly maximize the CMRR of the instrumentation amplifier but there is more consumption of power.

In such systems Operational Transconductance amplifier plays a very important role. They are the main building blocks of analog design but the problem is they consume more power.

The problem is to design a fully integrated ECG instrumentation amplifier which achieves both low noise for enhanced signal detection and low power for continuous monitoring.

6. Conclusion

In this paper a survey of various techniques of OTA in CMOS technology are examined in terms of Power, technology and DC gain. It is very well understood that all methods work well for different purposes. The advantages and disadvantages of these methods are discussed. Various methods have been employed to increase the performance of the amplifiers for biomedical applications. Thus, further research would lead to a high performance Operational Transconductance Amplifier implemented in CMOS technology with increased gain and CMRR along with low power consumption.

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