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Multicoding Techniqe to Reduce Power Dissipation in VLSI:A Review

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Abstract—*CMOS VLSI circuits having profuse number of gates are interconnected with every part to perform the logical manipulation by input signal. The input signal changes from 0 to 1 or vice-versa, it will change and spread via the circuit and results in power disappearing in the circuit. The charging and discharging of parasitic capacitance is main cause of the power dissipation in the circuit, this is dynamic power dissipation in CMOS circuit. Deep Submicron (DSM) is the one of technology to reduce the area of system. The focus is to reduce the area of CMOS VLSI circuit. There are several methods for the reduction of dynamic power dissipation through energy transition in data buses. Among them a novel Multi coding technique for reducing dynamic power dissipation is proposed by reduction in switching activity of self transitions. In this method, the applied input data is coded in five different ways and the coding resulting in maximum reduction in transition activity is selected. Through this coding scheme the average transition activity is reduced. The coding technique gives better results for longer bus width.*

Keywords— *transition activity; dynamic power dissipation; self transitions; on-chip bus.*

I. INTRODUCTION

In many digital processors power consumption in the bus is a major part of overall power dissipation. Several bus encoding techniques have been proposed from time to time to reduce the power consumption[1,2,3].The two types of power dissipation is presented such as Dynamic power dissipation and Static power dissipation. In this paper, the focus is on Dynamic power dissipation. The capacitance of interconnect can be classified as coupling capacitance and self capacitance. The coupling capacitance is the capacitance between the adjacent data lines while the self capacitance refers to the capacitance between the substrate and the wire itself [7].The dynamic power in VLSI chip decides the behavior of chip and is highly dependent on the load capacitance and the coupling capacitance i.e. bus line signal transitions [6]. Dynamic power dissipation on a coded bus is defined as shown in Fig. 1

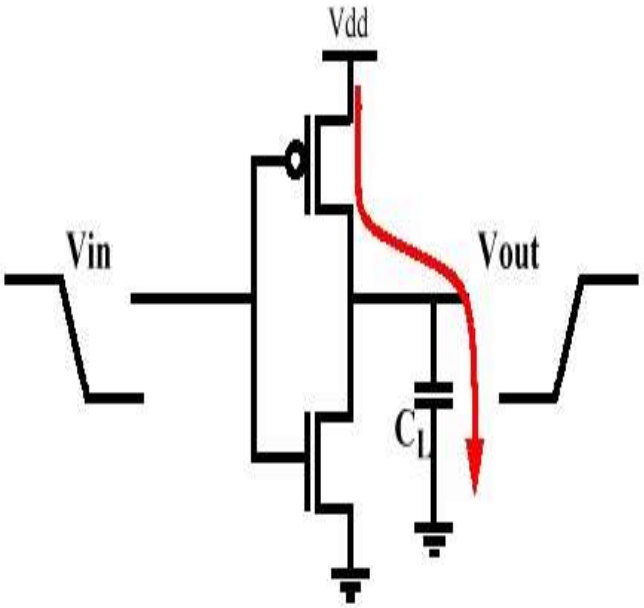

Fig. 1- CMOS circuit

During switching, either from '**0**' to '**1**' or, alternatively, from '**1**' to '**0**', both nMOS and pMOS transistors are ON for a short period of time. This result in a short current pulse from V_{DD} to V_{SS}. Current is also required to charge and discharge the output capacitive load. This latter term is usually the dominant term. The current pulse from V_{DD} to V_{SS} results in a 'short-circuit' dissipation that is dependent on the input rise/fall time, the load capacitance and the gate design.

$$P_{dynamic}=\alpha*V_{DD}*C_L*f \quad \ldots(1)$$

Where,
V_{DD} is the supply voltage,
C_L is the load capacitance,
f is the clock frequency,
$\alpha=\alpha_s*C_s + \alpha_c*C_c$
α_s is the self transition activity factor and
α_c is the coupling transition factor.

This paper provides the information on previous techniques which are used to implement the coding technique to low power dissipation in years as well as the proposed system which is useful in low power dissipation as compare to previous. This paper has been organized as follows. In section II, basic definition is given. In section III, literature reviews are discussed. Section IV gives a detailed of proposed system. In section V, results are discussed. Finally, conclusions are presented in section VI.

II. BESIC DEFINITION

1. **Coupling transitions**: Transition of data from 0 1 or vice versa between adjacent bus lines.
2. **Self transitions**: Transition of data from 0 to 1 or vice-versa on bus wire with reference to previous data on it.
3.**Bus width**: Number of bits in data is defined as bus width.

III. LITERATURE REVIEW

Many works have been concentrated on low power bus coding techniques. Quadro coding technique is used to reduce power dissipation[1]. Four type of coding are completed by using even and odd position of given data. Crosstalk reduction is done by using But-Invert coding[2]. These processes are complete by using one control bit. Making partition into two sub buses, then encode only one sub bus while leaving and remaining encode[3].In Bus-Invert coding the hamming distance is larger than half of the bus width, in that pattern is transmitted with each bit inverted. Rearrange the data by their position with respect to total number[4]. For 4-bit bus model the Coditional coded block ware used for coding[5]. There are tow types of the process such as Canonic Sign Digit and Binary Coded Canonic Sign Digit.The design of CMOS is genrated this bus is simply a circuit that connects one part of the circuit to the other[6,8]. A bus may consist of set of parallel lines with repeaters between them. Butterfly structure of FFT is design is genrated and using of Canonic Sign Digit and Banary Coded Canonic Sign Digit was coded[7].

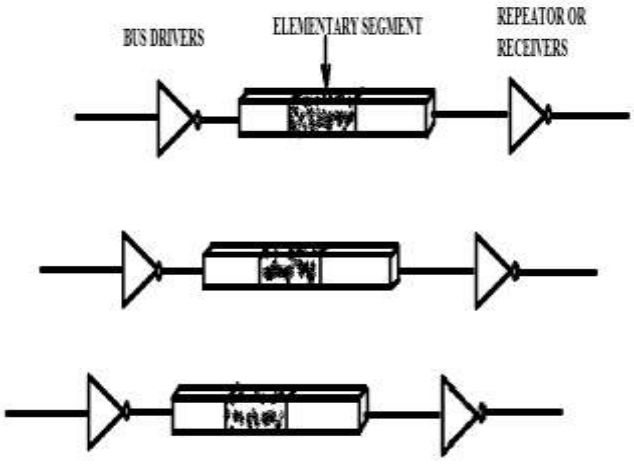

Fig. 2 –DSM Bus [8]

Octo coding was done for reducing the power dissipation and area[9]. Bus coding are used for reducing the power dissipation[10]. The extra line was added in the given line for coding, by this the power will be reduced and area also reduce.

IV. PROPOSED SYSTEM

The proposed technique is called Multi coding technique is based on reducing the number of transitions occurring on data bus when a new data is to be transmitted. By using the following technique self transitions from 0-1 and 1-0can be reduced as new data is sent on the data bus compared to previous data. Let the data be n bits wide. The proposed coding technique is given as follows:

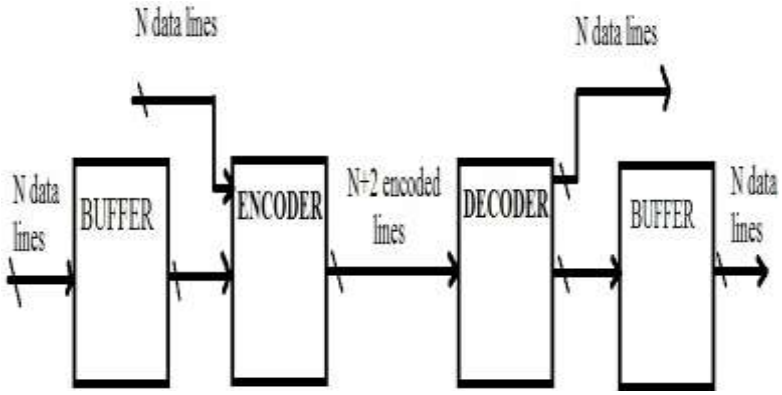

Fig. 2 –Block diagram of complete system

There two process to complete this such as encoding and decoding.

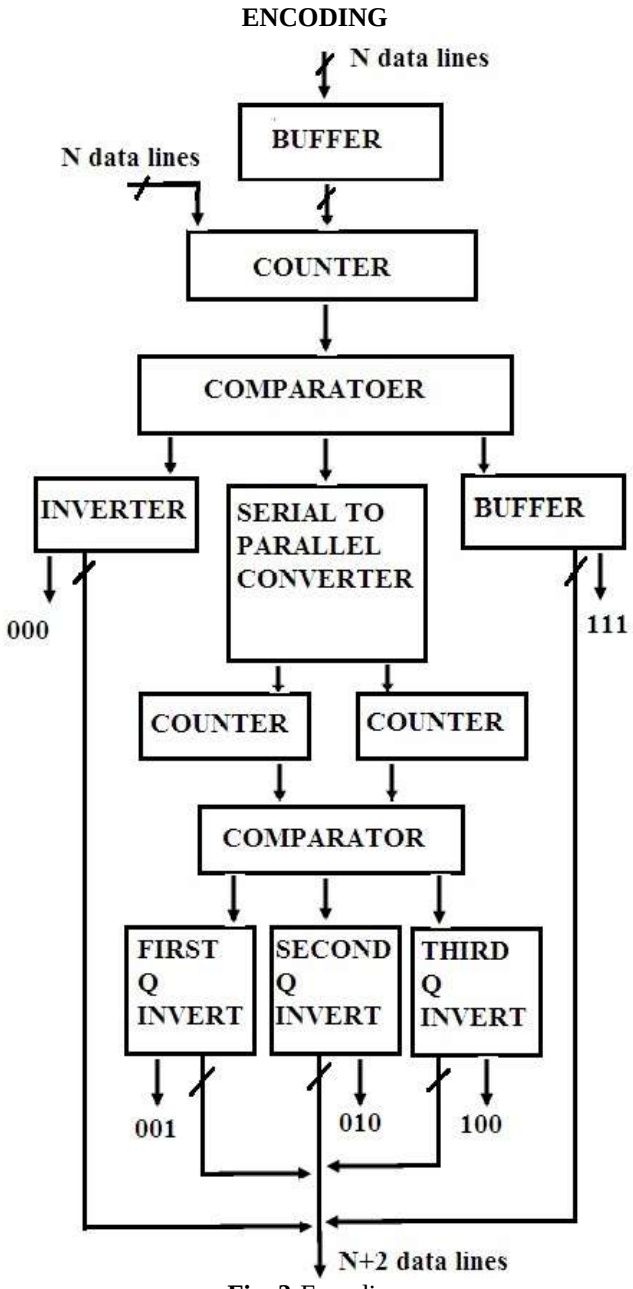

Fig. 3-Encoding

STEP 1:
Calculate number of transitions of the present bus data as compared to previous bus data.
STEP 2:
If the number of transitions >n/2 then revert the data to be sent and add it with '000' as control bits for decoding purpose.
STEP 3:
If the number of transitions <=n/2 and >n/4 then
Divide into three groups by using binary tree
First quadrant: AF1,AF2,AF3,….
Second Quadrant: BS1,BS2,BS3,…..
Third quadrant: CT1,CT2,CT3,….
Calculate number of transitions between First Quadrant of group of present data with the previous data, say FQGT then number of transitions between Second Quadrant of present data with previous data, say SQGT and number of transitions between Third Quadrant group of present data with the previous data, say TQGT.
If FQGT>SQGT and FQGT>TQGT then
Invert the data bits of First Quadrant and add it with control bit '001'.
Else if SQGT>FQGT and SQGT > TQGT then
Invert the data bits of Second Quadrant and add it with control bit '010'.
Else
Invert the data bits of Third Quadrant and add it with control bit '100'.
STEP 4:
If the number of transition <=n/4 then send the data as it is without any encoding and add it with '111'.

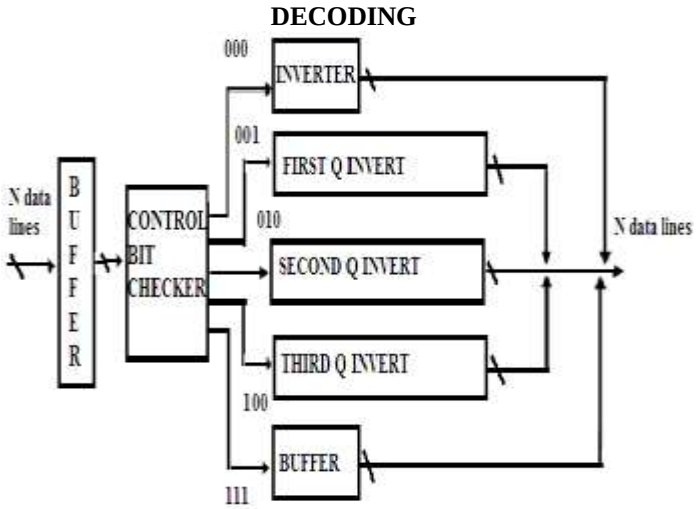

Fig. 4-Decoding

For decoding the data from the encoded data, control bits are recovered from the received data and the following operations are performed according to the control bits. **Table I** shows operation to be performed on data bits for decoding. Decoding is performed by adopting exactly opposite sequence of steps of encoding.

Table I. DECODING PROCESS EXPLANATION ACCORDING TO THE VALUS OF CONTROL BITS.

Control bits	Operation to be performed
000	Invert the receive data
001	Invert the data bits of First Quadrant
010	Invert the data bits of Second Quadrant
100	Invert the data bits of Third Quadrant
111	Data remains same

V. CONCLUSION

This paper presents the summary of various techniques of coding to reduce transitions. These techniques are elaborately discussed in the paper. In the proposed system, one of the most preferable technique multi coding is used to reduce the self transitions in CMOS. So many work are completed on the power dissipation as compare to all of this the recently power has reduce up to 36% for 9 bit bus. At 8 bit bus power saving from 47% to 25%.

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