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Implementation of a New Control Strategy for Diode-Clamped Multilevel Inverter in Distributed Generation

K.Mounika Yadav[1], Mr.K.Sudheer Kumar[2]

[1]EEE Dept, LBRCE
[2]EEE Dept, LBRCE

Abstract- *This paper presents a new control strategy for three phase inverter in distributed generation. This paper analyses a new NPC technique based three phase inverter with grid connected system. The proposed control strategy that enables both islanded and grid-tied operations of three phase inverter in DG. In addition the control strategy composes of an inner inductor current loop, and a novel voltage loop in the synchronous reference frame. The inverter is regulated as a current source just by the inner inductor current loop in grid-tied operation, and the voltage controller is automatically activated to regulate the load voltage upon the occurrence of islanding. The NPC inverter needs a neutral DC terminal which is provided by a buck converter. To review the effectiveness of the proposed system, the waveforms of the grid current and the load voltage are distorted under non-linear local load with the conventional strategy. Finally, the effectiveness of the proposed control strategy is validated by the simulation results using MATLAB/SIMULINK software*

Keywords-*Buck converter, Distributed generation (DG), islanding, load current, NPC (Neutral point clamped), seamless transfer.*

I.INTRODUCTION

Nowadays renewable energy resources are being widely used for power generation, such as wind turbines, fuel cells, micro-turbines, photovoltaic arrays etc [1], [3]. Most of these resources are connected to the utility through power electronic interfacing converters, i.e., three-phase inverter. Moreover, DG is a suitable form to offer high reliable electrical power supply, as it is able to operate either in the grid-tied mode or in the islanded mode [2].

In the grid-tied operation, DG deliveries power to the utility and the local critical load. Upon the occurrence of utility outage, the islanding is formed. Under this circumstance, the DG must be tripped and cease to energize the portion of utility as soon as possible according to IEEE Standard 929-2000 [4]. However, in order to improve the power reliability of some local critical load, the DG should disconnect to the utility and continue to feed the local critical load [5]. The load voltage is key issue of these two operation modes, because it is fixed by the utility in the grid-tied operation, and formed by the DG in the islanded mode, respectively. Therefore, upon the happening of lonely i.e., islanding, DG must take over the load voltage as soon as possible, in order to reduce the transient in the load voltage.

Droop-based control is used widely for the power sharing of parallel inverters [9], [10], which is called as voltage mode control in this paper, and it can also be applied to DG to realize the power sharing between DG and utility in the grid-tied mode [11]. In this situation, the inverter is always regulated as a voltage source by the voltage loop, and the quality of the load voltage can be guaranteed during the transition of operation modes. However, the limitation of this approach is that the dynamic performance is poor, because the bandwidth of the external power loop, realizing droop control, is much lower than the voltage loop. Moreover, the grid current is not controlled directly, and the issue of the inrush grid current during the transition from the islanded mode to the grid-tied mode always exists, even though phase locked loop (PLL) and the virtual inductance are adopted. In the hybrid voltage and current mode control, there is a need to switch the controller when the operation mode of DG is changed. During the interval from the occurrence of utility outage and switching the controller to voltage mode, the load voltage is neither fixed by the utility, nor regulated by the DG, and the length of the time interval is determined by the islanding detection process. Therefore, the main issue in this approach is that it makes the quality of the load voltage heavily reliant on the speed and accuracy of the islanding detection method [6]-[8].

This paper proposes a unified control strategy that avoids the aforementioned shortcomings. First, the traditional inductor current loop is employed to control the Neutral point clamped (NPC) inverter with a buck converter which gives neutral point in the dc voltage in DG to act as a current source with a given reference in the synchronous reference frame (SRF). Second, a novel voltage controller is presented to supply reference for the inner inductor current loop, where a proportional-plus-integral (PI) compensator and a proportional (P) compensator are employed in D-axis and Q-axis, respectively.

In the grid-tied operation, the load voltage is dominated by the utility, and the voltage compensator in D- axis is saturated, while the output of the voltage compensator in Q-axis is forced to be zero by the PLL. Therefore, the reference of the inner current loop cannot regulated by the voltage loop, and the DG is controlled as a current source just by the inner current loop. Upon the occurrence of the grid outage, the load voltage is no more determined by the utility, and the voltage controller is automatically activated to regulate the load voltage. These happen naturally, and, thus the proposed

control strategy does not need a forced switching between two distinct sets of controllers. Further, there is no need to detect the islanding quickly and accurately, and the islanding detection method is no more critical in this approach.

Moreover, the proposed control strategy, benefiting from just utilizing the current and voltage feedback control, endows a better dynamic performance, compared to the voltage mode control. Third, the proposed control strategy is enhanced by introducing a unified load current feed forward, in order to deal with the issue caused by the nonlinear local load, and this scheme is implemented by adding the load current into the reference of the inner current loop. In the grid-tied mode, the DG injects harmonic current into the grid for compensating the harmonic component of the grid current, and thus, the harmonic component of the grid current will be mitigated.

II. PROPOSED CONTROL STRATEGY

A. Power Stage

This paper presents a new control strategy for a three-phase neutral point clamped inverter in DG to operate in both islanded and grid-tied modes. Here the NPC inverter was also called the diode-clamped inverter because when it was first used in a three-level inverter the mid-voltage level was defined as the neutral point level. The schematic diagram of the DG based on the proposed control strategy is shown by Fig. 1. The DG is equipped with a three-phase interface inverter terminated with a LC filter. The primary energy is converted to the electrical energy, which is then converted to dc by the front-end power converter, and the output dc voltage is regulated by it. Therefore, they can be represented by the dc voltage source Vdc in Fig. 1. In the ac side of inverter, the local critical load is connected directly.

It should be noted that there are two switches, denoted by Su and Si respectively in Fig. 1, and their functions are different. The inverter transfer switch Si is controlled by the DG, and the utility protection switch Su is governed by the utility. When the utility is normal, both switches Si and Su are ON, and the DG in the grid-tied mode injects power to the utility. When the utility is in fault, the switch Su is tripped by the utility instantly, and then the islanding is formed. After the islanding has been confirmed by the DG with the islanding detection scheme [5]-[7], the switch Si is disconnected, and the DG is transferred from the grid-tied mode to the islanded mode. When the utility is restored, the DG should be resynchronized with the utility first, and then the switch Si is turned ON to connect the DG with the grid.

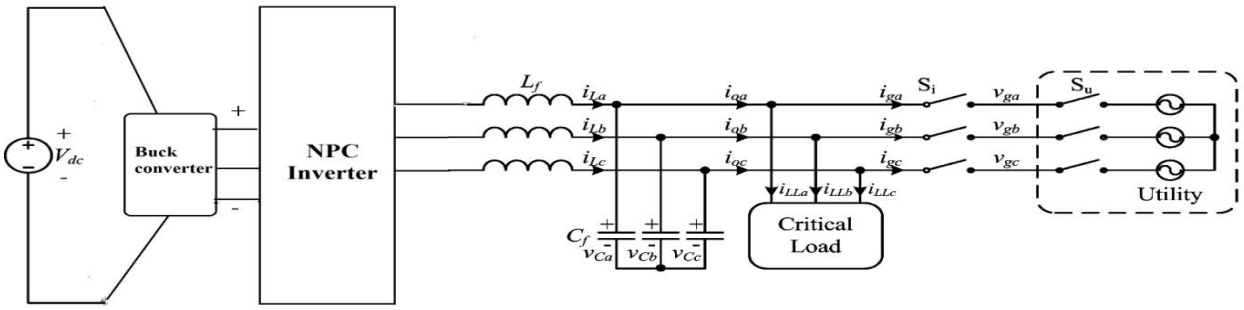

Fig.1. Schematic diagram of the DG based on the proposed control strategy.

B. Basic Idea

With the hybrid voltage and current mode control [12]-[13], the inverter is controlled as a current source to generate the reference power (PDG + jQDG) in the grid-tied mode. And its output power (PDG + jQDG) should be the sum of the power injected to the grid Pg + jQg and the load demand Pload + jQload , which can be expressed as follows by assuming that the load is represented as a parallel RLC circuit.

$$\text{pload} = \frac{3}{2}\frac{v_m^2}{R} \qquad (1)$$

$$\text{Qload} = \frac{3}{2}V_m^2\left(\frac{1}{\omega L} - \omega C\right) \qquad (2)$$

In (1) and (2), Vm and ω represent the amplitude and frequency of the load voltage, respectively. When the nonlinear local load is fed, it can still be equivalent to the parallel RLC circuit by just taking account of the fundamental component. During the time interval from the instant of islanding happening to the moment of switching the control system to voltage mode control, the load voltage is neither fixed by the utility nor regulated by the inverter, so the load voltage may drift from the normal range [6]. And this phenomenon can be explained as below by the power relationship. During this time interval, the inverter is still controlled as a current source, and its output power is kept almost unchanged.

However, the power injected to utility decreases to zero rapidly, and then the power consumed by the load will be imposed to the output power of DG. If both active power Pg and reactive power Qg injected into the grid are positive in the grid-tied mode, then Pload and Qload will increase after the islanding happens, and the amplitude and frequency of the load voltage will rise and drop, respectively, according to (1) and (2). With the previous analysis, if the output power

of inverter PDG + jQDG could be regulated to match the load demand by changing the current reference before the islanding is confirmed, the load voltage excursion will be mitigated. And this basic idea is utilized in this paper.

In the proposed control strategy, the output power of the inverter is always controlled by regulating the three-phase inductor current iLabc , while the magnitude and frequency of the load voltage VCabc are monitored. When the islanding happens, the magnitude and frequency of the load voltage may drift from the normal range, and then they are controlled to recover to the normal range automatically by regulating the output power of the inverter.

C. Control Scheme

The overall block diagram for the proposed unified control strategy was described in Fig 2. Here the inductor current iLabc, the utility voltage vgabc , the load voltage VCabc, and the load current iLLabc are sensed. And the three-phase neutral point clamped inverter is controlled in the SRF, in which, three phase variable will be represented by dc quantity. The control diagram is mainly composed by the inductor current loop, the PLL, and the current reference generation module.

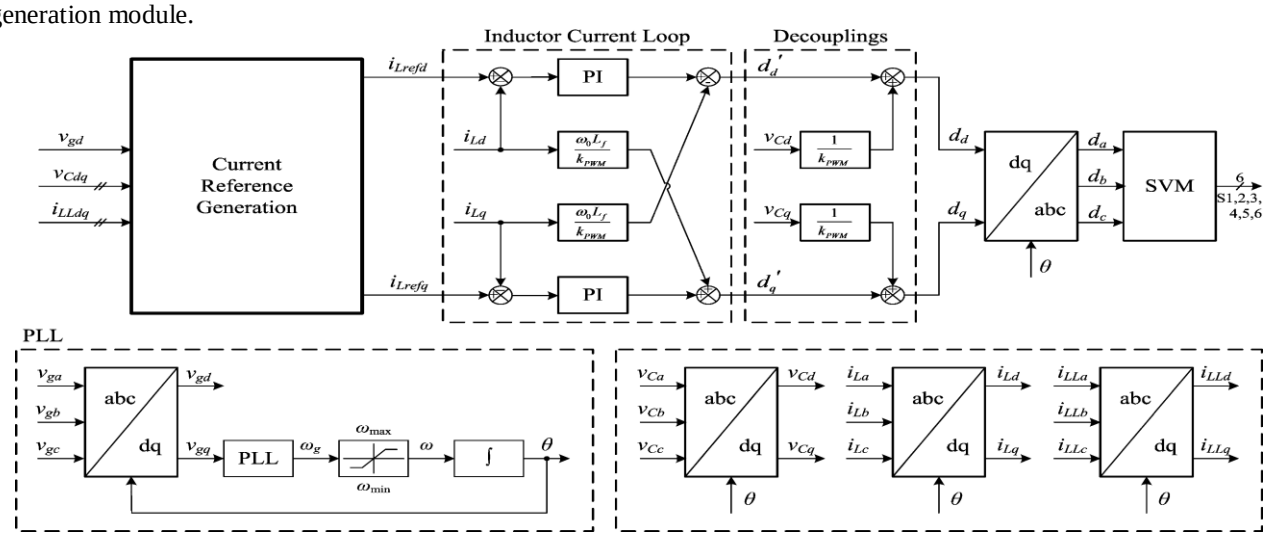

Fig. 2. Overall block diagram of the proposed unified control strategy.

In the inductor current loop, the PI compensator is employed in both D- and Q-axes, and a decoupling of the cross coupling denoted by $_{O}$Lf /kPWM is implemented in order to mitigate the couplings due to the inductor. The output of the inner current loop ddq ′, together with the decoupling of the capacitor voltage denoted by 1/kPWM, sets the reference for the standard space vector modulation that controls the switches of the three-phase NPC inverter. It should be noted that kPWM denotes the voltage gain of the inverter, which equals to half of the dc voltage in this paper.

The PLL in the proposed control strategy is based on the SRF PLL [14], [15], which is widely used in the three-phase power converter to estimate the utility frequency and phase. Furthermore, a limiter is inserted between the PI compensator GPLL and the integrator, in order to hold the frequency of the load voltage within the normal range in the islanded operation. In Fig. 2, it can be found that the inductor current is regulated to follow the current reference iLref dq , and the phase of the current is synchronized to the grid voltage Vgabc .If the current reference is constant, the inverter is just controlled to be a current source, which is the same with the traditional grid-tied inverter.

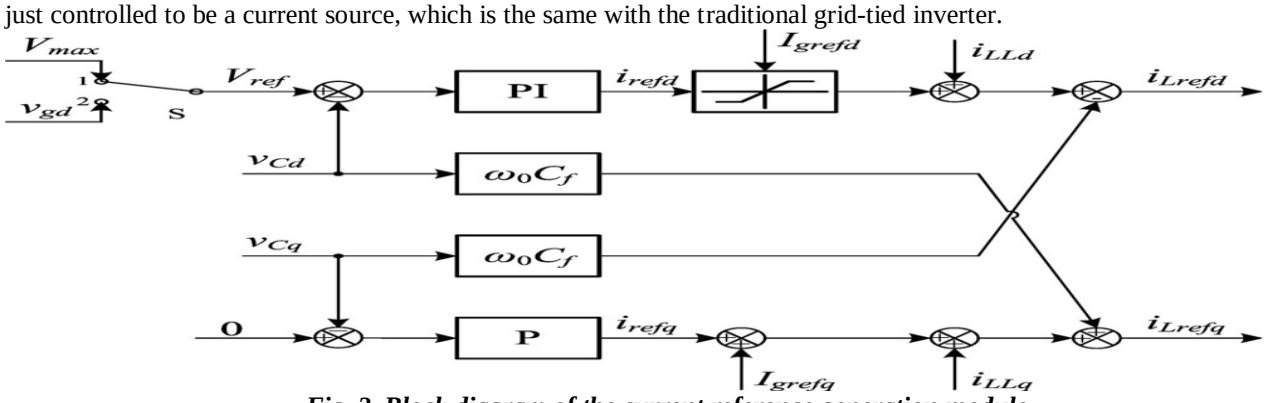

Fig. 3. Block diagram of the current reference generation module.

The new part in this paper is the current reference generation module shown in Fig. 2, which regulates the current reference to guarantee the power match between the DG and the local load and enables the DG to operate in the islanded mode. Moreover, the unified load current feed-forward, to deal with the nonlinear local load, is also

implemented in this module. The block diagram of the proposed current reference generation module is shown in Fig. 3, which provides the current reference for the inner current loop in both grid-tied and islanded modes. In this module, it can be found that an unsymmetrical structure is used in D- and Q-axes. The PI compensator is adopted in D-axes, while the P compensator is employed in Q-axis. Besides, an extra limiter is added in the D-axis. More-over, the load current feedforward is implemented by adding the load current iLLdq to the final inductor current reference iLref dq . The benefit brought by the unique structure in Fig. 3 can be represented by two parts: 1) seamless transfer capability without critical islanding detection; and 2) power quality improvement in both grid-tied and islanded operations. The current reference iLredq composes of four parts in D- and Q-axes respectively:

1) the output of voltage controller iref dq ;
2) the grid current reference Igref dq ;
3) the load current iLLdq ; and
4) the current flowing through the filter capacitor Cf .

In the grid-tied mode, the load voltage Vcdq is clamped by the utility. The current reference is irrelevant to the load voltage, due to the saturation of the PI compensator in D-axis, and the output of the P compensator being zero in Q-axis, and thus, the inverter operates as a current source. Upon occurrence of islanding, the voltage controller takes over automatically to control the load voltage by regulating the current reference, and the inverter acts as a voltage source to supply stable voltage to the local load; this relieves the need for switching between different control architectures. Another distinguished function of the current reference generation module is the load current feed-forward. The sensed load current is added as a part of the inductor current reference iLref dq to compensate the harmonic component in the grid current under nonlinear local load. In the islanded mode, the load current feed-forward operates still, and the disturbance from the load current, caused by the nonlinear load, can be suppressed by the fast inner inductor current loop, and thus, the quality of the load voltage is improved The inductor current control in Fig. 2 was proposed in previous publications for grid-tied operation of DG [16], and the motivation of this paper is to propose a unified control strategy for DG in both grid-tied and islanded modes, which is represented by the current reference generation module in Fig. 3. The contribution of this module can be summarized in two aspects. First, by introducing PI compensator and P compensator in D-axis and Q-axis respectively, the voltage controller is inactivated in the grid-tied mode and can be automatically activated upon occurrence of islanding. Therefore, there is no need for switching different controllers or critical islanding detection, and the quality of the load voltage during the transition from the grid-tied mode to the islanded mode can be improved. The second contribution of this module is to present the load current feed-forward to deal with the issue caused by the nonlinear local load, with which, not only the waveform of the grid current in grid-tied is improved, but also the quality of the load voltage in the islanded mode is enhanced. Besides, it should be noted that a three-phase unbalanced local load cannot be fed by the DG with the proposed control strategy, because there is no flow path for the zero sequence current of the unbalanced load, and the regulation of the zero sequence current is beyond the scope of the proposed control strategy.

III. OPERATION PRINCIPLE OF DG

The operation principle of DG with the proposed unified control strategy will be illustrated in detail in this section, and there are in total four states for the DG, including the grid-tied mode, transition from the grid-tied mode to the islanded mode, the islanded mode, and transition from the islanded mode to the grid-tied mode.

A. Grid-Tied Mode

When the utility is normal, the DG is controlled as a current source to supply given active and reactive power by the inductor current loop, and the active and reactive power can be given by the current reference of D- and Q-axis independently. First, the phase angle of the utility voltage is obtained by the PLL, which consists of a Park transformation expressed by (3), a PI compensator, a limiter, and an integrator.

$$\begin{pmatrix} x_d \\ x_q \end{pmatrix} = \frac{2}{3}\begin{pmatrix} \cos\theta & \cos\left(\theta - \frac{2}{3}\pi\right) \cos\left(\theta + \frac{2}{3}\pi\right) \\ -\sin\theta & -\sin\left(\theta - \frac{2}{3}\pi\right) - \sin\left(\theta + \frac{2}{3}\pi\right) \end{pmatrix} \times \begin{pmatrix} x_a \\ x_b \\ x_c \end{pmatrix} \quad (3)$$

Second, the filter inductor current, which has been transformed into SRF by the Park transformation, is fed back and compared with the inductor current reference iLref dq , and the inductor current is regulated to track the reference iLref dq by the PI compensator GI .The reference of the inductor current loop iLref dq seems complex and it is explained as below. It is assumed that the utility is stiff, and the three-phase utility voltage can be expressed as

$$\begin{cases} v_{ga} = V_g \cos\theta^* \\ v_{gb} = V_g \cos\left(\theta^* - \frac{2}{3}\pi\right) \\ v_{gc} = V_g \cos\left(\theta^* + \frac{2}{3}\pi\right) \end{cases} \quad (4)$$

Where, Vg = magnitude of the grid voltage, and θ∗ = actual phase angle. By the Park transformation, the utility voltage is transformed into the SRF, which is shown as,

$$v_{gd} = V_g \cos(\theta^* - \theta), v_{gq} = V_g \sin(\theta^* - \theta) \quad (5)$$

Where, Vgq is regulated to zero by the PLL, so Vgd equals the magnitude of the utility voltage Vg . As the filter capacitor voltage equals the utility voltage in the gird-tied mode, Vcd equals the magnitude of the utility voltage Vg and Vcq equals zero, too. In the *D*-axis, the inductor current reference iLref d can be expressed by (6) according to Fig. 3

$$i_{Lrefdq} = I_{grefd} + i_{LLd} - \omega_s C_f \cdot v_{Cq} \quad (6)$$

The first part is the output of the limiter. It is assumed that the given voltage reference Vmax is larger than the magnitude of the utility voltage V_{Cd} in steady state, so the PI compensator, denoted by G_{VD} in the following part, will saturate, and the limiter outputs its upper value Igref d.

The second part is the load current of D-axis iLLd, which is determined by the characteristic of the local load. The third part is the proportional part $-\omega 0Cf \cdot V_{Cq}$, where ω0 is the rated angle frequency, and C_f is the capacitance of the filter capacitor. It is fixed as V_{Cq} depends on the utility voltage. Consequently, the current reference iLref d is imposed by the given reference Igref d and the load current iLLd, and is independent of the load voltage. In the Q-axis, the inductor current reference iLref q consists of four parts as,

$$i_{Lref\,q} = v_{Cq} \cdot k_{Gvq} I_{gref\,q} + i_{LL\,q} + \omega_s C_f \cdot v_{Cd} \quad (7)$$

where kGvq is the parameter of the P compensator, denoted by G_{VQ} in the following part. The first part is the output of G_{VQ}, which is zero as the V_{Cq} has been regulated to zero by the PLL. The second part is the given current reference Igrefq , and the third part represents the load current in Q-axis. The final part is the proportional part $-\omega 0Cf \cdot V_{Cd}$, which is fixed since V_{Cd} depends on the utility voltage. Therefore, the current reference iLref q cannot be influenced by the external voltage loop and is determined by the given reference Igref q and the load current iLLq .

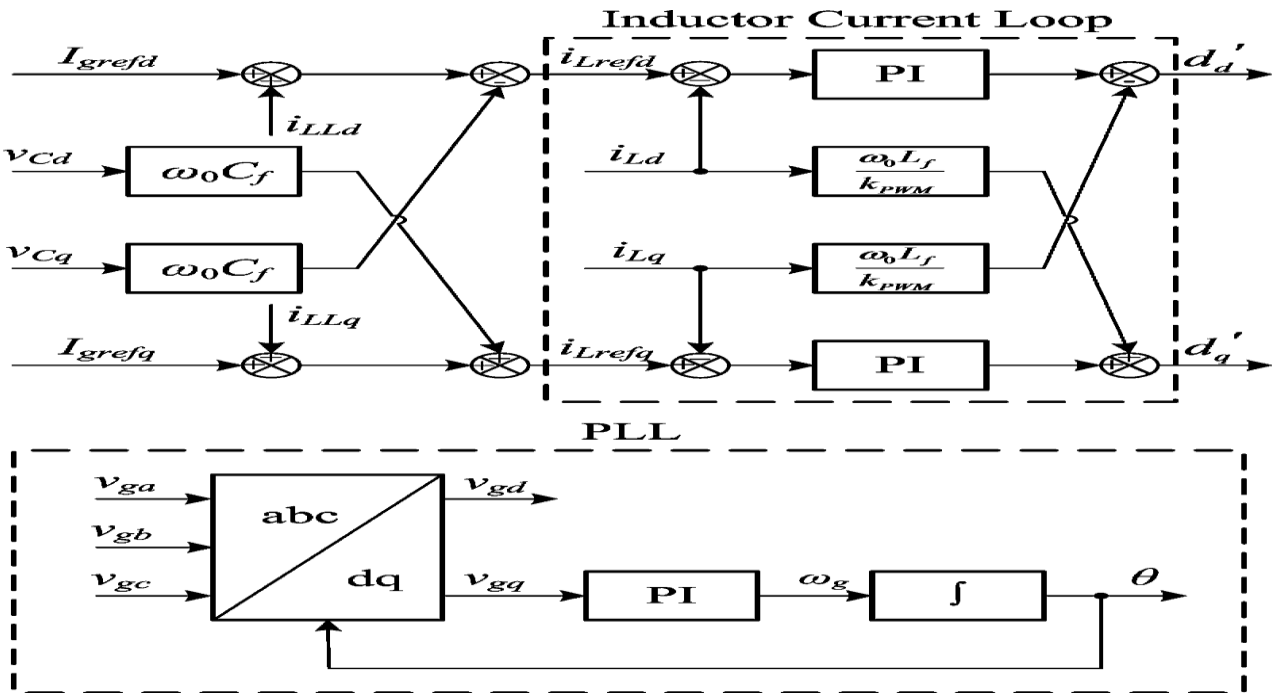

Fig. 4. Simplified block diagram of the unified control strategy when DG operates in the grid-tied mode.

With the previous analysis, the control diagram of the inverter can be simplified as Fig. 4 in the grid-tied mode, and the inverter is controlled as a current source by the inductor current loop with the inductor current reference being determined by the current reference Igref dq and the load current iLLdq . In other words, the inductor current tracks the current reference and the load current. If the steady state error is zero, Igref dq represents the grid current actually, and this will be analyzed in the next section.

A. Transition From the Grid-Tied Mode to the Islanded Mode

In the grid-tied mode, it is assumed that the DG injects active and reactive power into the utility, which can be expressed by (8) and (9), and that the local critical load, shown in (10), represented by a series connected RLC circuit with the lagging power factor.

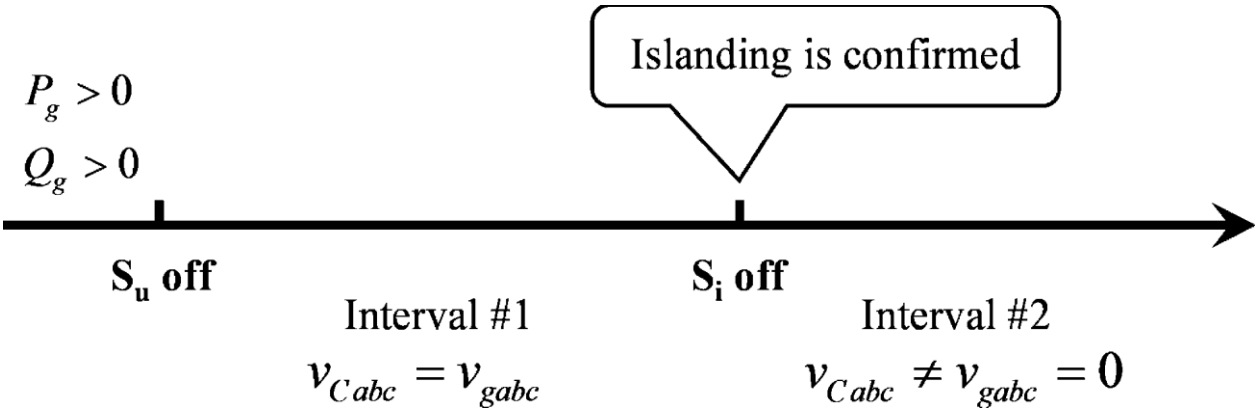

Fig. 5. Operation sequence during the transition from the grid-tied mode to the islanded mode

$$P_g = \frac{3}{2} \cdot (v_{Cd} i_{gd} + v_{Cq} i_{gq}) = \frac{3}{2} v_{Cd} i_{gd} \qquad (8)$$

$$Q_g = \frac{3}{2} \cdot (v_{Cq} i_{gd} - v_{Cd} i_{gq}) = -\frac{3}{2} v_{Cd} i_{gq} \qquad (9)$$

$$\begin{aligned} Z_{\text{sload}} &= R_s + j\omega L_s + \frac{1}{j\omega C_s} \\ &= R_s + j\left(\omega L_s - \frac{1}{\omega C_s}\right) \\ &= R_s + jX_s. \end{aligned} \qquad (10)$$

When islanding happens, igd will decrease from positive to zero, and igq will increase from negative to zero. At the same time, the load current will vary in the opposite direction. The load voltage in D- and Q-axes is shown by (11) and (12), and each of them consists of two terms. It can be found that the load voltage in D-axis V_{Cd} will increase as both terms increase. However, the trend of the load voltage in Q-axis V_{Cq} is uncertain because the first term decreases and the second term increases, and it is not concerned for a while,

$$v_{Cd} = i_{LLd} \cdot R_s - i_{LLq} \cdot X_s \qquad (11)$$

$$v_{Cq} = i_{LLq} \cdot R_s + i_{LLd} \cdot X_s \qquad (12)$$

With the increase of the load voltage in D-axis V_{Cd}, when it reaches and exceeds Vmax, the input of the PI compensator G_{VD} will become negative, so its output will decrease. Then, the output of limiter will not imposed to Igref d any longer, and the current reference iLref d will drop. With the regulation of the inductor current loop, the load current in D-axis i_{LLd} will decrease. As a result, the load voltage in D-axis V_{Cd} will drop and recover to V_{max}.

B. Islanded Mode

In the islanded mode, switching Si and Su are both in OFF state. The PLL cannot track the utility voltage normally, and the angle frequency is fixed. In this situation, the DG is controlled as a voltage source, because voltage compensator G_{VD} and G_{VQ} can regulate the load voltage V_{Cdq}. The voltage references in D and Q-axis are Vmax and zero, respectively. And the magnitude of the load voltage equals to Vmax approximately, which will be analyzed in Section IV. The load current i_{LLdq} is partial reference of the inductor current loop. So, if there is disturbance in the load current, it will be suppressed quickly by the inductor current loop, and a stiff load voltage can be achieved.

C. Transition From the Islanded Mode to the Grid-Tied Mode

If the utility is restored and the utility switch Su is ON, the DG should be connected with utility by turning on switch Si . However, several preparation steps should be performed before turning on switch Si . First, as soon as utility voltage is restored, the PLL will track the phase of the utility voltage. As a result, the phase angle of the load voltage V_{Cabc} will follow the grid voltage Vgabc. If the load voltage V_{Cabc} is in phase with the utility voltage, Vgd will equal the magnitude of the utility voltage according to (5). Second, as the magnitude of the load voltage Vmax is larger than the utility voltage magnitude Vg , the voltage reference Vref will be changed to Vg by toggling the selector S from terminals 1 to 2. As a result, the load voltage will equal to the utility voltage in both phase and magnitude. Third, the switch Si is turned on, and the selector S is reset to terminal 1. In this situation, the load voltage will be held by the utility. As the voltage reference Vref equals Vmax, which is larger than the magnitude of the utility voltage Vg, so the PI compensator $G_{V\,D}$ will saturate, and the limiter outputs its upper value Igref d. At the same time, V is regulated to zero by the PLL according to (5), so the output of G_{VQ} will be zero. Consequently, the voltage regulators G_{VD} and G_{VQ} are inactivated, and the DG is controlled as a current source just by the inductor current loop.

IV. ANALYSIS AND DESIGN

The conventional three-phase inverter with control strategy is analyzed and designed in both steady state and transient state in the reference paper [17]. So in this section a new Neutral point clamped (NPC) with a buck converter is designed to achieve maximum efficiency. NPC inverter needs a three input terminals namely positive dc, negative dc and a neutral dc terminal and these three terminal are provided by a buck convert which bring a neutral terminal along with two output dc terminals.

A. Buck converter

Buck converter which acts as a voltage balancer is shown in Fig. 6, in which a neutral line is built by using a voltage balancer achieving two same voltage levels for requirements of different types of loads, such as unbalanced loads, half-bridge converter and inverter, and so on.

The proposed voltage balancer—a dual-buck half-bridge voltage balancer—is shown in Fig. 6, which is made up of a left bridge leg (S1,D1, L1), a right bridge leg (S2,D2, L2),and a neutral line LN usually connected to the earth ground.

If the conventional driving technology is adopted between the switches S1 and S2, the two-inductor currents iL1 and iL2 will always exist during a switching period, and the unbalanced load current value (iRLoad2 − iRLoad1) is equal to the different value between the current average value iL1 and iL2.

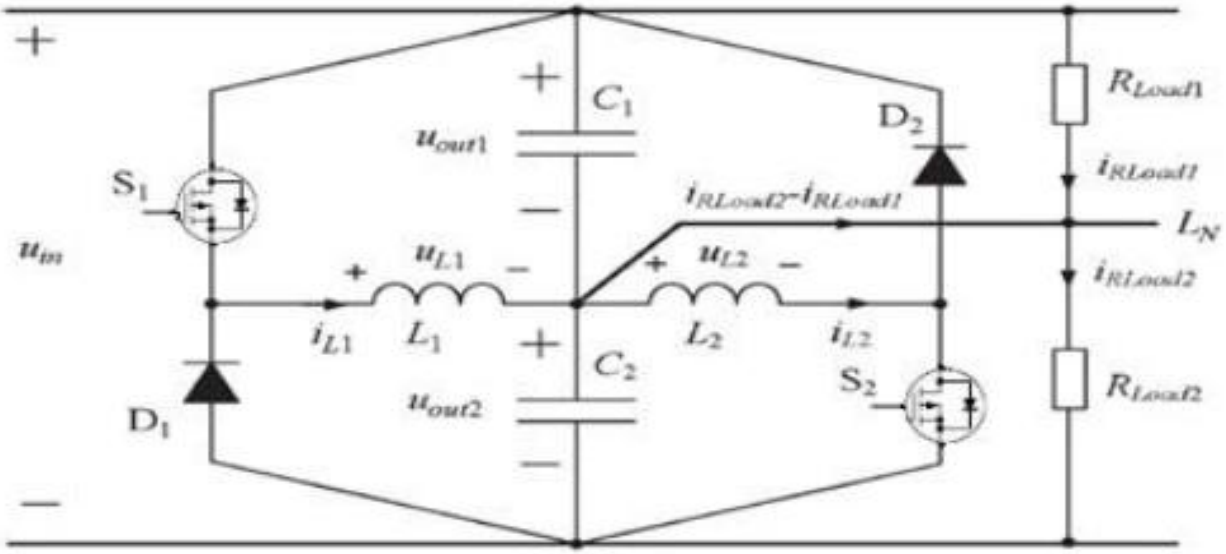

Fig.6. Proposed dual buck half bridge voltage balancer

Thus, the two inductor currents will cause additional power losses which leads to system inefficiency. It is very essential to have a control strategy that can drive the left bridge leg and the right bridge leg, respectively, based on the different power quantity of the balanced and unbalanced loads. Hence voltage balancer is placed near a converter to balance positive and negative voltages. It is also possible to place it near load side.

B. *Neutral point clamped (NPC) inverter*

The neutral point converter is proposed in fig. 7 was essentially a three-level diode-clamped inverter. Several researchers have reported that NPC inverter is very efficient when compared with the traditional inverters. These inverter

will be used in static var compensation, variable speed motor drives, and high-voltage system interconnections. A three-phase six-level diode-clamped inverter is shown in Figure 7. Each of the three phases of the inverter shares a common dc bus, which has been subdivided by five capacitors into six levels. The voltage across each capacitor is Vdc, and the voltage stress across each switching device is limited to Vdc through the clamping diodes.

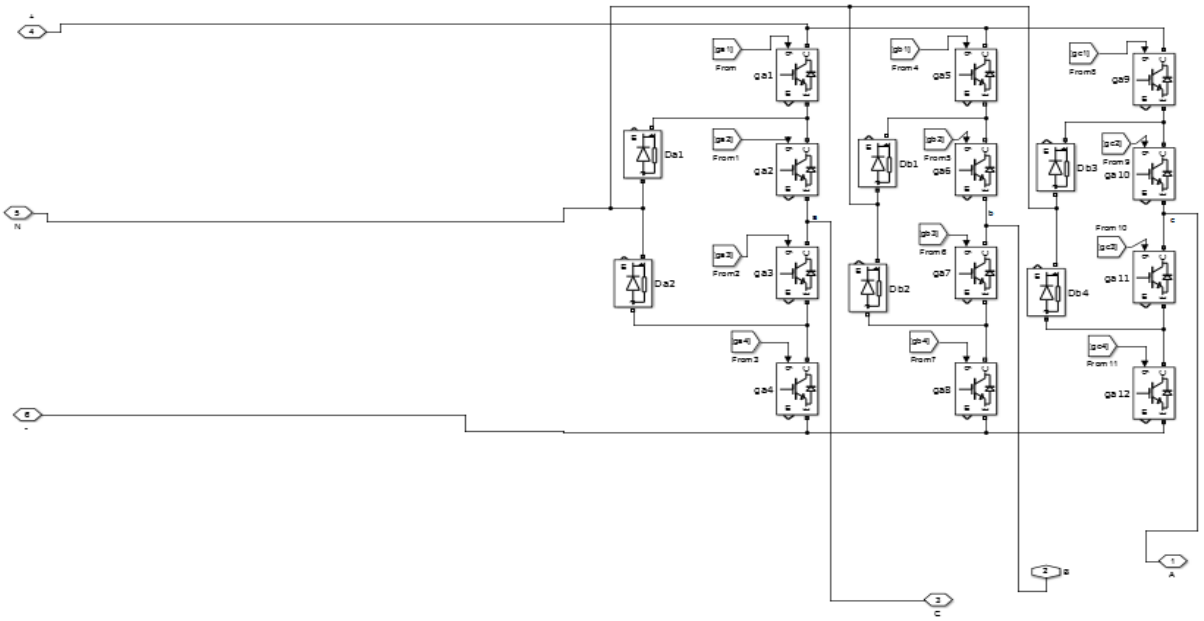

Fig.7 Simulation diagram of neutral point clamped inverter

C. Advantages of NPC:

i. All of the phases share a common dc bus, which minimizes the capacitance requirements of the converter. For this reason, a back-to-back topology is not only possible but also practical for uses such as a high-voltage back-to-back inter-connection or an adjustable speed drive.

ii. The capacitors can be pre-charged as a group.

iii. Efficiency is high for fundamental frequency switching.

iv. Reduced switching losses.

IV. SIMULATION RESULTS

To analyze the propose d control strategy, the simulation has been done in PSIM. The power rating of a Neutral clamped inverter is 3 kW in the simulation. The parameters in the simulation are shown in Table II. The RMS of the rated phase voltage is 115 V, and the voltage reference Vmax as 10% higher than the rated value. The rated utility frequency is 50 Hz, and the upper and the lower values of the limiter in the PLL are given as 0.2 Hz higher and lower than the rated frequency, respectively.

Table 1

Parameters in the power stage

Parameters	Values
DC voltage V_{dc}	400V
Filter inductor L_f	3.5mH
Filter capacitor C_f	15 F
Switching frequency f_s	10kHz
Sampling frequency f_{smp}	20kHz
Rated power of DG P_{DG}	3000W
Rated RMS phase voltage V_n	115V
Rated utility angle frequency $_o$	50
Rated linear local load $R_{load\ ac}$	60
Rated nonlinear local load $R_{load\ dc}$	120

Table 2

Parameters in the control system

Parameters	Values
Voltage reference V_{max}	179V
Rated current reference I_{grefd}	9A
Rated current reference I_{grefq}	0A
Upper value of the limiter $_{max}$	50.2
Lower value of the limiter $_{min}$	49.8

In the grid-tied mode, the dynamic performance of the conventional voltage mode control and the proposed unified control strategy is compared by stepping down the grid current reference from 9 A to 5 A. Here the simulation result of the proposed control strategy is represented in Fig. 8(a) dynamic process is very less than the previous one. By observing the simulation results it can be seen that the dynamic performance of the proposed control strategy is better than the conventional voltage mode control.

During the transition from the grid-tied mode to the islanded mode, the proposed unified control strategy is compared with the hybrid voltage and current mode control, and the simulation scenario is shown as follows: 1) Initially, the utility is normal, and the DG is connected with the utility; 2) at 0.5 s, islanding happens; and 3) at 0.52 s, the islanding is confirmed.

Simulate results with the hybrid voltage and current mode control.It can be seen that the grid current drop to zero at 0.5 s, and that the load voltage is distorted from 0.5 to 0.52 s. Then, the load voltage is recovered to the normal value after 0.52 s. Here Fig. 8(b) presents the simulation results with the proposed control strategy with neutral point clamped (NPC) inverter. Initially, the magnitude of grid current is 9 A and follows the current reference Igref dq . The magnitude and frequency of the load voltage are held by the utility. After the islanding happens, the amplitude of the load voltage increases a little to follow the voltage reference Vmax, and the output current of DG decreases autonomously to match the load power demand with a smooth inductor current.

Comparing the simulation results above, it can be found that the voltage quality is improved deeply by the proposed control strategy in the transition from the grid-tied mode to the islanded mode, and the speed of the islanding detection is no more critical.

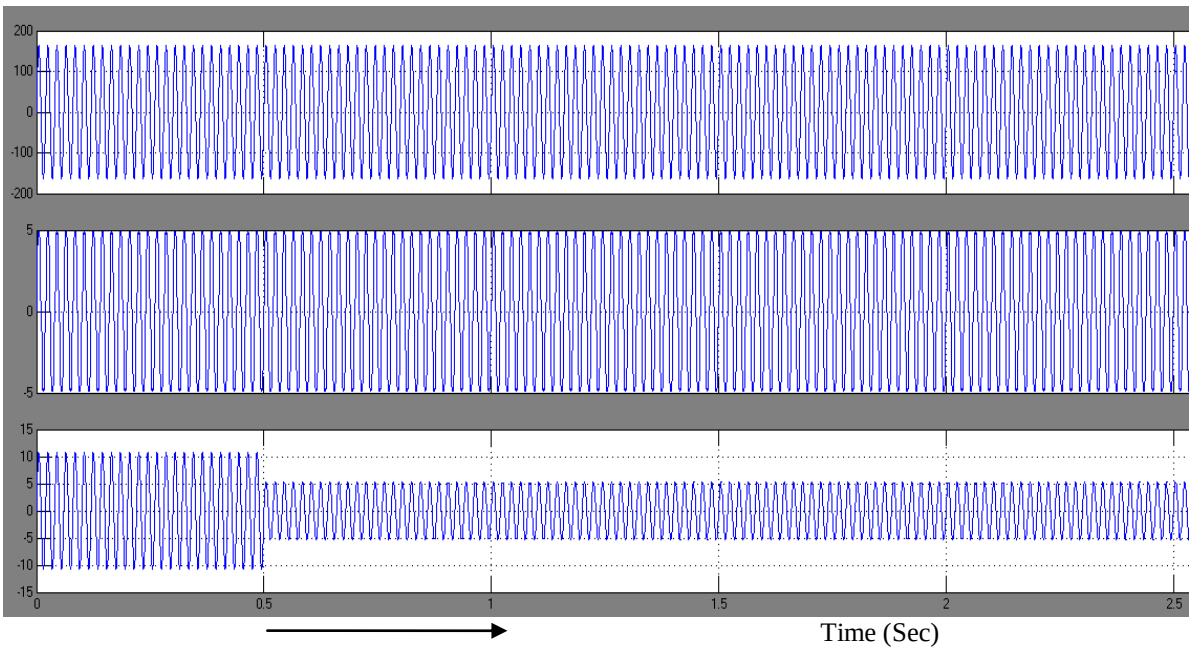

Fig.8.(a) Simulation waveforms of load voltage v_{ca}, grid current i_{ga}, and inductor current i_{la} when DG is in the grid-tied mode with proposed control strategy.

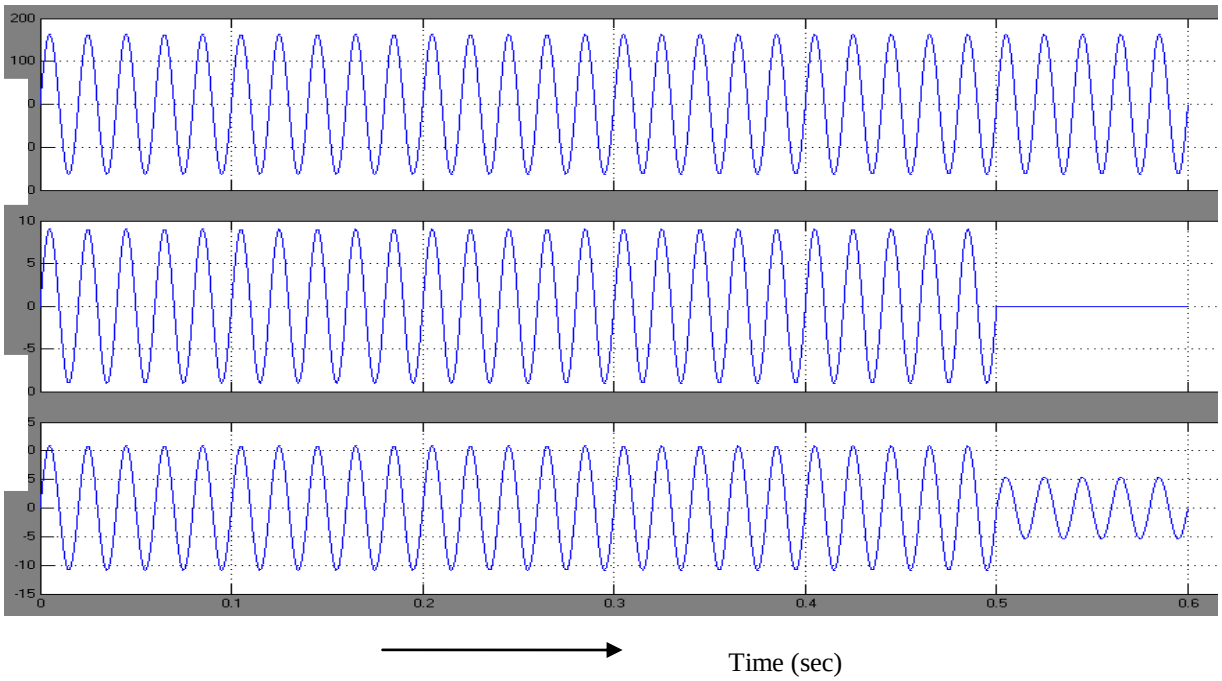

Fig.8.(b) Simulation waveforms of load voltage v_{ca}, grid current i_{ga}, and inductor current i_{la} when DG is transferred from the grid-tied mode to the islanded mode with proposed control strategy.

V. CONCLUSION

A new control approach was proposed for three-phase neutral point clamped (NPC) inverter in DG to operate in both islanded and grid-tied modes, with no need for switching between two different control architectures or critical islanding detection. A novel voltage controller was presented. It is inactivated in the grid-tied mode, and the DG operates as a current source with fast dynamic performance. Upon the utility outage, the voltage controller can automatically be activated to regulate the load voltage. Moreover, a novel load current feed-forward was proposed, and it improves the waveform quality of both the grid current in the grid-tied mode and the load voltage in the islanded mode. The quality of waveform, fast dynamic performance of DG and the advantages of the proposed control topology are verified by the simulation results.

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