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Design of Low Power Phase Locked Loop using Current Starved Voltage Controlled Oscillator

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Abstract — *This work is based on design of low power PLL with the help of CSVCO. The conventional voltage control oscillator will take more power as compare to CSVCO. VCO is the major part of PLL circuit and it affects the system performance in terms of power consumption and noise performance. In modern VCO design power consumption and high output frequency range have become important performance metrics .To design PLL proposed circuit will replace PLL with CSVCO .Because the VDD varies ±10% of 1.8V i.e from 1.62V to 1.98V.For this voltage variation the ring architecture produces an output frequency from 4.175GHz to 5.077GHz with the difference of 992 MHz, which is large variation. The output frequency is not stable when it is dependent on VDD. In most of the application PLL are used for clock and data recovery purpose to achieve this the CSVCO will use. This CSVCO is applicable for PLL application such as clock generation and recovery, frequency synthesizer, fast locking in digital circuit etc. The proposed circuit area and power consumption are very less and compatible for PLL application. The circuit analysis is performed and respective wave form are generated at 1MHz and power gain estimation at1GHz is 33.22E-6 is obtained with supply voltage of 1V. All the generated wave form are analyzed by using Cadence Virtuoso Gpdk045nm CMOS technology.*

Keywords- *Phase Locked Loop, Current Starved Voltage Control Oscillator, and Voltage Control Oscillator.*

I. INTRODUCTION

PLL stands for Phase Locked Loop and is basically a closed loop feedback control system that compares the output frequency/phase with the input frequency/phase. The Phase Locked Loop was first discussed in literature as far back as 1919 by Vincent [1] and Appleton [2], who experimented with the synchronization of oscillator. It wasn't until 1932 that it become a main stream electronic device when it was used as part of a simpler alternative to the popular, but somewhat complicated superheterodyne receiver. The alternative device become known as the homodyne or synchronous receiver. However at the time that this simple alternative was conceived (1932) the cost of including a PLL in every receiver was significant and so the superheterodyne receiver continued to be used commercially until the PLL becomes available as a cheaper integrated circuit in late 1960's . In the 1960's interest and publications in PLLs increased dramatically and culminated in the development of the PLL Integrated Circuit, which facilitated the rapid introduction of PLLs into consumer electronic devices [3]. Today, PLLs play an important role in model in communication devices. They are considered to be the most robust means of generating a low noise reference signal and the best means of determining the clock signal from o noisy source. The ubiquitousness of the PLL is due to its wide range of application including frequency synthesis, phase modulation, clock data recovery, disk drive electronics, AM and FM demodulation, motor speed control, and FSK decoders [4]. A VCO is a main building block of the PLL circuit. A PLL can be designed with the help of RC or LC circuit. A LC VCOs have better noise performance compared to ring oscillator but it has a small tuning range, large layout area and possibly higher power [5] .The ring oscillator has not required on-chip inductors. Thus the chip area is reduced and it has wide tuning range. Basically PLL has two type namely source coupled VCO and current starved VCO. Current Starved VCO provide some advantage as compare to source coupled VCOs. CSVCO has good phase noise, consuming less power and has improved tuning range [6]. That's why in proposed circuit VCO has replaced by CSVCO. This paper mainly focus on design of low power PLL circuit and the remaining part of the paper is ordered as follows. Section II describes the design parameter for CSVCO and section III describe the methodology of the proposed circuit. Section IV describe simulation results and discussion and finally section V includes the conclusion.

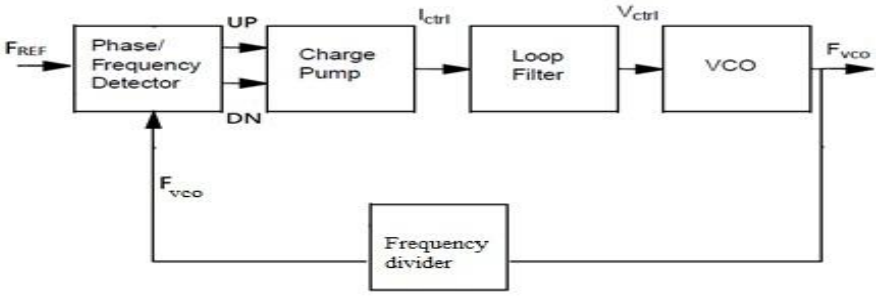

Figure 1: Basic block diagram of PLL

II. DESIGN PARAMETER FOR CSVCO

The CSVCO circuit is main part of the proposed PLL circuit. So before design the CSVCO circuit we need some design parameter which is very important for the design procedure .Basically CSVCO has two major parts, the inverter stage and current starving circuitry. The design objective of the proposed circuit is to minimize phase noise and power of the CSVCO with desired frequency oscillation .An N-stage current starved VCO has an oscillation frequency which is given by [7]-[8] .

$$f_{osc} = \frac{I_D}{NV_{dd}\left(C_{in}+C_{g_{dp}}+C_{gdov_p}+C_{db_p}+C_{gdov_n}+C_{db_n}+C_{gsov_n}+C_{gbov_n}\right)}$$

Where,

$$C_{in} = \frac{2}{3}C_{ox}W_nL_n$$

$$C_{gd_p} = \frac{1}{2}C_{ox}W_pL_p$$

$$C_{db_n} = \frac{C_{jn}A_{d_n}}{\left(1+\frac{V_{dd}}{pb_n}\right)^{mj_n}} + \frac{C_{js}W_n pd_n}{\left(1+\frac{V_{dd}}{pbs\,w_n}\right)^{mjsw_n}}$$

$$C_{gdov_n} = \left(1+\cos\frac{\pi}{N}\right)W_nC_{gdo_n}$$

$$C_{db_p} = 2Cj_pAd_p + 2Cjsw_pPd_p$$

$$C_{gdov_p} = W_pC_{gdo_p}$$

$$C_{gsov_n} = W_nC_{gso}$$

$$C_{gbov_n} = 2L_nC_{gbo}$$

Where,

C_{ox} = Oxide capacitance pr unit area
w_n = Channel width of nMOS
w_p = Channel with of pMOS
L_n = Channel length of nMOS
L_p = Channel length of pMOS

To determine the total capacitance equation of CSVCO is given as

$$C_{tot} = C_{out} + C_{in}$$

$$C_{tot} = C_{ox}\left(W_pL_p+W_nL_n\right)+\frac{3}{2}C_{ox}\left(W_pL_p+W_nL_n\right)$$

$$C_{total} = \frac{5.C_{ox}\left(W_pL_p+W_nL_n\right)}{2}$$

Where,

C_{ox} = Oxide capacitance
w_n = Width of nMOS
w_p = Width of pMOS
L_p = Length of pMOS
L_n = Length of nMOS

Power Consumption: The total power dissipated by N-stage CSVCO circuit is given by [9]

$$P = P_{avg} + P_{SC}$$

Where, P_{avg}= Average power dissipated by the CSVCO
P_{sc}= Short circuit power dissipation

Phase Noise: The phase noise of the CSVCO circuit is given by [10]

$$\mathcal{L}\{\Delta f\} = \frac{8}{3\eta}\frac{kT}{P}\frac{Vdd}{Vchar}\frac{f_{osc}^2}{\Delta f^2}$$

Where, $V_{char} = \frac{\Delta V}{\gamma}$

P = Total power dissipated by the CSVCO, Δv is the gate over drive voltage, k is Boltzmann Constant is absolute temperature and γ is a coefficient which is 2/3 for long channel devices in saturation and twice or thrice of this for short channel devices and η is a characteristic constant which is taken here as 1. Δf is the offset frequency from the carrier at which the phase noise is measured .

III. METHODOLOGY

3.1. Phase Frequency Detector

Phase frequency detector is one of the important parts in PLL circuits. PFD is a circuit that measures the phase and frequency difference between two signals. PFD has two outputs UP and DOWN which are signaled according to the phase and frequency difference of the input signals. The output signals of the PFD are fed to the charge pump. The output voltage of the charge pump controls the output frequency of the VCO. So with a change happens at the input of the charge pump the output voltage will change which will change the output frequency of the VCO. In this case the sensitivity of the phase and frequency difference detection of the PFD is very crucial. Sensitivity of the phase frequency detector means the smallest difference the PFD can detect and produce UP or DOWN signals that will affect the charge pump [11]. This lead to the conclusion that the higher sensitivity is better for Phase Frequency Detector.

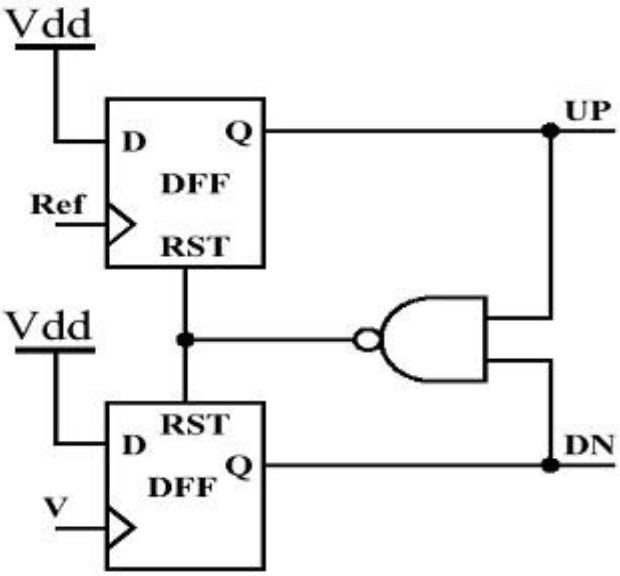

Figure 2: Phase Frequency Detector

3.2. Charge Pump

The Charge pump PLL is an extension of the basic phase locked loop which requires the addition of a charge pump between the phase detector and loop filter. The charge pump converts the voltage fluctuation in the phase detector to corresponding current signal thereby reduces the static error. The charge pump of PLL is considered to be ideal when it reduce equal output current from both the UP and DOWN network. Eventually signal output current is pumped out from this circuit by taking two input voltages UP and DOWN. The charge pump consists of a set of current sources with magnitudes of I_{p1} and I_{p2} amps respectively. In most cases the current sources are symmetrical. Thus I_{p1}= I_{p2}= Ip. In the circuit one source (Ip) is connected to the positive supply rail while the other (-Ip) is connected to the negative supply rail. The source are separated by two switches S1 and S2. The output of the phase detector provides the gating signals UP and DOWN which tur n on S1 and S2 respectively. The phase detector is designed such that the switches are never ON simultaneously. When UP is high and DOWN is low then S1 is ON and S2is OFF. This causes current to flow out of the pump and into the loop filter. The three control state for charge pump is shown in table 1.

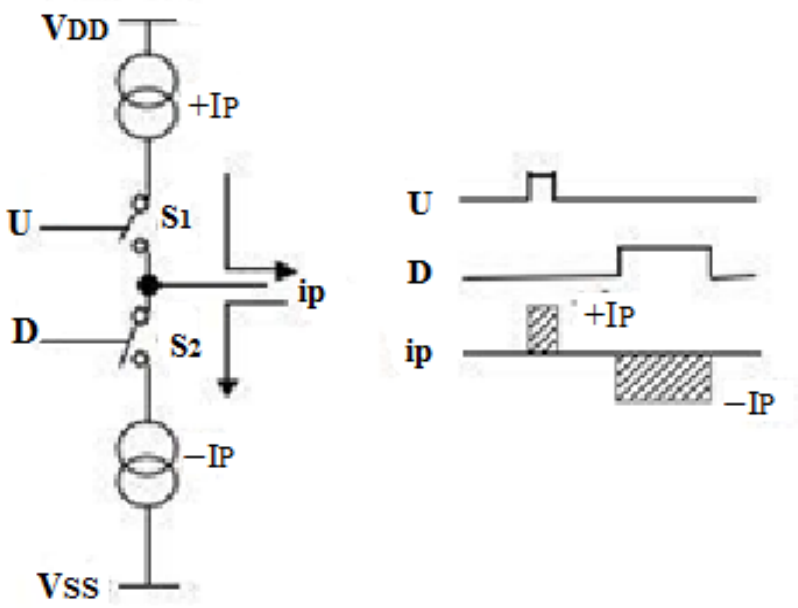

Figure 3: Charge Pump

Table 1: Three state of Charge Pump

Up	Down	Description
1	0	Raising up signal
0	1	Raising down signal
0	0	No change in UP/DOWN

3.3 Loop Filter

The function of the loop filter is to convert the output signal of phase frequency detector to control voltage and also to filter out any high frequency noise introduced by phase frequency detector. The loop filter shown in figure is a simple combination of RC circuit component. Since the output of the phase frequency detector is oscillating the output of the loop filter will show a ripple as well even when the loop is locked.

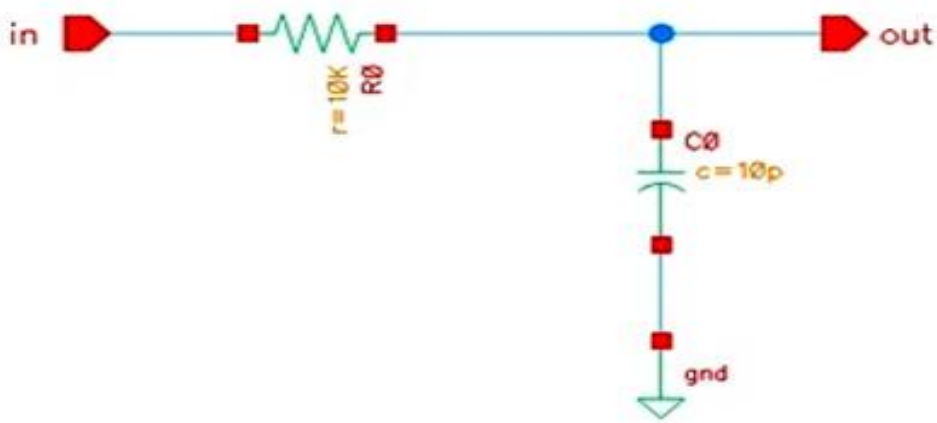

Figure 4: Low pass filter

3.4 Current Starved Voltage Controlled Oscillator

The current starved VCO is a heart of phase locked circuit. In proposed PLL design the CSVCO circuit is used. The working of the CSVCO is similar to the ring oscillator. In the designed CSVCO an inverter stage is fixed with 5. To better understanding of the CSVCO working an on stage CSVCO is shown in figure 5.

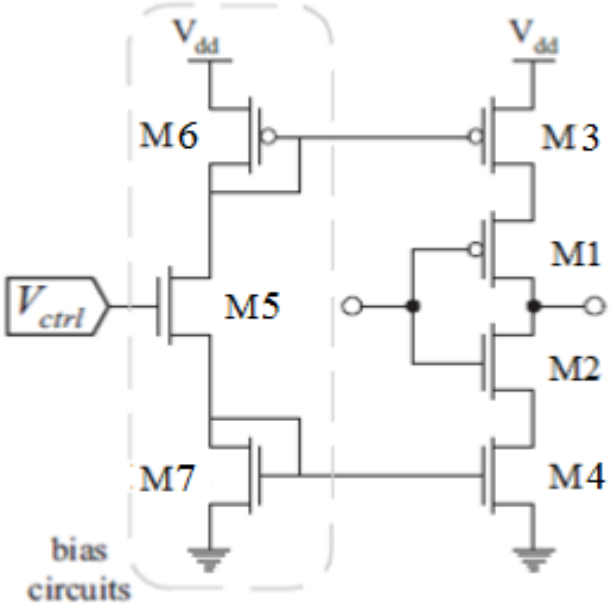

Figure 5: Simplified view of CSVCO

In the above circuit transistor M1 and M2 operate as an inverter while transistor M3 and M4 operate as current sources. The current sources M3 and M4 are limit the current available to the inverter stage. In other words the inverter is starved for current. The transistor M6 and M7 have a drain current are same and it is set by the input control voltage. The current provided to M6 and M7 are mirrored in each current and inverter stage [12].

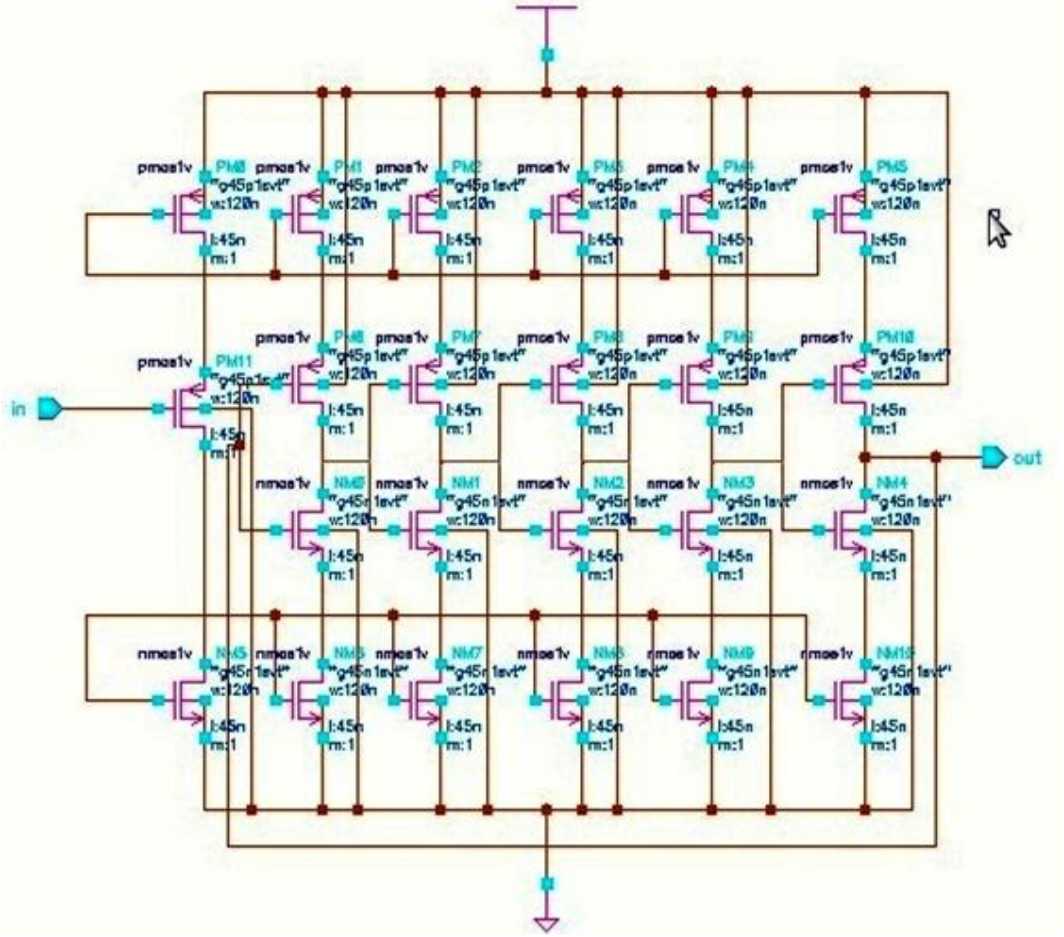

Figure 6: Schematic circuit of Current Starved VCO

The above schematic circuit of CSVCO is used in proposed Phase locked loop circuit. In this circuit a 5 stage inverter is proposed. The working of each stage can easily understand by the principal of single stage CSVCO. In the proposed circuit five stage ring oscillator is used and a 1V of input voltage is provide to each stage.

3.5 Frequency Divider

Frequency divider divides the VCO frequency to generate a frequency which is comparable with reference frequency. The frequency divider which connects to the feedback loop of the PLL multiplies the incoming external clock. In the PLL closed loop the effect of the frequency divider is to multiply the PLL input frequency by its division factor.

IV. SIMULATION RESULTS

The main objective of the design was low power phase locked loop using current starved voltage controlled oscillator. And it is achieved in proposed design. The designed objective is shown in figure 7. And the output of the phase locked loop is shown in figure 8.The overall power calculation has done for PLL circuit and it is observed to be 33.22µw. And during the overall performance of the circuit supply voltage was 1V and frequency was 1GHz.

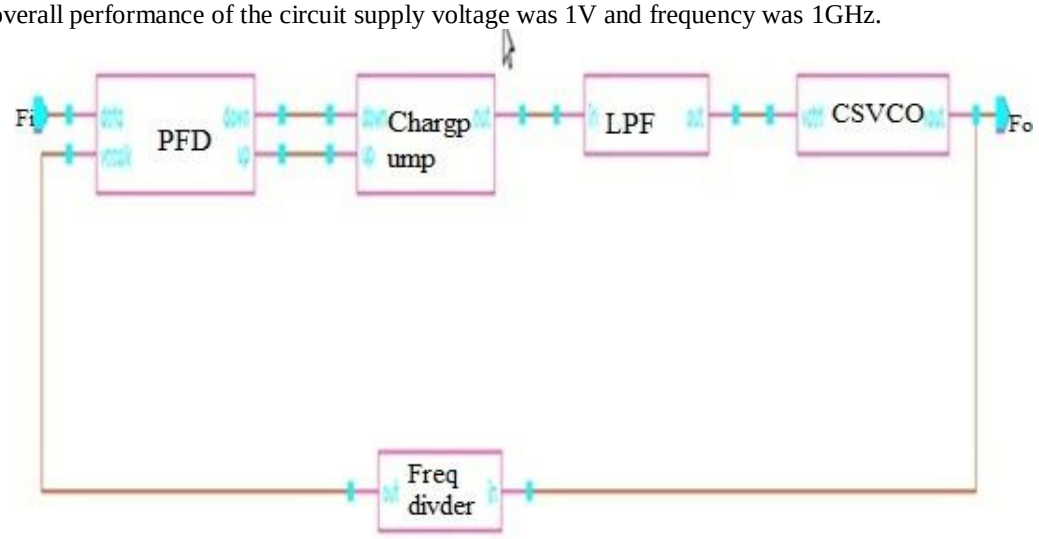

Figure 7: proposed design of Phase locked loop

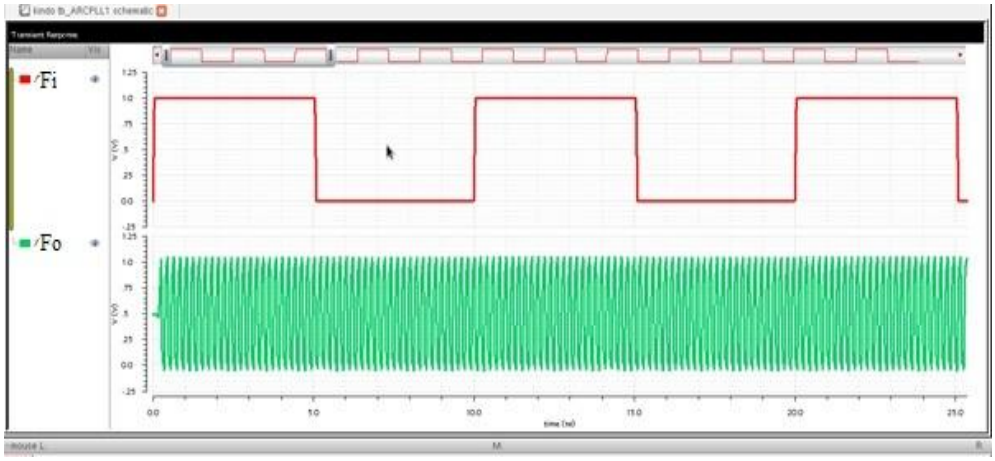

Figure 8: Designed simulation result of Phase locked loop

Table 2: Performance comparison of present work with earlier work

Parameters	Reported in[9]	Reported in[6]	Proposed work
Technology	45nm	90nm	45nm
Centre Frequency	1GHz	2GHz	1GHz
Power	55. 257µw	765. 641µw	33. 22µw
Supply Voltage	1V	1.2V	1V

The performance of the Phase locked loop is being compared with the other work and found that this work is better than other works. Table 2 shows the comparison on the basis of various parameters. The proposed phase locked loop has been designed and simulated in Cadence virtuoso gpdk045nm technology.

IV. CONCLUSION

This paper presents a design of low power phase locked loop using current starved voltage controlled oscillator. The design of PLL is then compared with previous works and improvements are observed. The PLL circuit is used in synchronizing the clock, skew and jitter reduction as well as wireless application etc. All the design of the PLL circuit has done in 45nm technology using Cadence virtuoso tool with supply voltage of 1V. With the simulation result it can be concluded that the proposed CSVCO which used in design of PLL could achieve high frequency of oscillation having low power and less delay.

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