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COMPARATIVE PERFORMANCE ANALYSIS OF OPTIMIZED POWER AND AREA FOR FULL ADDER USING GDI CELL

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Abstract— *This paper presents a high drivability of full adder with less area and power consumption. This GDI based full adder is implemented by using both gate diffusion input (GDI) technique and pass transistor logic that leads to be a reduced area and power.. The comparison has been done between existing systems like CMOS, CPL, 14T full adder and proposed full adder. All full adders are designed with 0.18um in tanner schematic and simulations are done in T-Spice. Tool .By Using this full adder we have designed the ripple carry adder and carry skip adder which is compared with all existing systems and finally concluded that our proposed method is showing better results in terms of area and power hence we can say our method is efficient in area and power consumption.*

Keywords— *GDI technique, Ripple carry adder, CMOS and CPL.*

I. INTRODUCTION

The adder is a basic building block to many digital circuits like a digital signal processor (DSP), microprocessor, and also it plays the major role in array multiplier to add partial products. In arithmetic unit binary addition plays the major role because every arithmetic operation are performed by using an addition operation. So building low power and high performance adders would affect the system performance and also reduce the whole power consumption. That's why to achieving its performance is crucial to improving the whole circuit performance. The proposed full adder is designed with a minimum number of transistors it causes the low power consumption and also less Area. Adders are extensively used circuit elements in Very Large Scale Integration (VLSI) systems such as Digital Signal Processing (DSP)processors, microprocessors etc. It is the nucleus of many other operations like subtraction, multiplication, division and address calculation. In most of the digital systems, adders lie in a critical path which influences the overall system performance

II. LITERATURE SURVEY

K. Navi, M.H. Moaiyeri [1] designed Two new low-power full adders based on majority-not gates power consumption, a high degree of regularity, and simplicity. Low power consumption is targeted in implementation of our designs. Eight state-of the-art 1-bit Full Adders and two proposed Full Adders are simulated using 0.18 mm CMOS technology at many supply voltages. Simulation results demonstrate improvement in terms of power consumption.

M.H. Moaiyeri [2], D. Radhakrishna,,R. Faghih Mirzaee [3] and M. Alioto, G. Palumbo [38] Low average power consumption. Some effective approaches are presented for improving the performance, voltage levels, and the driving capability and lowering the number of transistors of the basic structure of the designs. All of the proposed designs and several classical and state-of-the-art 3-input XOR circuits are simulated Low power design has become one of the primary focuses in digital VLSI circuits, especially in clocked devices like microprocessor and portable devices. Optimization of several devices for speed and power is a significant issue in low-voltage and low-power applications. These issues can be overcome by incorporating Gated Diffusion Input (GDI) technique.

C.N.Nagendra M.J. Irwin[3],G. Maki and Arkadiy Morgenshtein,[18] The results differ from those previously published both for the more realistic simulations carried out and the more appropriate figure of merit used. They show that, except for short chains of blocks or for cases where minimum power consumption is desired, topologies with only pass transistors or transmission gates are not attractive. It provides high speed digital component as well as a full voltage swing circuit. Many of the previously reported adders in literature suffered from the problems of low-swing and high noise when operated at low supply voltages. These two new designs successfully operate at low voltages with tremendous signal integrity and driving capability. The group generate and group propagate functions used in Ripple Carry Adder logic are used to speed up multiple stages of carry Skip adders. The optimum sizes for the skip blocks are decided by considering the critical path into accountt

III. DIFFERENT FULL ADDER TOPOLOGIES

The full adders are mainly classified into two types one is static and another one is dynamic full adders. Static full adders consume less power than the dynamic full adders because dynamic logic is a clocked logic. For N-input module, static

requires 2N transistors and dynamic requires N+2 transistors. The advantage of using dynamic logic is faster switching speed and less static power dissipation. By combining both logic styles. We can achieve low area and power by combining two or more logic styles in a single circuit

3.1 CMOS full adder

The static CMOS full adder follows the regular CMOS structure it usually contains one PMOS pull-up network and one NMOS pull-down network. as shown in Figure 1.

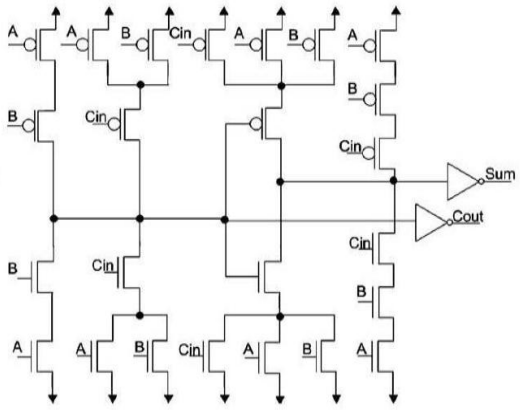
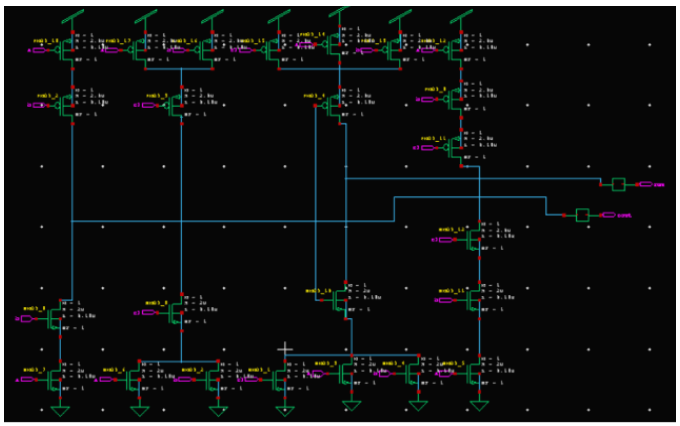


Fig.1 C-CMOS Full adder

Schematic diagram of C-CMOS full adder using Tanner



In complementary CMOS logic the same function is performing two times, it may cause increasing of area and power.The advantage of complementary CMOS style is its robustness against voltage scaling and transistor sizing, which are essential to provide reliable operation at low voltage with arbitrary transistor size.

It is used in integrated circuit, microprocessors, microcontrollers and other digital logic circuits for to reduce power consumption and being more immune towards noise occurring conditions. In the CMOS there are complementary and Symmetrical pairs which are of P-type (PMOS) and N Type (NMOS) which are used for implementation of logic functions. In a PMOS transistor we can have input from voltage source or from other PMOS transistor

3.2 CPL Full adder

CPL full adder provides high-speed, full-swing operation and good driving capabilities due to the output static inverters and fast differential stage of cross coupled PMOS transistors. It is connected to any one input. The block diagram of a full adder using CPL as shown in Figure-2 The disadvantage, of pass transistor logic is that threshold voltage drops through the NMOS transistors makes it necessary to maintain output voltage level, hence inverter is used at output which increases the number of transistors .Due to the presence of lot of internal nodes and static inverters, there is large power dissipation.

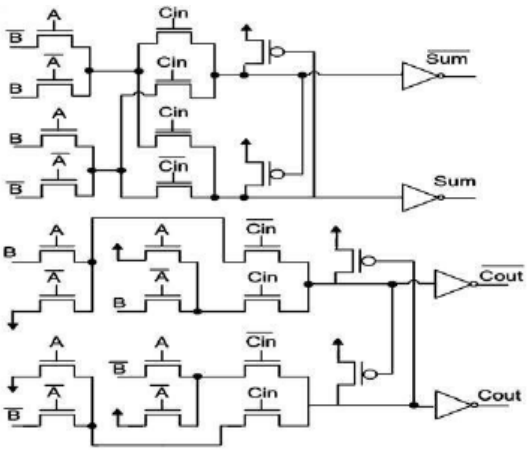
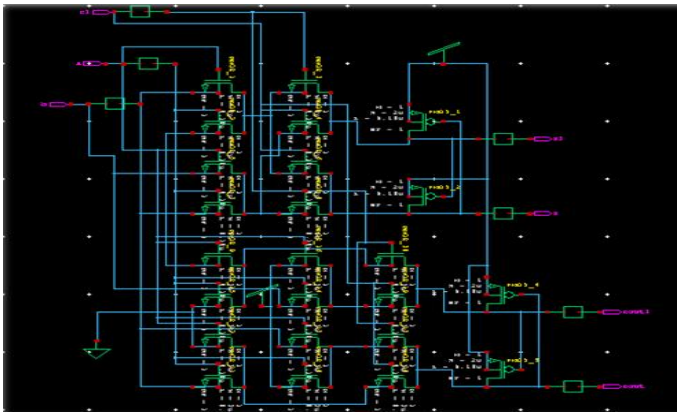


Fig.2 CPL Full adder

The differential stage, on the other hand, leads to considerably larger short- circuit currents. Because the high voltage level of the pass-transistor outputs is lower than the supply voltage level by the threshold voltage of the pass transistors, the signals have to be amplified by using CMOS inverters at the outputs. The advantages of pass logic transistors include smaller number of transistors and smaller input loads, along with MUX and especially XOR circuits being implemented efficiently.

Schematic diagram of CPL Full adder Using Tanner



4. Proposed Full adder

The new approach to GDI-MUX and pass transistor. Using GDI-MUX technique AND, OR and multiplexer eliminating the use of XOR and XNOR gates in full adder design is full adder using are implemented, by using this gates and pass transistor logic a new full adder is implemented

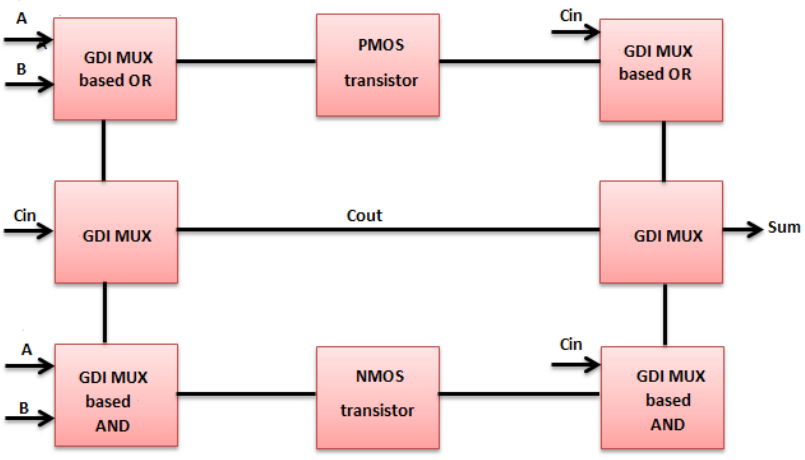


Fig.3 logical structure for designing full adder

GDI (Gate Diffusion Input) cell consists of one PMOS and NMOS transistor. Its look like a static CMOS inverter but it differs because the GDI cell has two extra inputs. The GDI method is based on the use of a simple cell. One may be reminded of the standard CMOS inverter at the first glance of this circuit, but there are some important differences: The GDI cell contains three input G (common gate input of NMOS and PMOS), P (input to the source/drain of PMOS), and N (input to the source/drain of NMOS).Bulks of both NMOS and PMOS are connected to N or P (respectively), so it can be arbitrarily biased in contrast to CMOS inverter The GDI cell with four ports can be recognized as a newly multifunctional device, which can achieve six functions with different combinations of inputs G, P and N.

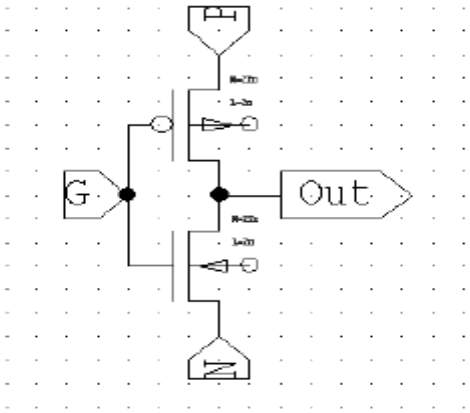


Fig.4 Basic GDI Cell.

PMOS and NMOS are connected to Vdd and ground. The GDIMUX based OR gate is modeled by connecting source/drain of NMOS (N input) to Vdd, common gate (G input) to A and P input to B. Similarly AND gate is designed by connecting N input to B, G to A and P input to GND The requires only four transistors. Obviously, the proposed GDI XOR and XNOR gates use less transistors compared with the conventional CMOS counterparts.

From truth table of a full adder, we can consider that when Cin = 0, the full adder Cout is equal to A AND B otherwise it is equal to A OR B. By using multiplexer Cout is selected. As shown in table 1 and 2 The analysis has been performed on various process and circuits techniques, the analysis with minimum transistor size to minimize leakage power, the latter with simulate transistor dimension to minimize leakage current. The simulation has been carried out on a Tanner voltage values. Thus design guide-lines have been consequent to select the most suitable topology for the design features required. This paper also proposes a novel figure of merit to realistically environment virtuoso tool using a 180nm technology. Simulations have been also compared for different supply compare n-bit adders implemented as a chain of one-bit full adders

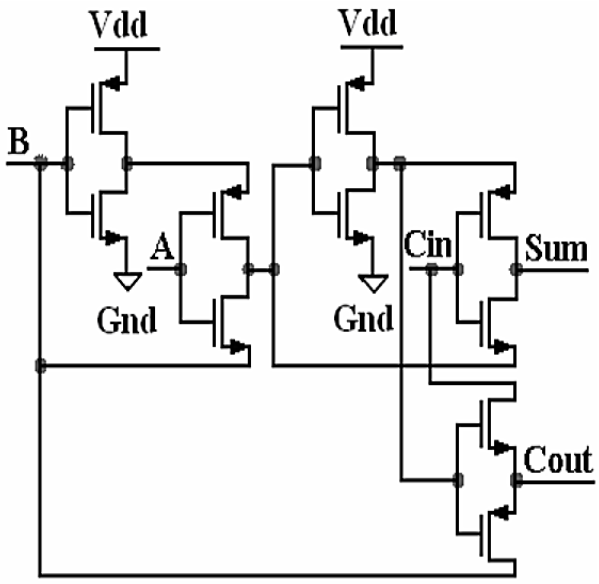


Fig.5 Proposed Full Adder using GDI Based 10t Transistor.

The source terminals of PMOS and NMOS are connected to Vdd and groundThe schematic of the proposed 10T CMOS full adder Proposed 10T CMOS full adder circuit design is optimized to consume less power and less fabrication area

Table 1

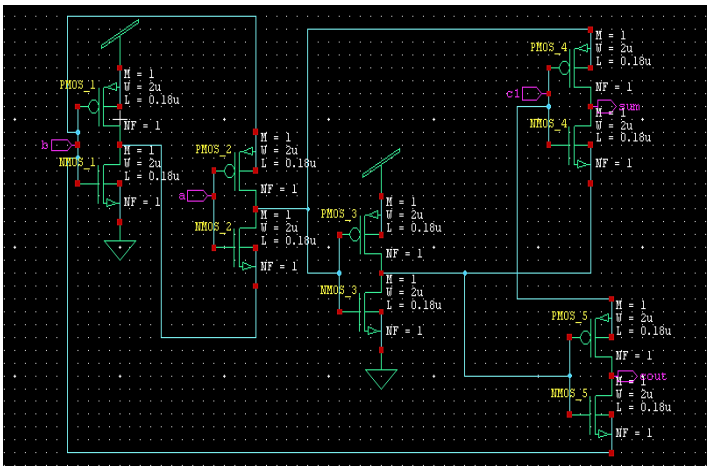
Cin	A	B	Cout=A AND B
0	0	0	0
0	0	1	0
0	1	0	0
0	1	1	1

Table 2

Cin	A	B	Cout=A OR B
1	0	0	0
1	0	1	1
1	1	0	1
1	1	1	1

When Cout = 0, the sum is equal A OR B OR Cin otherwise sum is equal to A AND B AND Cin. The width and length ratio of PMOS and NMOS transistor in first GDI-MUX and second GDI-MUX based AND gate is 400n:180n. To achieving the full swing the width and length ratio is changed. And also the PMOS and NMOS pass transistors are added

Schematic diagram of proposed Full adder using Tanner



5. ADDER ARCHITECTURE OVERVIEW

A n-bit binary adder can be seen as the special arrangement of n full adder units that each take three one-bit inputs: A, B and Cin and which generate sum and Cout,. The characteristics of a few common adder architectures are summarized in the following subsections, which include: Ripple Carry Adder (RCA)

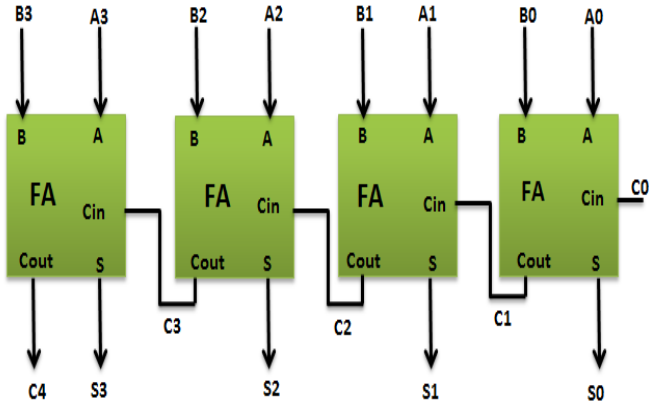


Fig.6 Ripple carry adder architecture

So to design a 4-bit adder circuit we start by designing the 1 –bit full adder then connecting the four 1-bit full adders to get the 4-bit adder as shown in the diagram above. For the 1-bit full adder, the design begins by drawing the Truth Table for the three inputs and the corresponding output Sum and Carry. The delay of ripple carry adder is linearly proportional to n, the number of bits, therefore the performance of the RCA is limited when n grows bigger. The advantages of the RCA are lower power consumption as well as a compact layout giving smaller chip area

Schematic diagram of Ripple carry adder

Using Tanner

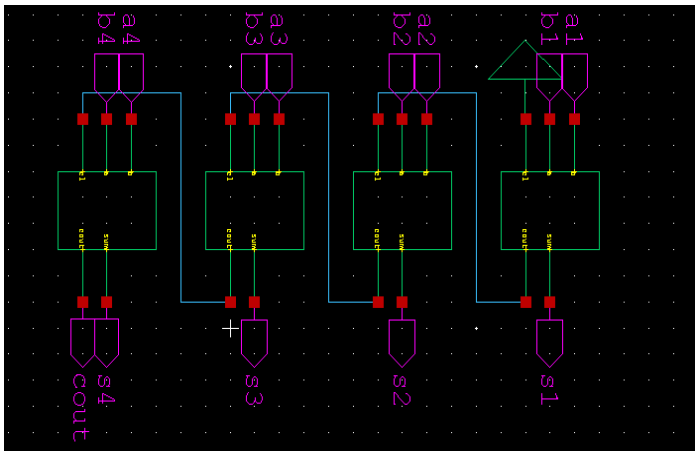


Table 3

Input Data A				Input Data B				Output				
A3	A2	A1	A0	B3	B2	B1	B0	Cout	S4	S3	S2	S1
0	0	0	0	0	0	0	0	0	0	0	0	0
0	1	0	0	0	1	0	0	0	1	0	0	0
1	0	0	0	1	0	0	0	1	0	0	0	0
1	0	1	0	1	0	1	0	1	0	1	0	0
1	1	0	0	1	1	0	0	1	1	0	0	0
1	1	1	0	1	1	1	0	1	1	1	0	0
1	1	1	1	1	1	1	1	1	1	1	1	0

6. Simulation and Results

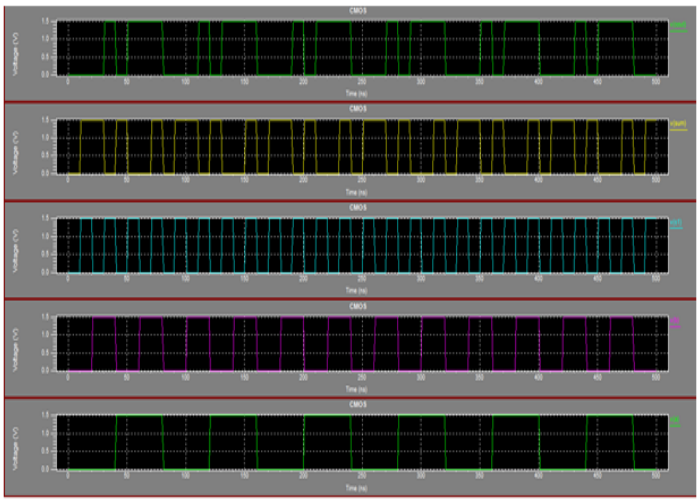


Fig.7 Output Waveform for CMOS

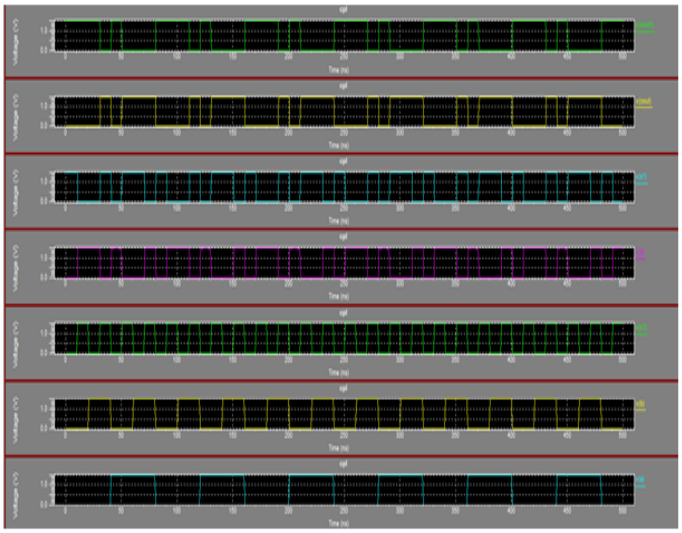


Fig.8 Output Waveform for CPL

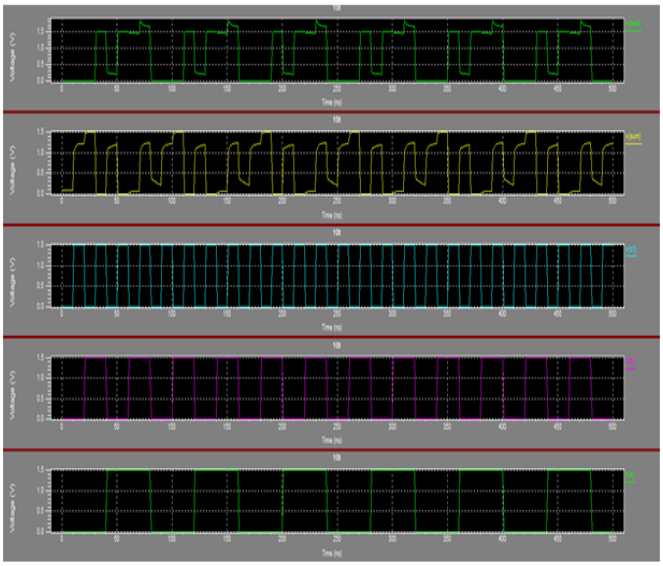


Fig.9 Output Waveform for GDI based 10t Transistor

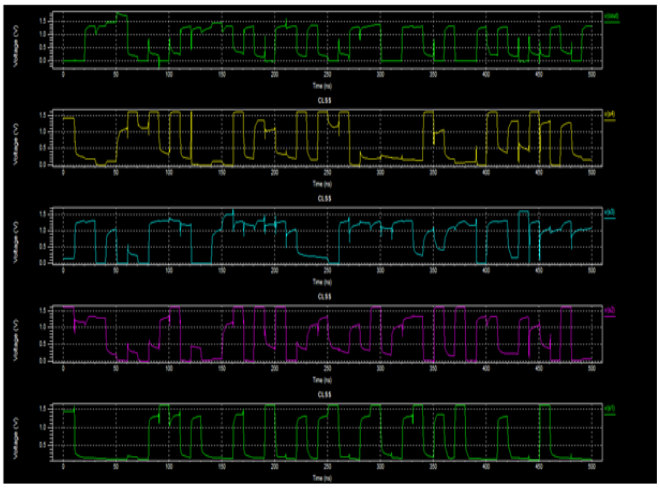


Fig.10 Output Waveform for Ripple Carry Adder

7. Observations

Power dissipation is calculated by varying supply voltage from 1.5 to 1.8V as shown in table-4..

Table 4

Supply Voltage(V)	C-CMOS (mW)	CPL (mW)	Proposed Full Adder (mW)	Ripple Carry Adder (mW)
1.5V	16.8m	13.6m	8.67m	10.59m
1.6V	20.6m	17.8m	10.11m	12.75m
1.7V	24.3m	21.9m	10.33m	15.51m
1.8V	29.1m	28.5m	11.69m	19.58m

8. Conclusion

Various types of full adders are designed using different logic styles. These C-CMOS, CPL and hybrid full adders are compared with new proposed full adder. The proposed full adder consist of less number of transistors, because of less number of transistors results in less switching activity and area. Power consumption is increases with increasing supply voltage as shown in table 4 The topology offers a more reasonable trade-off between power and delay for high performance circuits. 10T uses one three-transistor XNOR and one three-transistor XOR circuit. This is the reason for less power consumption in 10T circuit. Output load is one of the important parameters that affects power and performance of the circuits. In the final analysis, 10T GDI based full adder for multiplier is the best circuit for arithmetic operation in terms of power consumption for all values of output loads. Hence this is verified in case of extension applications of ripple carry adder and carry skip adder.

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