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LOW POWER AND HIGH PERFORMANCE MSML DESIGN FOR CAM USE OF MODIFIED XNOR CELL

Vidhi Chaudhary [1], Sarman K. Hadia[2], Brijesh Shah[2], Rachna Jani[2]

[1]*M.Tech (E.V.D), Department of CSPIT, Charusat University, Changa, India.*
[2]*Associate Professor, Department of CSPIT, Charusat University, Changa, India.*

Abstract-- *MSML design has been shown with the help of modified XNOR cell. Mainly this is used for low power and high performance. To perform the searching operations conventional design use only single match-lines and Master-Slave match line use single MMLs and multiple SMLs. Lower Power and high performances when MML share charge with mismatch SML. In this paper the simulations are obtained using Tanner EDA V-13 tool with 90nm CMOS technology. Match-delay of implementation of CAM design compare to conventional design in different bit-size condition.*

Keywords- *Master-slave match line (MSML),Master-slave (MS), content- addressable memory (CAM), low power, match line (ML), match delay (MD), Master match-lines (MMLs), Slave match-lines (SMLs).*

I. INTRODUCTION

A CAM memory comparing input searching data over a storing data and return addressed of match-data. CAM capable to use different type of execution which need high search speed. And those executions involve parametric curve extraction, Hough transform, Huffman coding-decoding and image coding [4],[5],[6]. CAM is good options to implement larger bit operation due to fastest search capability. As different type of memory, CAM store data in storage unit, provide searching data, after performing searching operation and last if any data will be match to the output data. In larger bit and larger word size bit design at that time large number of transistors and wires are used on every search that require more power consumption of CAM is significant. Each search will be a larger numbers of ML switching so matching and searching lines are main power consumers in CAM memory.

Most of the research will be interested in the ML power reduction and match-delay by different types of methods, including the ML segmentations, pipeline searching-scheme [7], [8]. In selective pre-charged techniques partitioned comparator and memory array in two part[7],[3].When ML needed to be pre-charged at that time main part will be active and smallest part of every comparison evaluation-phase done first. ML breaks in different part, pipeline search scheme [3], [8]. Every part evaluation-phase is continues. All these methods will be minimize power in good condition, to solve this type of problem other method is implemented is charged-share ML minimize the worst case power-consumptions. In charged–share ML recycled and transferred single ML charged to other ML charged [9]. The full ML separated in four segment and selected pre-charge to minimize power-consumption, in segments ML architecture (SMA) [10].Segment is divided in charge-share and pre-charge type. Before ML evaluations pre-charge segment charge and charge-share segment not pre-charge but shared charge to charge segments for evaluations of ML.

Improving the power-efficiency of shadow ML design suggest by current-recycle technique. These technique voltage-detector charged ML to define matching and mis-matching [11]. In mis-matching condition word circuit recognize fastest deactivate charging-path, in this shadow ML voltage detect schemes [12]. Here not only because of fast lookup table but also for minimize power-consumption effect in word-circuit, so voltage detectors and comparators are introduced. Best compact between ML power-consumptions and match-delay for CAM have continuously challenge point between the researches. The main focused in this paper is minimizing power-consumptions and high performances. Also compare conventional design with MSML design. So in this MSML design using XOR cell due to slow charging sharing problem some match-delay issue will be there, to overcome this type of problem modified XNOR CAM cell design. In XNOR cell high performances, low power consumptions and area also minimize to reduced number of transistor.

II. CAM Cell Design

Figure 1 shows a XOR CAM cell which include two units, first will be storage unit which store data and second will be comparator unit which compare data. In storage unit normally implement as 6T-SRAM cell which use include two cross coupled inverter. To compare storing data with searching data at that time comparator unit uses pass transistor logic (PTL).

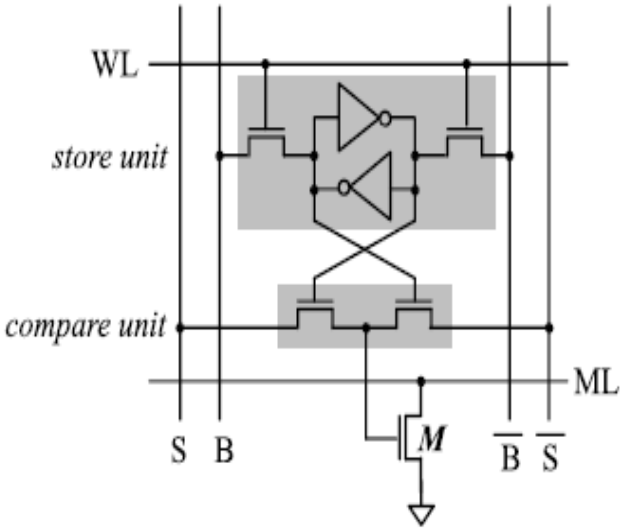

***Figure 1**: XOR CAM cell[1]*

According to different applications, the NOR compare unit can be modified as XNOR logic[1]. A part from storage and comparing unit, pull down transistor M is gate-control to compare results, and important to connecting and disconnecting ML from/to the ground.

A. Conventional NOR- Type CAM

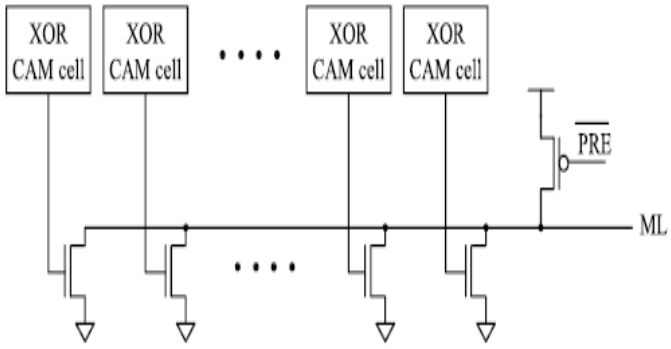

***Figure 2:** Conventional NOR-Type CAM[1]*

In CAM cell it is including XOR cell, every CAM cell pull-down transistor organized as NOR-type and it is connected to match line in above fig.2 shows conventional NOR-type CAM [1]. In a searching-operation two phase are there such as pre-charge phase and evaluation phase. In pre-charged phase, PRE=1 can pre-charged ML to high. After PRE is reduced to 0 its start the evaluation phase. In CAM-words single or more cell will be mis-match then ML dis-charge to 0. If all cells are match like input data equal to storing-data at that time ML continue high logic in pre-charged phase. And mis-matched case ML dis-charged to 0 instantly, because of pull down path is very short. NOR type CAM give best searching performances. In contrast to the NOR type CAM, the NAND type CAM reduces the power consumption in search operation but pull down path is too long so discharging of ML is very slow. Therefore, NOR type CAM trades the bad performance for a large amount of power saving [1], [3].

III. IMPLEMENTATION of CAM

A. Basic of MSML Design

The main plans to implement CAM design to combining the master-slave designs through charged-refilled minimize techniques decreases match-line switching power. In below fig.3 MSML design use single master-match line (MML) and two slave-match lines (SMLs) like SML_1, SML_2 as MS2 type and PRE=1 also given to all SMLs and after that PRE connected to NMOS type shared transistor and it is connected to FML. Where FML and MML both connected PMOS transistor and it is common connected to PRE=0. Here S1, S2 and P given as path of MML, SMLs and FML. Different from conventional-CAM it is used single match-line, in this designed using both MMLs/SMLs to execute searching operations. In When MMLs power dissipation minimizes at that time used SMLs [1].

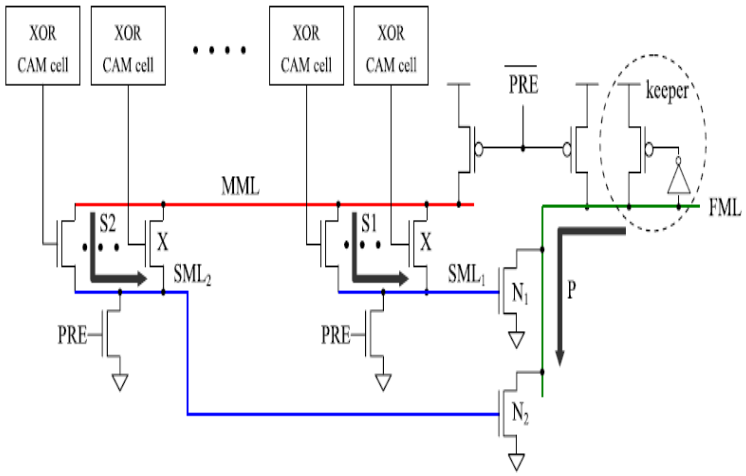

***Figure 3**: MSML Design[1]*

In conventional CAM, when mis-match condition occurred at that time MML discharged to 0. In MSML design, charge loss is less because only mis-match SMLs charges from MML and then discharge before dis-charging the overall MML to 0.After MML, SML and FML(Final Matching-Line) use to define match- result.

B. MSML Design Searching Operations MSML design work same as conventional-type design, in MSML two phase are there when searching-operations. There are pre-charged phase and match-evaluation phase [1].

(1)Pre-charged Phase: In pre-charged Phase PRE to high. Therefore, MML and FML both pre-charged to high, and each SML1 and SML2 which shown in Fig.3 are discharged to zero. In this phase Searching data will be not there, and charged-share path S1 and S2 both dis-connect.

(2)Match-evaluation Phase: End of pre-charged phase, PRE decreased to 0, searching-data to load in searching-line to start match process. It is depend on matched results of SML1 and SML2 in match-evaluation phase. In Table I path and key-node voltage are there and operation of different condition given below.

***Table 1:** Path and Key-node Voltages for every condition in the MSML Design*

	SML1	SML2	Path			Key-node Voltages				Results
			S1	S2	P	MML	SML1	SML2	FML	
Condition1	Match	Match	X	X	X	V_{dd}	0	0	V_{DD}	Match
Condition2	Mis-match	Match	0	X	X	2/3 V_{dd}	2/3 V_{dd}	0	0	Mis-match
	Match	Mis-match	X	0	0	2/3 V_{dd}	0	2/3 V_{dd}	0	Mis-match
Condition3	Mis-match	Mis-match	0	0	0	1/2 V_{dd}	1/2 V_{dd}	1/2 V_{dd}	0	Mis-match

Power consumptions and match-delay problem will be occurred in MSML design. When SML1 and SML2 both are mis-matched at that time worst condition occur. Above table I, increasing power consumption at that time when number of SMLs increased with the mis-matched SML numbers. When single SML is mis-match at that time only single pull-down transistor on to dis-charge the FML its worst condition for performances. Charged share to MMLs and SMLs, performances will be improving by increased the SMLs but it increased power.

C. XNOR Cell

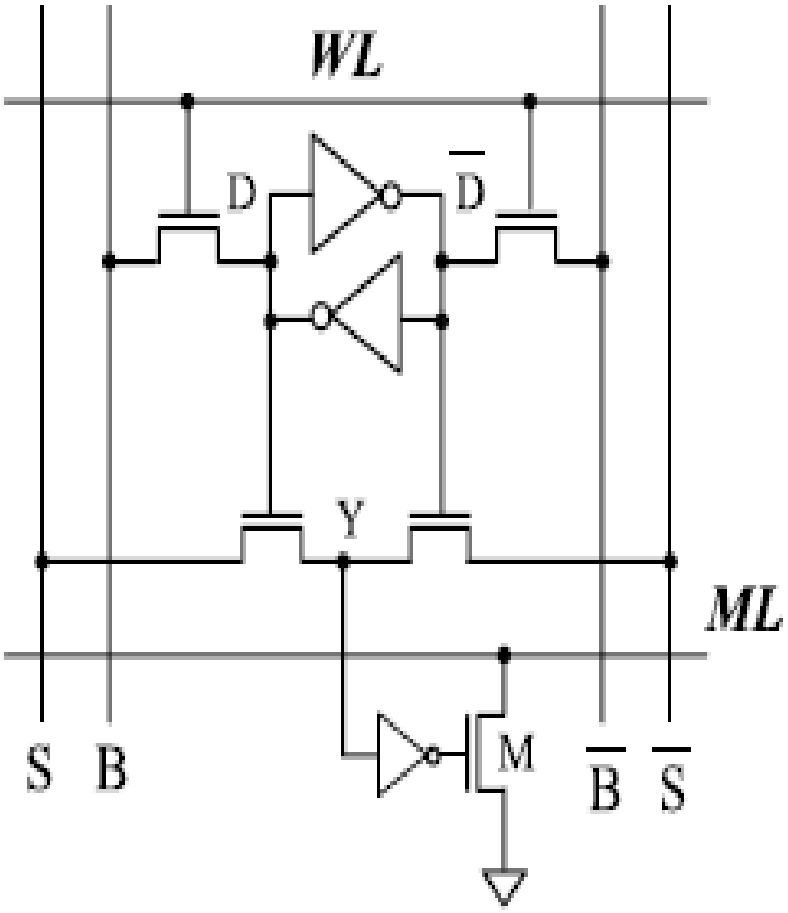

Figure 4: *XNOR Cell for Good Performance[1]*

The main disadvantages in conventional-CAM, is improving in above fig. 4 XNOR CAM cell for better searching-performance of MSML design. In that case conduction of NMOS is better than PMOS, the shared transistor (M) is still NMOS. Conventional XOR design is converted in to XNOR by adding extra inverter. So in above design shared transistor M remain in control compare to XOR design. XNOR CAM will improve charged-share speed as one can achieved in MSML. MSML design use of XNOR cell known as MSML_hp.

In MSML design mis-match condition is long compared to conventional-type where its divide in two parts: 1) charge-share to MML up the mis-match SML, 2) SMLs turn on pull-down transistor to discharged the FML. In different condition, MSML design will be minimize power consumption, it can be degrading searching performance too.

In upper analyze, dis-charging speed FML determine to mis-matching SMLs raise timing. It is implied MSML performances will improving via speed-up the charge-share to MML and SML.

D. Modify XNOR Cell

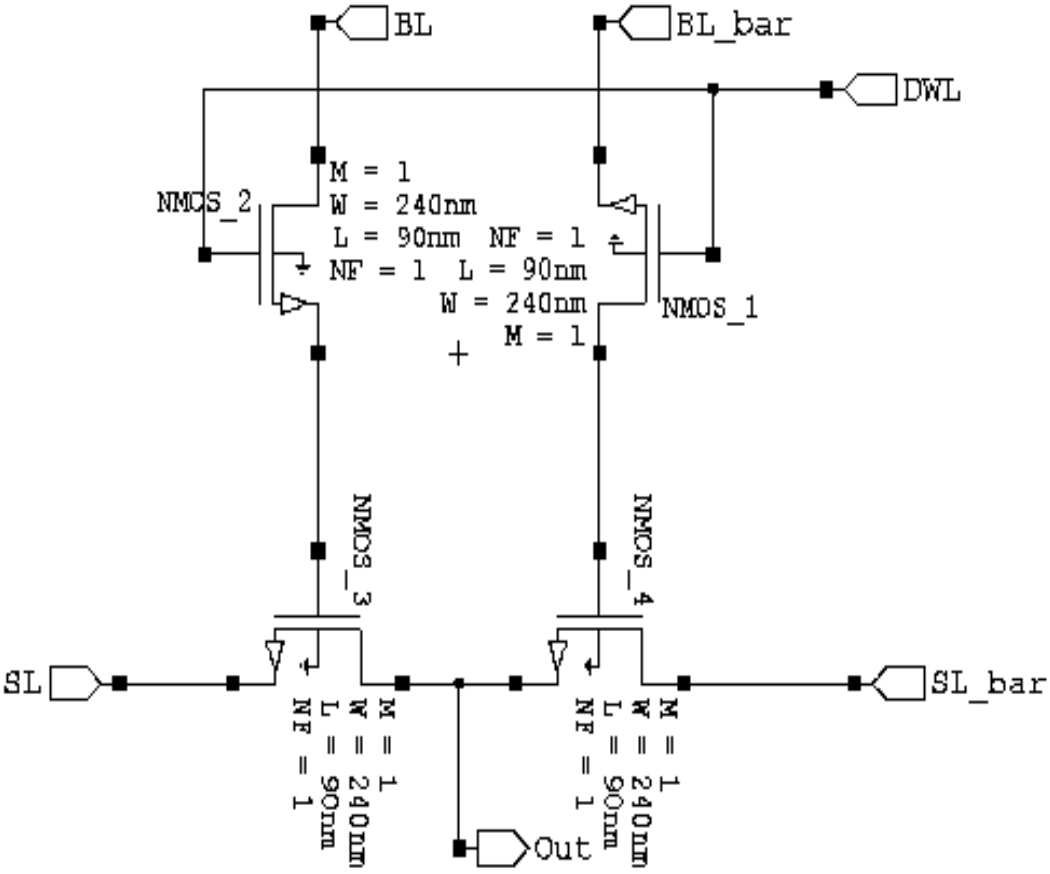

Figure 5: *Modify 4T XNOR CAM Cell[2]*

In MSML_hp improve the charge sharing speed and match-delay, and MSML_hp more power and area compare to conventional design. So overcome to that type of issue through modified XNOR CAM cell which given above fig.5.In modified XNOR CAM its use four NMOS transistor. In this two series NMOS transistor us as storage bit and two parallel NMOS transistor use as write the data.

Logic1 and Logic 0 both are act as output of match line, but in Logic 1 present that store data and input data matching by using pre- charged transistor and logic0 present that no mis-matching to store data and input data so the ML gets discharge by using pull down transistor [2]. So in modified XNOR cell lower power-consumption and high performance, also minimize area so at that time this circuit acts as good CAM design compare with other CAM design.

IV. SIMULATION RESULTS

Different implementation of CAM design types compare with conventional CAM design, and all design simulation are done with 90nm CMOS technology and Vdd = 1v in Tanner EDA version-13. All designs are implemented to different word size with different CAM arrays. All the comparison of performance, avg. ML power consumption, area overhead is given in Table II, Table III, Table IV for 1×4 bit, 4× 4 bit, 8× 8 bit respectively.

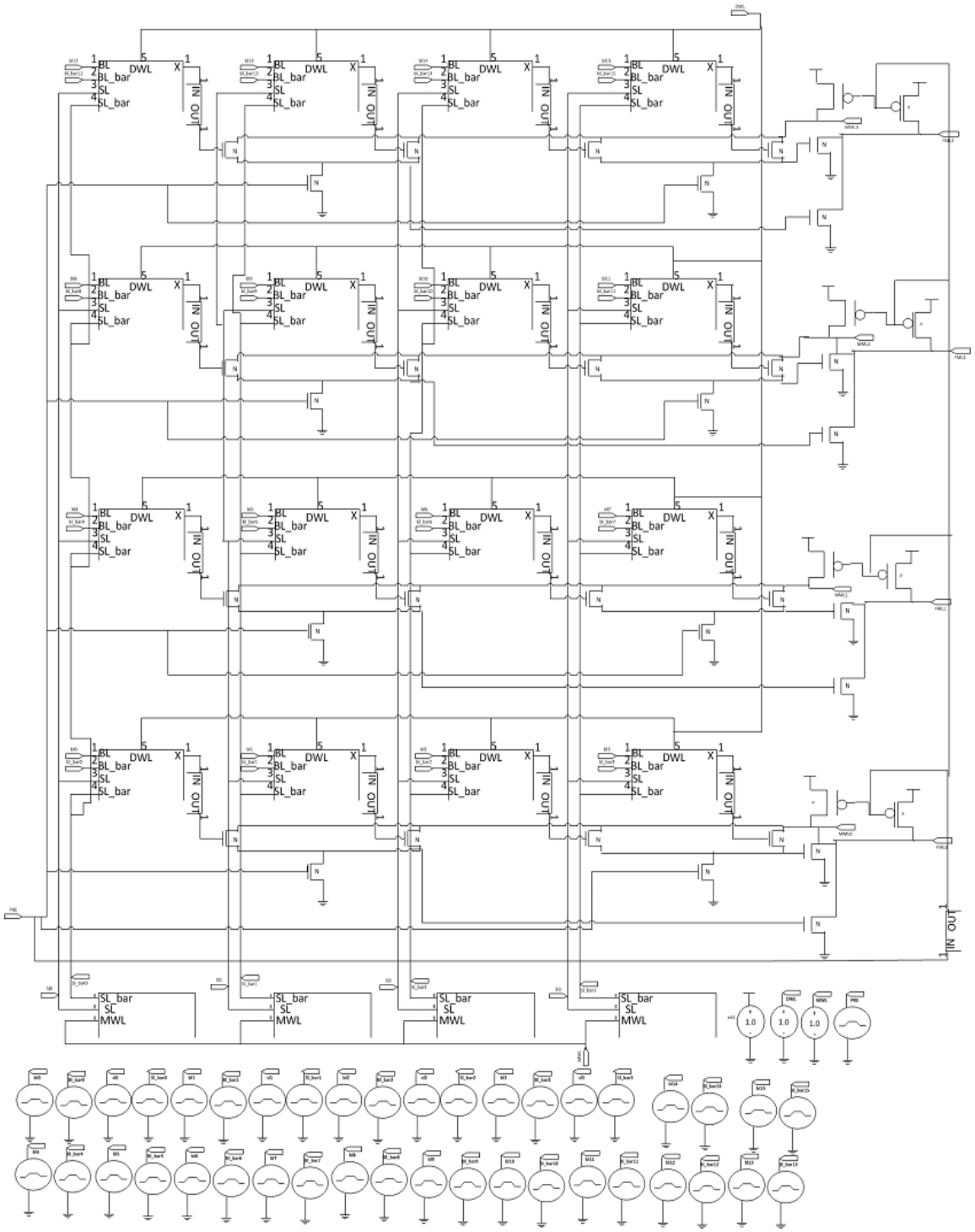

Figure 6: *Schematic of 4×4 bit Modified 4T XNOR Cell MSML Design*

In fig.6 4×4 bit modified 4T XNOR cell MSML design schematics shows and respective analysis (transient) is in fig.7 for mis-match condition. If storing data mis-match with searching data, MML is ½ Vdd in evaluation phase, SMLs are remaining high and FML discharge to 0.

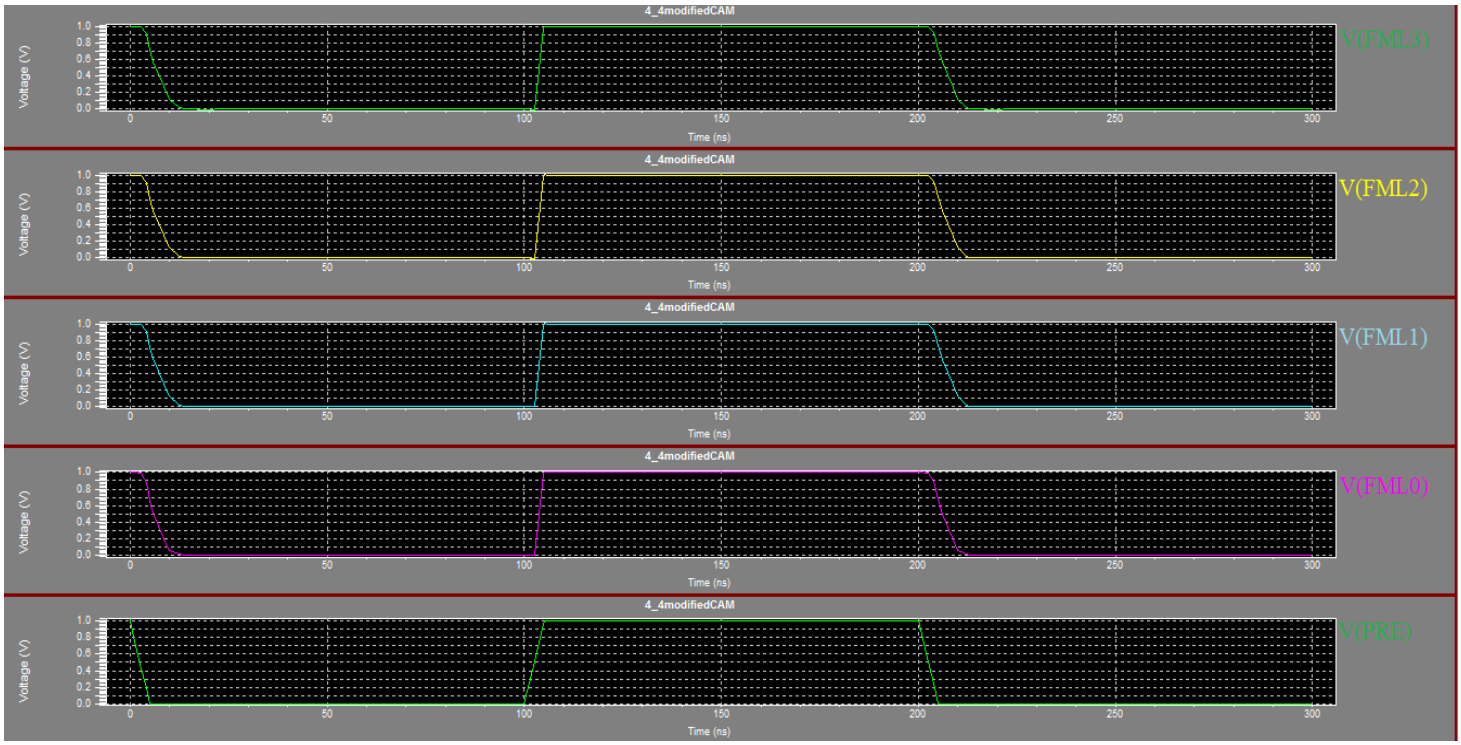

Figure 7: *Transient Simulation of 4×4 bit Modified 4T XNOR CellMSML Design (Mis-match Condition)*

A. Performance

Performance analyzed in term of matching-delay (MD) in MSML CAM, in mis-match condition performance define as the passing time from PRE=0 to the FML discharged to 0. Increase in mis-match SMLs with MD will be decreasing. In conventional type CAM MD is different of SMLs numbers that mean constants. In table II performance of different CAM designs.

Table 2: *Performance for different CAM Design*

Performance (ns) of CAM	**1×4 CAM**	**4×4 CAM**	**8×8 CAM**
Conventional	83.87	85.2	95.0
MSML	12.85	21.1	14.6
MSML_hp	5.62	6.3	4.5
Modified XNOR	4.77	5.60	4.0

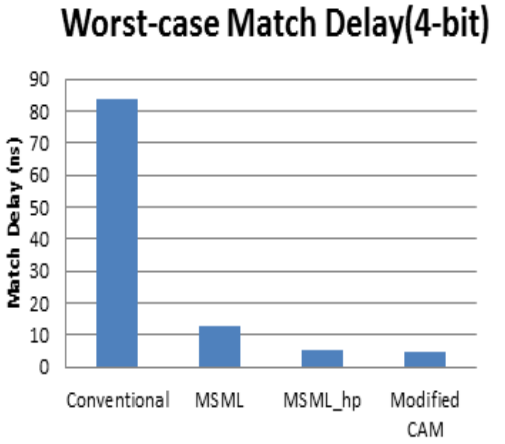

Figure 8(a)

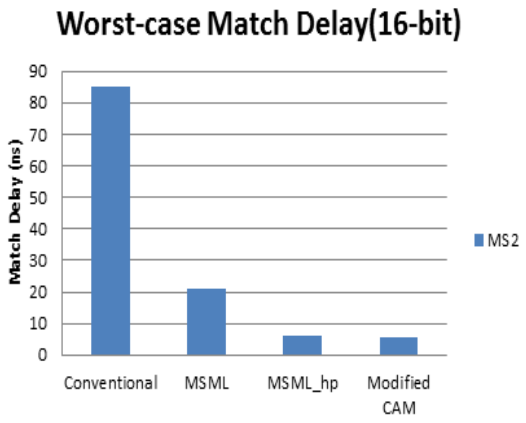

Figure 8(b)

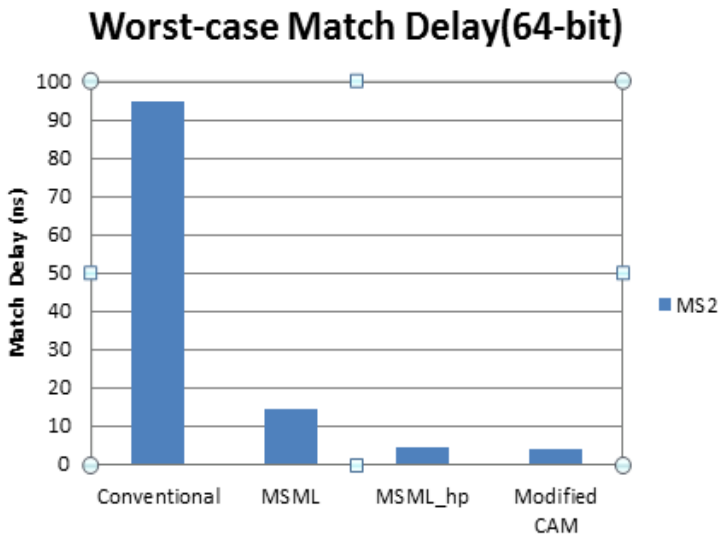

Figure 8(c)

Figure 8. Worst-case MD for different CAM designs (a) 4-bit size (b) 16-bit size (c) 64-bit size

B. Power Consumption

In below Table III average ML power consumptions for different CAM design with different size. Here for all mis-match condition power consumption will be measured. If SMLs smallest at that time Power consumptions is decreased. Compared to different MSML designed in MSML_hp more power consumption. MSML_hp modified as 4T XNOR CAM cell which give less power consumption compared to other design.

Table 3:Mis-match Power Consumption for different CAM Design

Mis-match Power Consumption (µW) of CAM	**1×4 CAM**	**4×4 CAM**	**8×8 CAM**
Conventional	42.55	182.70	414.95
MSML	37.90	91.60	330.04
MSML_hp	41.44	99.89	354.26
Modified XNOR	31.90	87.15	184.16

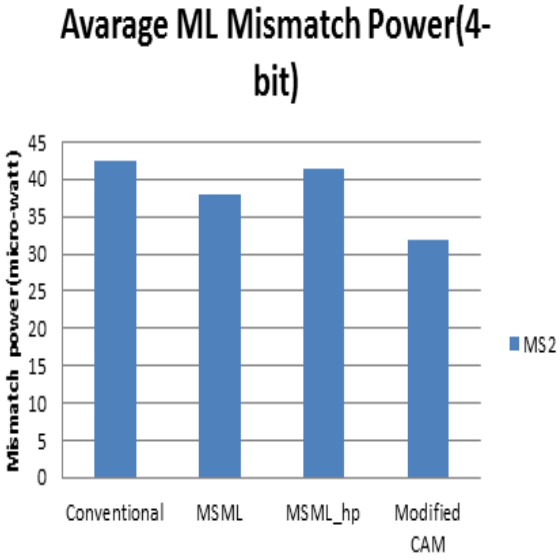

Figure 9(a)

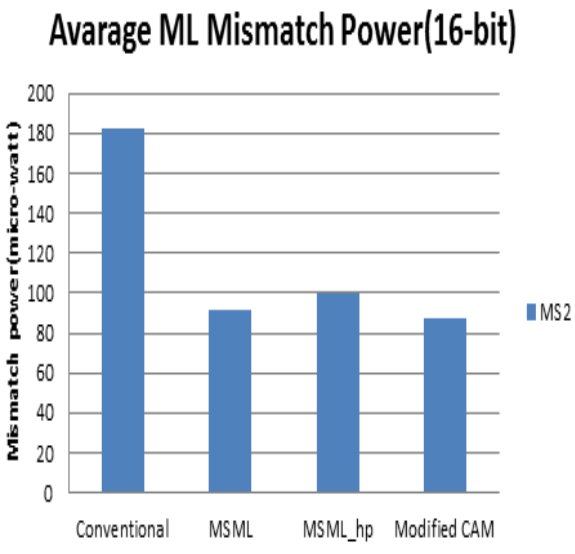

Figure 9(b)

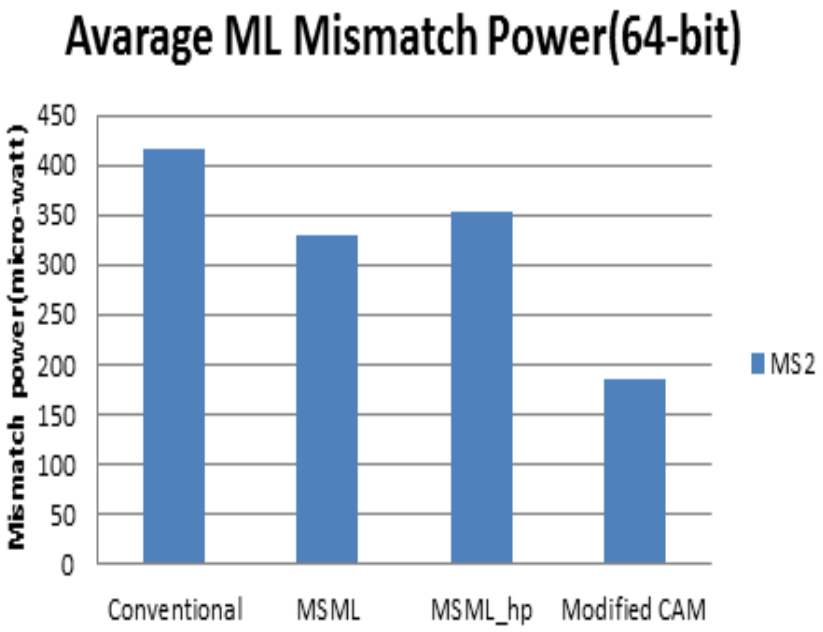

Figure 9(c)

Figure 9: Average ML mis-match power consumption for different CAM designs (a) 4-bit size (b) 16-bit size (c) 64-bit size

C. Area Overhead

In MSML and MSML_hp design include number of transistor and wires for low power compared with conventional CAM. Compare to other design modified XNOR cell reduced transistor count, and area will be measured on transistor count. So in modified XNOR reduced transistor count means less area required. In below Table IV area overhead for different CAM design.

Table 4*: Area Overhead for different CAM Design*

Transistor Count CAM	**1×4 CAM**	**4×4 CAM**	**8×8 CAM**
Conventional	63	174	634
MSML	68	202	674
MSML_hp	76	326	802
Modified XNOR	60	162	546

V. CONCLUSION

Here low power ML designs introduce to reduce switching-activity of ML. In conventional cell more power and larger area required so overcome this problem MSML design introduced. And for larger bit design implementation of CAM design good compared to lower bit. Compare to all design in modified XNOR CAM cell give high performances, low power consumption and area also minimize for all mis-match condition.

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