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Performance Evaluation of SRAM CELL Sense Amplifiers

L Rangaiah[1]
Ph.D Scholar, Rayalaseemauniversity
Kurnool

K. Srinivasa Rao[2]
TRR College of Engineering
Hyderabad

Rajendraprasad S[3]
VNR VJIET, Hyderabad

INTRODUCTION

SRAMs are used as cache memory; hence it must perform both read & write operations at high speed along with low power consumption. But its peripheral circuits can adversely affect the overall speed and power of the system. Among all the peripherals of a SRAM memory, sense amplifier plays a major role. It is used to sense or read the data stored or written onto the selected memory bit. The performance of sense amplifiers strongly affects both memory access time and overall power consumption. Sense amplifier is thus used to convert this small voltage swing to a full logic signal [1-4]. To improve the speed and overall performance of memory it is necessary to understand and analyze different types of sense amplifiers. According to the demand of situation appropriate sense amplifier must be used as every design has its own advantage and disadvantage. The main aim of the paper is to design the SRAM cell with different sense amplifiers using HSPICE and calculate various performance characteristics and compare them.

Keywords: SRAM, Sense Amplifier, CSA, VSA, CTSA, Power, Delay

1. SENSE AMPLIFIERS

In modern computer memory, a sense amplifier is one of the elements which make up the circuitry on a semiconductor memory chip (integrated circuit); the term itself dates back to the era of magnetic core memory. A sense amplifier is part of the read circuitry that is used when data is read from the memory; its role is to sense the low power signals from a bit-line that represents a data bit (1 or 0) stored in a memory cell, and amplify the small voltage swing to recognizable logic levels so the data can be interpreted properly by logic outside the memory [5-8]. Modern sense-amplifier circuits consist of two to six (usually four) transistors, while early sense amplifiers for core memory sometimes contained as many as 13 transistors. There is one sense amplifier for each column of memory cells, so there are usually hundreds or thousands of identical sense amplifiers on a modern memory chip. As such, sense amplifiers are one of the only analog circuits in a computer's memory subsystem. The design objectives of sense amplifier includes Minimum sense delay, Required amplification, Minimum power consumption, Restricted layout and High reliability and Tolerance.

There are different types of sense amplifiers that can be used in SRAM, but in this paper the following three sense amplifiers are designed:

i) Cross Coupled Voltage Sense Amplifier
ii) Current Sense Amplifier
iii) Charge Transfer Sense Amplifier

The simplest Voltage Sense Amplifier is the differential couple. When a cell is being read, a small voltage swing appears on the bit line which is further amplified by differential couple and use to drive digital logic. However the bit line voltage swing is becoming smaller and is reaching the same magnitude as bit line noise, the voltage sense amplifier become unusable.

The fundamental reason for applying current mode sense amplifier in sense circuit is their small input impedances. Benefits of small input and output impedances are reductions in sense circuit delays, voltage swings, cross talking, substrate currents and substrate voltage modulations. The operation of the CTSA is based on the charge re distribution mechanism between very high bit line capacitance and low output capacitance of the sense amplifier. A differential charge transfer amplifier takes advantage of the increased bit-line capacitance and also offers a low-power operation without sacrificing the speed [9-12].

1.1. CROSS COUPLED VOLTAGE SENSE AMPLIFIER (VSA)

Sense amplifier which detects the voltage difference on the bit lines is called voltage mode sense amplifier. There are some voltage mode sense amplifiers like single ended sense amplifiers, differential amplifiers and Cross coupled sense amplifiers. Different types of sense amplifier are used in different types of memory cells according to the proper design and efficient performance.

In the circuit shown IN Fig. 1, M1- M4 forms cross-coupled inverters whereas M5 is the driver transistor. There is voltage on BL and BLB which are charged and discharged when the read operation is initiated and are connected to this sense amplifier. Due to positive feedback, higher voltage level goes to VDD and other level goes towards zero. In the basic cross-coupled SA, the nodes BL and BLB are input and output terminals at the same time.

Let us suppose that the bit stored in the memory cell is logic '1' i.e., Q=1 so thus bit stored in QB=0. Due to this, voltage on BL remains constant but voltage on BLB discharges to certain extent. This BL voltage is charged to

VDD and the BLB voltage goes to zero. With this, due to the voltage VDD on BL, it is determined the bit stored in cell is '1'.

The following fig. 1 shows the circuit of cross coupled voltage sense amplifier.

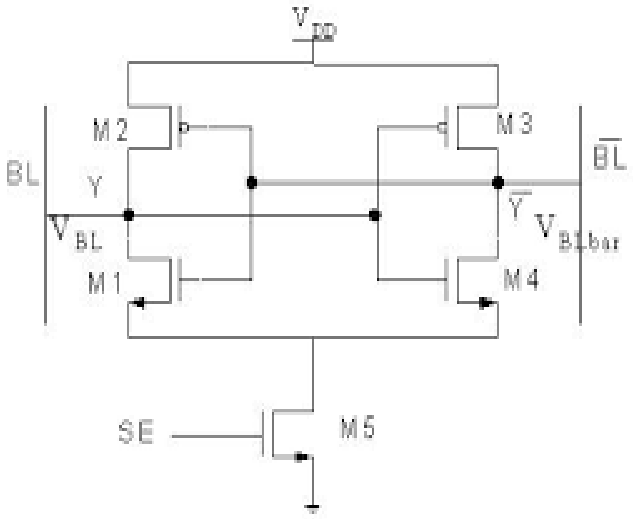

Fig. 1: Cross Coupled Voltage Sense Amplifier

The W and L values of the transistors used in the memory cell are given by:
Width of NMOS is 0.245µm and its length is 0.18µm making the w/l ratio equal to 1.36. Width of PMOS is 0.2µm and its length is 0.18µm making the w/l ratio equal to 1.11.Width of Access transistors NMOS is 0.3µm and its length is 0.2µm making the w/l ratio equal to 1.5. The transistors used in sense amplifier have the following respective w and l values. NMOS transistors (M1 and M4) has a width of 0.6µm and length of 0.18µm making the w/l ratio equal to 3.3. PMOS transistors (M2, M3 and M5) has a width of 2.5µm and length of 0.18µm making the w/l ratio equal to 13.8.

1.2. CURRENT SENSE AMPLIFIER (CSA)

In advanced memories the capacitances of the bit line is increasing due to technology scaling and the increasing number of cells attached to the column. In such memories voltage mode cannot keep up to their performance thereby leading to the need for faster sensing techniques that are not affected by the bit line capacitance. Current sensing is typically 17-20% faster than voltage sensing. Current Sense Amplifier can be enabled faster than voltage mode, as current sensing does not depend on differential discharging of large bit-line capacitance. The bit-line swing for current sensing is 35-40% less than the voltage mode, but the energy saved with reduced bit-line swing is compensated by the static power dissipation of the current sense amplifier.

Current mode sense amplifiers (shown in fig.2) are applied to reduce the sense circuit delays as they provide low common input/output impedances. The small input impendence presented to the bit-lines result in reduced voltage swings, cross-talk and substrate currents.

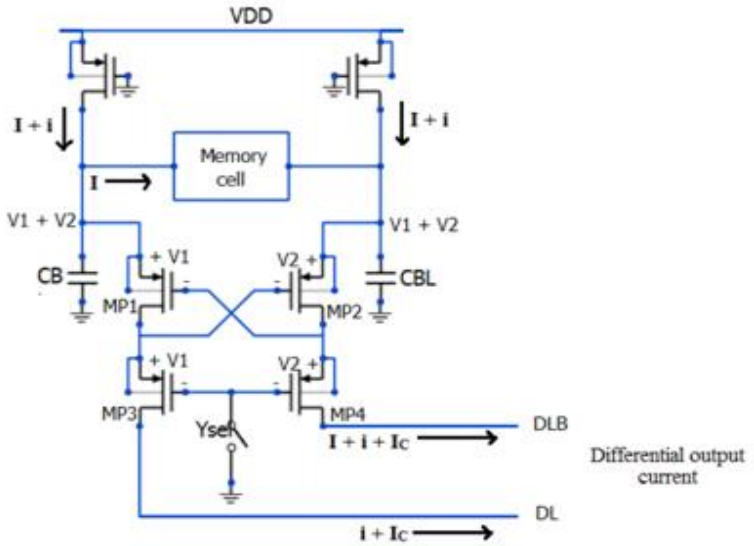

Fig. 2: Current Sense Amplifier

Current mode sense amplifier is used to detect the current difference between the bit lines to determine whether a '1' or '0' is stored in the memory cell. It directly measures the cell read current and transfers to the output circuits. This approach can overcome the restriction of gain reduction brought on by voltage mode sense amplifier at low power supply voltage. The simplest structure of the current mode sense amplifier is described in Fig. 2.

The Conventional Current Sense Amplifier basically consists of four equal sized PMOS transistors as shown in Fig.2. It features a current sensing character since it represents a virtual short circuit to the bit lines, which transfer the cell current directly to the output circuits. If memory cell stores '0' then when it is accessed, it draws some current. The difference in the current flowing through both branches will be equal to cell current. The current in DLB is higher than current in DL as shown in Fig.2. This differential current is used to find whether the stored bit in the SRAM cell is either 0 or 1.

The W and L values of the transistors used in the memory cell are given by:

Width of NMOS is 1µm and its length is 50nm making the w/l ratio equal to 20. Width of PMOS is 1.5µm and its length is 50nm making the w/l ratio equal to 30. Width of Access transistors NMOS is 1.5µm and its length is 50µm making the w/l ratio equal to 30. The transistors used in this sense amplifier are all PMOS transistors (MP1, MP2, MP3 and MP4) and have the following respective w and l values. PMOS transistor has a width of 0.1µm and length of 50µm making the w/l ratio equal to 2.

1.3. CHARGE TRANSFER SENSE AMPLIFIER (CTSA)

The Charge Transfer Sense Amplifier (CTSA) operates by making use of the charge redistribution from high capacitance bit-lines to the low capacitance sense amplifier output nodes. This results in high speed operation and lower power consumption due to low voltage swing on the bit-lines. The circuit diagram of a CTSA is shown in Fig. 3. The basic concept behind charge-transfer amplification is to produce voltage gain by exploiting charge conservation among capacitive devices. For a series connection of two capacitive elements in a system for which charge is conserved, the product of the voltage across the first element and its capacitance must be equal the product of the voltage across the second element and its capacitance as shown in the following equation.

Csmall * Vsmall = Q = Clarge * Vlarge

The basic operation of CTSA is based on the charge redistribution from high bit-line capacitance to the low capacitance of the nodes Sa and Sa#. This charge redistribution results in high-speed operation and low bit line swing.

The circuit consists of two parts. First is the common gate cascade formed by M1, M3 and M5 (and M2, M4 and M6), with PMOS M1 and M2 biased at Vb. Second, the cross-coupled inverters formed by M7 through M11 latches the output of the common-gate amplifier (Sa and Sa#). In the pre-charge phase, the bit-lines and all the intermediate nodes (A, B, C and D) are pre-charged high. The output of the common-gate amplifier (Sa and Sa#) is pre-discharged low by keeping SAen high. In the evaluation phase, Pch is pulled high and Ysel is grounded to select a column. CTSA is enabled by pulling SAen low. Suppose, the bit-line bl# is going low. As the voltage of the bl# goes near Vb + |Vthp|, M1 goes into sub-threshold region of operation preventing the output node Sa# from getting charged. However, the other bit-line bl remains high and charges the output node Sa to high. Initially, NMOS pair M10 and M11 helps in rejecting the common-mode noise and thereafter helps in latching the value sensed by the common gate amplifier.

The bias voltage Vb is set at 0.3V. It is critical to set this voltage at the right value as the charge transfer device M1/M2 cuts off when its input source voltage falls to Vb + Vtp. Setting Vb at a higher value causes the charge transfer device to be cut off early and not have the differential voltage propagate to the sense nodes Sa and Sa#. Setting this voltage too low prevents the charge transfer device from entering the sub-threshold region and causes the cross coupled positive feedback inverter to further discharge the bit-line resulting in higher pre-charge power.

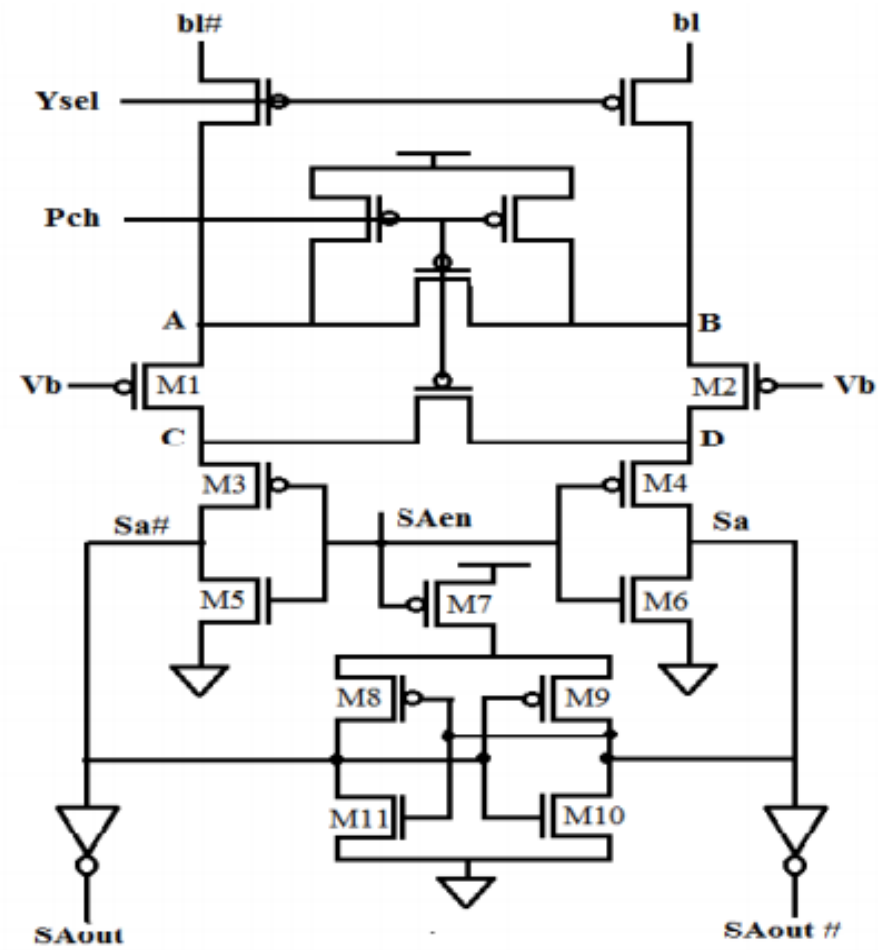

Fig.3: Charge Transfer Sense Amplifier

The W and L values of the transistors used in the memory cell are given by:
Width of NMOS is 1.5µm meters and its length is 50nm making the w/l ratio equal to 30. Width of PMOS is 1µm and its length is 50nm making the w/l ratio equal to 20. Width of Access transistors NMOS is 1µm and its length is 50 nm making the w/l ratio equal to 20. The pre-charging transistors of this sense amplifier are all PMOS transistors (M1 and M2) having width of 0.25µm and length of 50nm making the w/l ratio equal to 5. The remaining transistors have the following values of NMOS transistors (M5, M6, M10 and M11) have a width of 0.25µm and length of 50µm making w/l ratio equal to 5. PMOS transistors (M3, M4, M7, M8 and M9) have a width of 4µm and length of 50 nm making w/l ratio equal to 80.

2. RESULTS

The various sense amplifier circuits are implemented in HSPICE (H Simulation Program for Integrated Circuit Emphasis) and their performance is evaluated by calculating various parameters like read delay, average power and area of the circuit (in terms of number of transistors) in the 45nm technology with the power supply V_{DD} = 3V.

2.1. CROSS COUPLED VOLTAGE SENSE AMPLIFIER (VSA)

The waveforms of Cross Coupled Voltage Sense Amplifier are shown below in the fig. 4. The nodal voltages are described as V(1) = V(q1) where q1 is the complement of the bit stored in the cell, V(2)=V(q) where q is the bit stored in the cell, V(3)= V_{DD}, power supply of the circuit, V(4)= V(bl) and V(5)=V(bl1) where bl is the bit-line associated to q and bl1 is the bit-line associated to q1. These bit-line are used as reference lines for read and write operations taking in SRAM cell. Finally, for selection of this particular memory cell word line has to be high and it is given by V(6)=V(wl) and V(7)=V(pc) , here, pc stands for pre-charging of bit lines which is mandatory for read operation.

Initially, pre-charging is on and word-line is off i.e., pre-charging signal is high and word-line signal is low and the bit stored in cell is given by q which is shown in figure as 3V and thus, q1 reads 0V as it is the complement of q. During this phase, both bl and bl1 are pre-charged to certain value and then when word-line goes high, the cell is selected and based on the values stored in their respective q q1, the corresponding bl and bl1 charge and discharge. As the value stored in the bit is logic 1, q=3V and q1=0V so, bl1 is discharging and bl is charging. Eventually, at the end of cycle, bl reaches 3V and bl1 becomes 0V thus helping us in determining the stored bit in the cell.

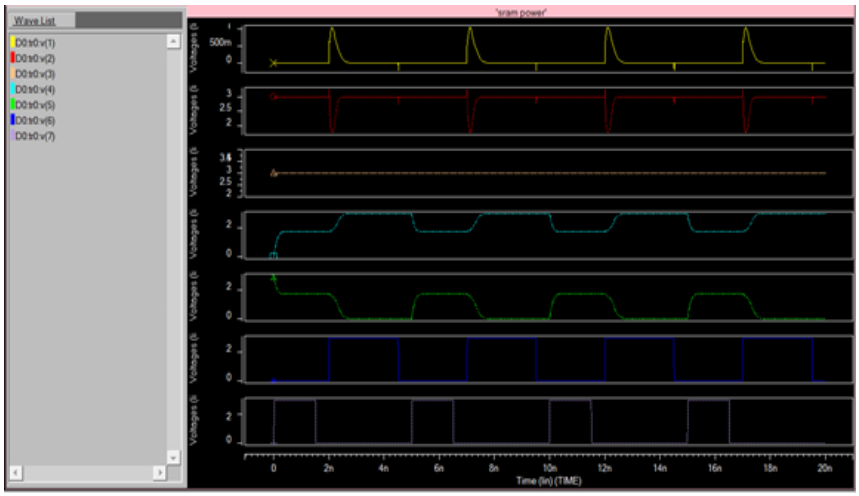

Fig.4: Simulated waveforms of Cross Coupled Voltage Sense Amplifier

2.2. CURRENT SENSE AMPLIFIER (CSA)

The waveforms of Current Sense Amplifier are shown below in the fig. 5. The nodal voltages are described as V(1) = V(q) where q is the bit stored in the cell, V(2)=V(q1) where q1 is the complement of the bit stored in the cell, V(3)= V_{DD}, power supply of the circuit, V(4)= V(bl) and V(5)=V(bl1) where bl is the bit-line associated to q and bl1 is the bit-line associated to q1. These bit-line are used as reference lines for read and write operations taking in SRAM cell. V(op) and V(op1) denote the output lines. Finally, for selection of this particular memory cell word line has to be high and it is given by V(6)=V(wl).

Initially, pre-charging is on and word-line is off i.e., pre-charging signal is high and word-line signal is low and the bit stored in cell is given by q which is shown in figure as 3V and thus, q1 reads 0V as it is the complement of q. During this phase, both bl and bl1 are pre-charged to certain value and then when word-line goes high, the cell is selected and based on the values stored in their respective q q1, the corresponding bl and bl1 charge and discharge. As the value stored in the bit is logic 1, q=3V and q1=0V so, bl1 is discharging and bl is charging.

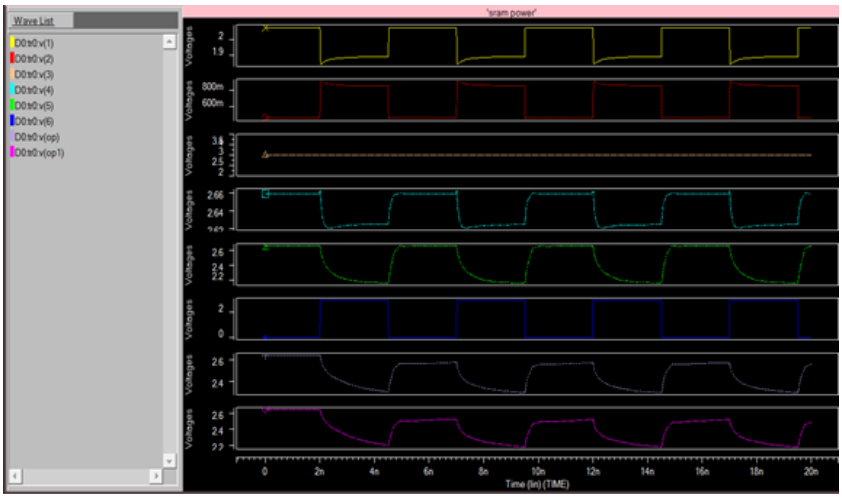

Fig. 5: Simulated waveforms of CSA

The op and op1 are the results obtained where it is clear that op decreases to a value around 2.3V whereas op1 decreases to a value 2.2V. This small difference on op and op1 lines is considered and the bit stored in the cell is read out. As the difference between op and op1 is positive, the bit stored in the memory cell is logic 1. If the difference between op and op1 is negative, then it is evident that the bit stored in memory cell is logic 0.

2.3. CHARGE TRANSFER SENSE AMPLIFIER (CTSA)

The waveforms of Charge Transfer Sense Amplifier are shown below in the fig. 6. The nodal voltages are described as V(8) = V(q) where q is the bit stored in the cell, V(7)=V(q1) where q1 is the complement of the bit stored in the cell, V(3)= V_{DD}, power supply of the circuit, V(bl) and V(bl1) represent bit-line voltages, V(saen) is the sense amplifier enable signal which turns on the amplifier after the discharging and charging of bit-lines, V(ysel) and V(pch) are for the pre-charging of sense amplifier. Finally V(sa) and V(sa1) are the outputs of the sense amplifier.

After the charging and discharging of bit-lines bl and bl1, in the pre-charge phase, the bit-lines and all the intermediate nodes (A, *B, C* and *D)* are pre-charged high. The output of the common-gate amplifier *(Sa* and *Sa1)* is pre-discharged low by keeping saen high. In the evaluation phase, pch is pulled high and ysel is grounded to select a column. CTSA is enabled by pulling *saen* low. Here, bl1 is discharging faster and to a smaller value and thus sa1 is low and sa is high. The bit stored in the cell is given by sa.

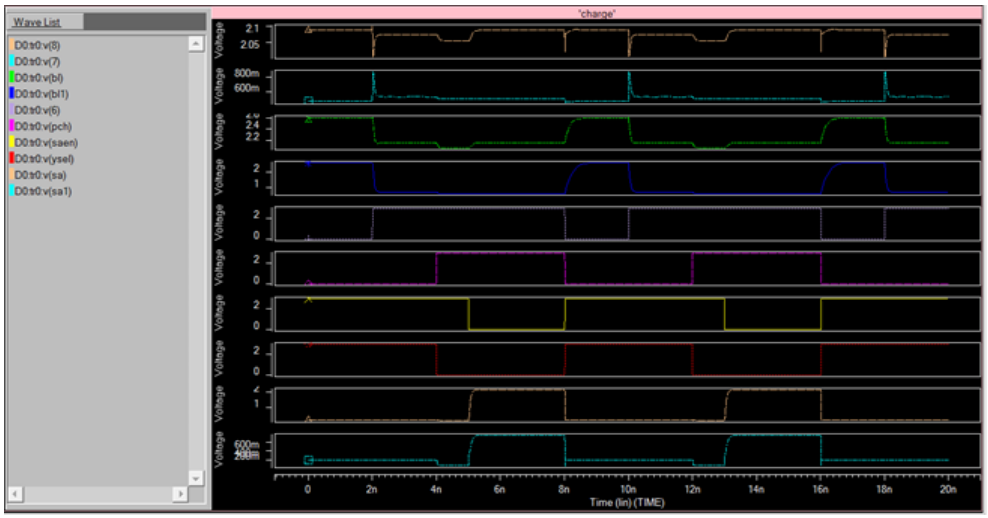

Fig. 6: Simulated waveforms of CTSA

2.4. COMPARISON OF THREE SENSE AMPLIFIERS

The Table 1 shows the comparison of different parameters among the three sense amplifiers.

Table 1: Comparison of three sense amplifiers

Parameter	Average Power (mW)	Read Delay (ns)	No. of Transistors
VSA	1.19	0.14	5
CSA	26.7	0.07	6
CTSA	16.3	0.0019	17

The following Fig. 7 shows the representation of comparison of delay parameter between the three different circuits of sense amplifier. It shows that voltage sense amplifier has more delay (0.14 ns) compared to the current sense amplifier which has 0.07ns delay. Among the three circuits, charge transfer sense amplifier has very less delay of 1.9ps.

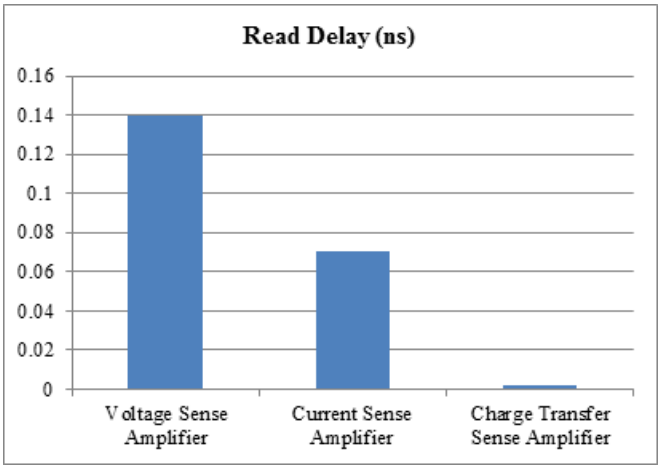

Fig. 7: Comparison of read delays of different sense amplifiers

The Fig. 8 shows the representation of comparison of average power parameter between the three different circuits of sense amplifier. It shows that voltage sense amplifier has less average power (1.19mW) compared to the current sense amplifier which has 26.7 mW and also charge transfer sense amplifier which has 16.3mW

The Fig. 9 shows the representation of comparison of number of transistors in different sense amplifier circuits. It shows that voltage sense amplifier has less number of transistors (5) thereby has less area than current sense amplifier

which has 6 transistors. Among the three circuits, charge transfer sense amplifier has more area since it has more number of transistors (17).

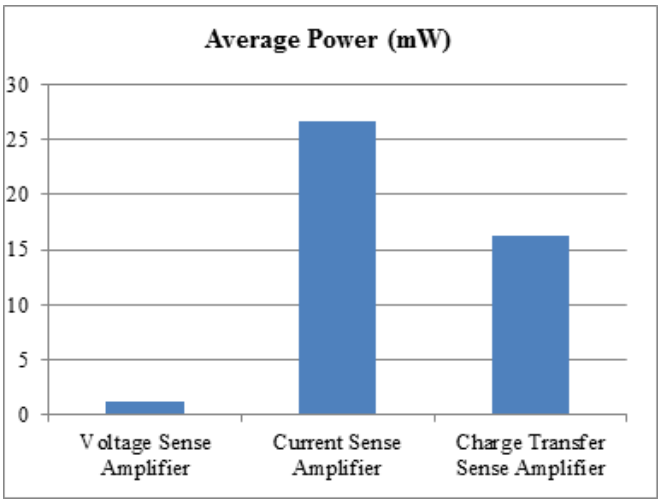

Fig. 8: Comparison of average power of different sense amplifiers

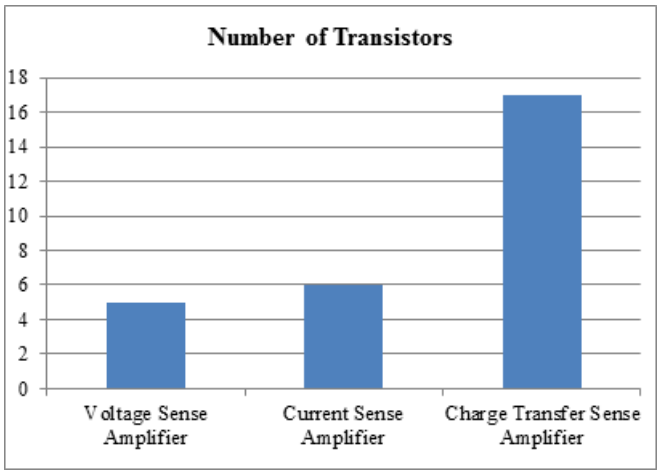

Fig.9: Comparison of number of transistors in different sense amplifiers

3. CONCLUSION

This paper presented the performance evaluation of three different sense amplifier topologies – Voltage Sense Amplifier (VSA), Current Sense Amplifier (CSA) and Charge Transfer Sense Amplifier (CTSA) by implementing them using HSPICE in 45nm technology with a supply V_{DD} of 3V. The comparison of different parameters between these three circuits is shown in the Table 1. It shows that among the three topologies, CSA is the best choice with minimum delay. CSA is faster than VSA with reduction in delay. But it consumes more power dissipation than VSA and CTSA. CTSA shows reduction in delay compared to VSA. Now, power obtained in VSA is 1.19mW which is less than CSA having 26.7mW whereas the read time delay in voltage sense amplifier is 0.14ns which is greater than 0.07ns of CSA. Thus, using CTSA, read time delay problem overcame by having done read operation in only 1.93 ps.

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