International Journal of Advance Engineering and Research Development (IJAERD)
Volume 1,Issue 6,June 2014, e-ISSN: 2348 - 4470 , print-ISSN:2348-6406

Novel Memristor Logic Gates: A New Paradigm In Electronics

Deepa A[1], SRS Prabaharan[2]

[1]School of Electronics Engineering, VIT University, Chennai, deepaagp@gmail.com
[2] School of Electronics Engineering, VIT University, Chennai,prabaharan.srs@vit.ac.in

Abstract: Memristor is referred to as a non-linear resistor. Memristor changes its state according to the amount of current passing through its terminals. Even though the electrical bias is removed, the memristor retains its state. It is the leading candidate for future solid state memories as well as logic applications. This paper focuses on implementation of basic logic gates using memristors. A logic gate can be described as a physical device through which Boolean function is implemented. As a case study flip-flops are implemented.

Keywords: Memristor, non-volatile, linear ion drift model, TEAM model, flip-flops.

I. INTRODUCTION

A huge success in the field of semiconductor devices was observed in 20th century with the introduction of transistors. Shrinking of CMOS devices into nanoscale regime has led to the use of multicore architectures in CPU to increase the performance. In sub 100nm regime, FET suffers from practical issues like short channel effect. This effect prevents FET from operating normally. There is alsoan increase in power dissipation due to sub-threshold slope non-scaling. Hence the performance of the transistor is limited as scale down increases. At present the challenge of semiconductor technology is the requirement of a new technology which combines the advantages of existing memories.

As a result a new technology is evolved which involves properties like high density, fast speed and non-volatile and is known as RRAM. Hence Resistive Random Access Memory (RRAM) is an emerging next-generation non-volatile memory which shows promise towards achieving faster operation speed. Memristor is one such device. It can store information and can also switch between different states. It is a two terminal device. Other upcoming conceptual RAMs which are under close scrutiny are Magneto resistive random access memory (MRAM), phase change RAM (PCRAM), and Spin Torque Transfer Magnetic Random Access (STT-MRAM).

There are a number of upcoming methods in recent technology which finds memristive applications. Memristor finds applications in fields like analog circuits, neuromorphic systems and logic circuits. Memristors basic property is data storage. i.e. it serves as a memory element. The information is stored in the form of resistance.

The main goal of this paper is to implement logic gates using memristor as a basic element. The behavior of the logic gates can be realized using the truth table. AND, OR, NOT are the basic logic gates. In electronics, every circuit is basically made up of logic gates. A logic gate can be described as a physical device through which Boolean function is implemented. Logic gates can be analyzed using transistors and memristors. The main focus here the use of bipolar memristive device made of TiO_2.

@IJAERD-2014, All rights Reserved

Section II gives the concept of memristor followed by Section III which describes the proposed model: memristive implementation of logic gates and Section IV presents the case study: implementation of flip flops using memristor and section V presents the result. Section VI concludes the paper by summarizing the advantages of the proposed model over the existing model.

II. MEMRISTOR

The most basic passive circuit elements are Resistor, Capacitor and Inductor. Memristor which is said to be the missing element is the fourth basic passive circuit element and was originally realized conceptually by Leon Chua in 1971[1]. Recently, after almost 3.5 decades, in 2008, researchers at Hewlett Packard (HP) Lab's reported that the memristor can be realized physically using two-terminal titanium-di-oxide (TiO_2) which is a nanoscale device [2]. The term Memristor is coined by the contraction of 'memory-resistor', as the exact function ofit is, to remember the history. The major difference between a memristor and other passive elements is the non-linear characteristics. Memristor is a non- linear device which maintains the functional relationship between time integrals of current and voltage. A current controlled time-invariant memristive system is defined as:

$$\frac{dw}{dt} = f(w,i) \quad \ldots\ldots\ldots(1)$$

$$V(t) = R(w,i) * i(t) \quad \ldots\ldots\ldots(2)$$

$$M(q) = \frac{d\phi}{dq} \quad \ldots\ldots\ldots(3)$$

Where M is memristance, i(t) is memristor current, w is internal state, variable t is time

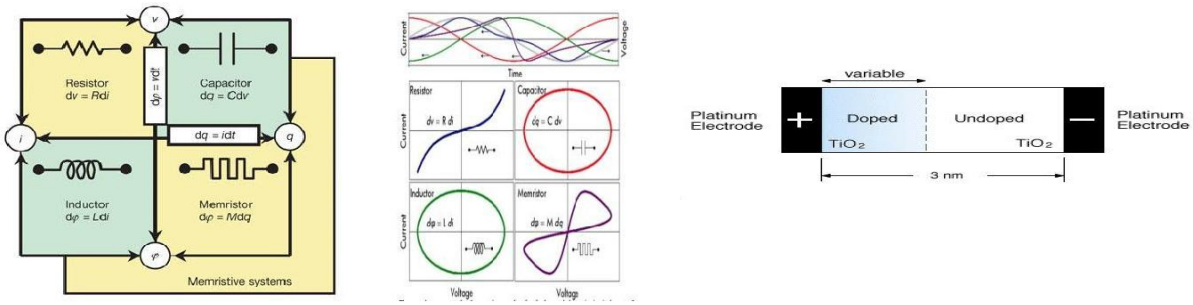


Fig 1: a) Relation between four passive elements. b) i-v curve of passive elements
c) Cross-section of Memristor depicting the internal structure of Memristor [Fig. 1(a) is adapted from Ref. [2]]

III. MEMRISTOR BASED LOGIC CIRCUIT DESIGN

The main focus here the usage of bipolar memristive device employing TiO_2. In this device, resistance depends on the direction of current flow. The polarity and symbol are shown:

@IJAERD-2014, All rights Reserved

Fig 2: Memristor symbol

When current flows into the thick black line the memristance decreases. When current flows out of the thick black line the memristance increases. There are several models like: linear ion drift model, non-linear ion drift model, Simmonds tunnel barrier model, TEAM model. This paper focuses on linear-ion drift model and also the TEAM model. It also describes the advantage of TEAM model over other models. HP labs developed the linear ion model for the first time to introduce memristor. The model assumes that charged ions are free to move under the influence of large field, this movement changes the conductance of the media. The integral portion of the TEAM model is based on an expression for the derivative of the internal state variable that can be fitted to any memristive device type.

Linear ion drift model is described by equation:

$$\frac{dw}{dt} = u * Ron * \frac{i(t)}{D} \text{.....(4)}$$

$$v(t) = (Ron * \frac{w(t)}{D} \quad + \quad Roff(1 - \frac{w(t)}{D}))\text{*i(t).....(5)}$$

We are using hybrid CMOS model, as this integration would be beneficial for logical operation. During various computing stages, every individual memristor behaves as an input, an output, and also a logic element. The output is taken at the common node of the memristor. The input are fed separately to individual memristors. Because of the polarity of the memristor, whenever a positive voltage is applied through OR gate, the resistance of the device decreases. For similar inputs theis no voltage drop in the circuit(i.e no current flows in circuit). For different input cases [0,1] or [1,0] based on the applied input voltage, the memristor behaves accordingly. The current flows from higher region to lower region of voltage, thus changes the resistance value of the memristor accordingly.

In CMOS circuit design, for each and every logic function, there are specified number of FET's used based on the logic function to be implemented. In CMOS, the word complementary is used to describe pmos and nmos transistors. Similarly, in memristors we have forward polarized memristor and backword polarised memristor.

$$V = (Roff * Vhigh)/(Ron + Roff) \text{ .....(6)}$$

The initial resistance does not affect the computation in memristive device. This comes into existence only during initial delay. Voltage level also affects the delay.

Until switching process is completed, output produces dynamic hazards. Here the current through logic gate is relatively small, hence requires relatively more time for settling. Power computation is also an issue. Because when similar inputs are applied there is no current in circuit

@IJAERD-2014, All rights Reserved

and hence there is no power consumption. On the other hand, when different inputs are applied, current flow occurs in circuit resulting in power consumption. The power is calculated as:

$$P = V2/Req \ldots\ldots\ldots(7)$$

where $R_{eq} = R_{on} + R_{off}$

We can avoid the signal degradation by using CMOS inverter or buffer which act as level shifter by amplifying signal.

In general during logic implementation of memristor, the LOGIC "1" and LOGIC "0" is distinguished by the ratio $\frac{w(t)}{D}$. When $\frac{w(t)}{D}$ is greater than 0.5 it is considered as LOGIC "1" and if it is less than 0.5, then it is considered as LOGIC "0". Here all the basic logic gates and few sequential circuits are implemented using memristor. This paper describes about the memristor based logic circuits considering the linear ion model and TEAM model.

This following section gives the overview of the memristive circuits implemented for the basic logic gates and its corresponding truth table.

OR GATE

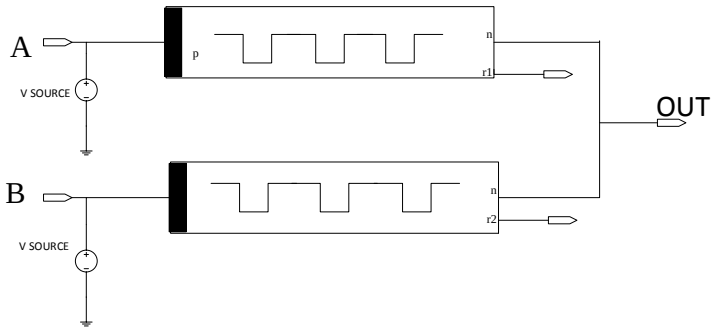


Figure 2:Schematic of Memristor based OR Gate

A	B	OR
0	0	0
0	1	1
1	0	1
1	1	1

The Fig2: shows the schematic of Memristor based OR Gate. Consider two memristors M1 and M2 which are connected in series. When positive voltage is applied to the Memristor M1, the width

@IJAERD-2014, All rights Reserved

of the undoped region increases, as a result the resistance across it falls. At this same time current inside the Memristor increases and we get a larger voltage drop across the output resistor, which indicates it as LOGIC"1".

Case I When A=0 and B=0: As 0V is applied to both the Memristor M1 and M2, we observe that effective resistance of the memristor is exactly 8KΩ(linear ion model) or 16KΩ(for TEAM model)and it is not altering. Here both the input A and B are low the output is also low.

Case II When A=0 and B=1: When 2V is applied to the Memristor M1 and 0V is applied to M2, we observe that effective resistance of the memristor M1 decreases, on the other hand a negative voltage is fed to the memristor M2 which results in increasing of the resistance R as shown in the a Fig. Here the output is high only when the resistance R is greater than 8KΩ(linear ion model) or 16KΩ (for TEAM model) and the effective resistance across the R1 falls below 8KΩ(linear ion model) or 16KΩ (for TEAM model).This principle of determining the change in logic with the change in resistance is employed in all other logic gates. An important point to note, there is delay in output because it is the time taken by memristor to change its resistance state. Similarly, the other two cases are shown in the table in result section of this paper.

NOR GATE

The Fig 3 shows the schematic of Memristor based NOR gate. It is also called as inverted OR gate. The operation of the NOR gate is very similar to the OR gate where an inverter is placed in front of OR gate to function as NOR gate.

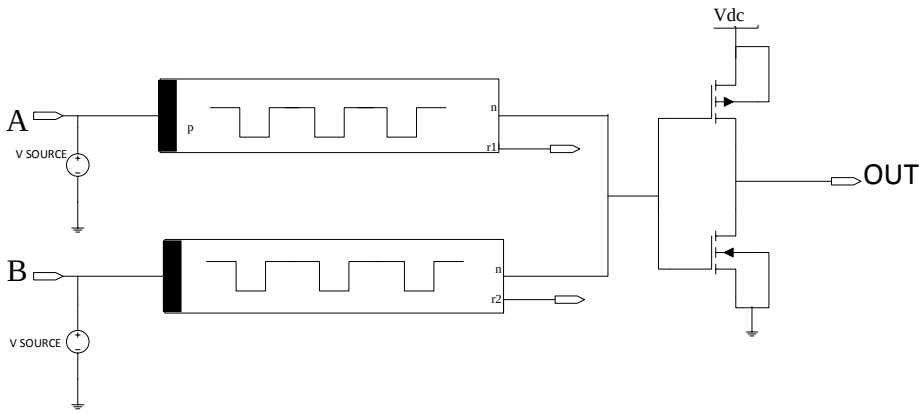


Figure 3. Schematic of memristor based NOR gate

Table 2: Truth table of NOR gate

A	B	NOR
0	0	1
0	1	0
1	0	0

@IJAERD-2014, All rights Reserved

1	1	0

NAND GATE

The Fig4 shows the schematic of Memristor based NANDgate. Here positive voltage supply is given to the negative terminal (n side) of the memristor which leads to shift of doping boundary (w) from D towards "0". This results in making the net resistance of the memristor equivalent to 16KΩ.

Alternatively when a negative voltage supply is applied to the negative terminal of the memristor, it causes the net resistance of the memristor to decrease and it approaches to about 100Ω.The four different combination of input to the two input NAND gate is verified in four cases and graph is in results section of this paper.

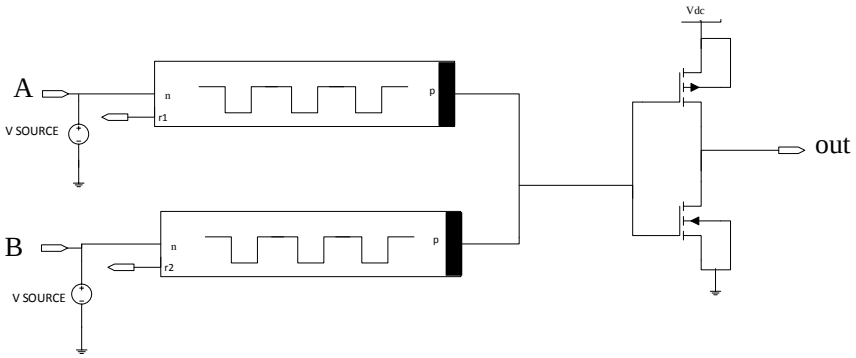


Figure 4: Schematic of Memristor based NAND gate

Table 3: Truth table of NAND gate

A	B	NAND
0	0	1
0	1	1
1	0	1
1	1	0

AND GATE

The operation of AND gate is almost similar to NAND gate except an inverter is placed at its output.Since NAND and NOR are universal gates, AND gate is designed an NAND gate by placing an inverter in front of it. The Fig shows the schematic of Memristor based ANDgate.

@IJAERD-2014, All rights Reserved

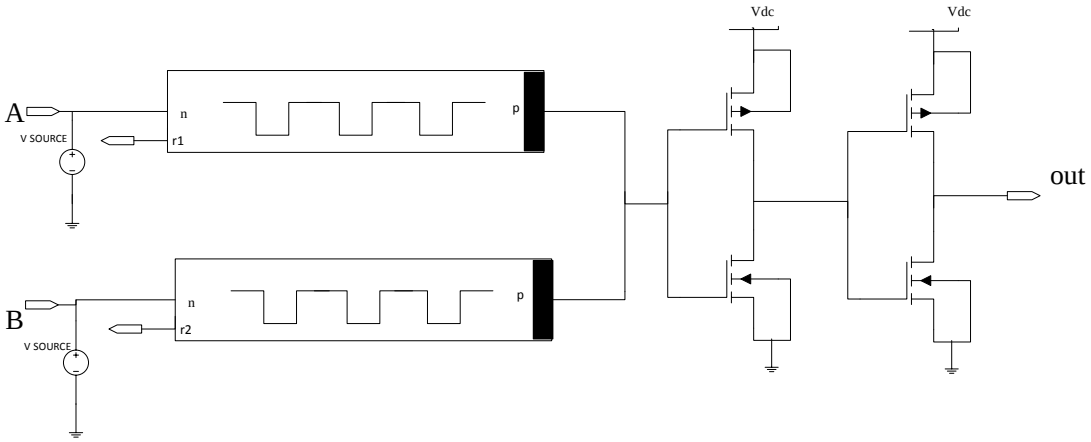


Figure 5: Schematic of Memristor based AND gate

Table4: Truth table of AND gate

A	B	AND
0	0	0
0	1	0
1	0	0
1	1	1

IV. CASE STUDY: IMPLEMENTATION OF FLIP- FLOPS USING MEMRISTOR

Flip- flop or a latch is a circuit which has two stable states and can be used to store state information. The flip-flop is also referred to as a bistable multivibrator. The states of these circuits can be changed by applying signal to one or more control input and will have one or two output. The basic storage element of sequential circuits are flip flops. A sequential circuit (also called finite state machine) is a circuit with memory output depend on both circuit state and current input.

The SR flip flop and D flip flop are analyzed using memristor based logic circuits. The memristive flip flops behave in a similar manner to the usual CMOS flip flops. The advantage of using memristive flip flop is that it consumes less chip area and gives faster result.

SR FLIP FLOP

The simplest type of flip flop is the SET-RESETflip flop. It can be constructed from either two nand gate or two nor gates. Here we have constructed using two memristive based nand gates. Initially assume that q=0, qbar=1 and clock (clk) =1. When both the inputs S and R are "0", it is observed that there is no change in the value of q and qbar. The result section depicts the verificationof these cases. It is called as SET-RESET Flip-flop because the value of q depends on

@IJAERD-2014, All rights Reserved

the input S and R. If the input S is high then q=1,which implies that the Flip-flop is in SET condition.

D FLIP-FLOP

D flip flop captures the value of D input at the definite position of clock as observed in the waveform shown in figure in result section. This captured value becomes the output. At other times, the output does not change.It stores the data present in the D input at every positive edge of clock.

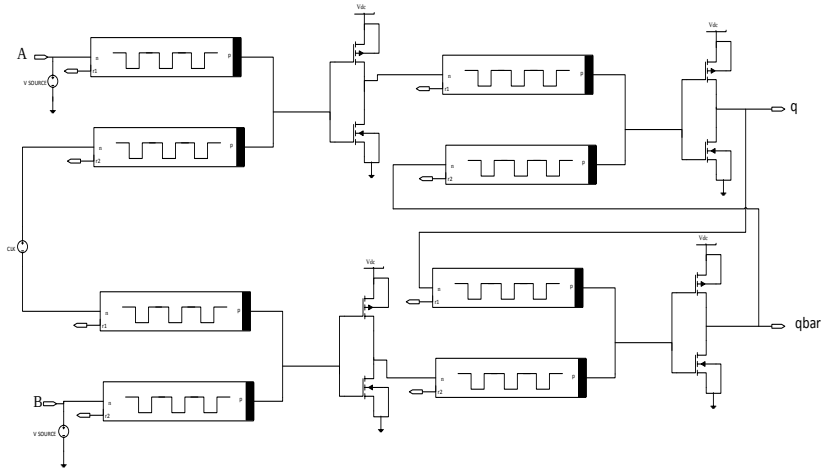


Figure 6: Memristive implementation of SR – Flip Flop

Table 5: Excitation table for SR flip-flop

Clk	S	R	Q	Qbar	
1	0	0	1	1	Hold
1	0	1	1	0	Reset
1	1	0	0	1	Set
1	1	1	0	1	Invalid

D FLIP-FLOP

Table 6:

Clk	D	Q	qbar
1	0	0	1
1	1	1	0

@IJAERD-2014, All rights Reserved

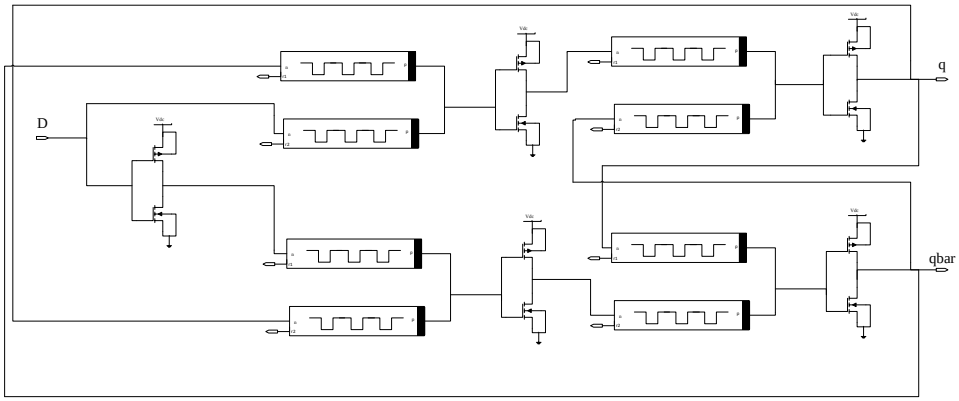
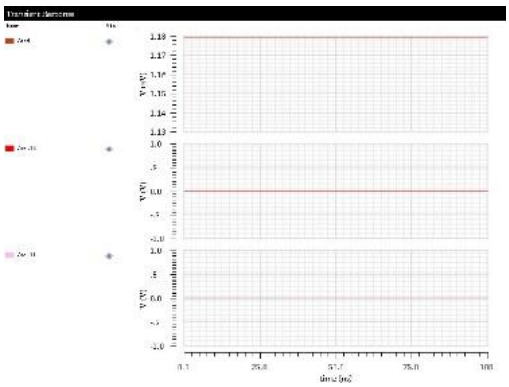
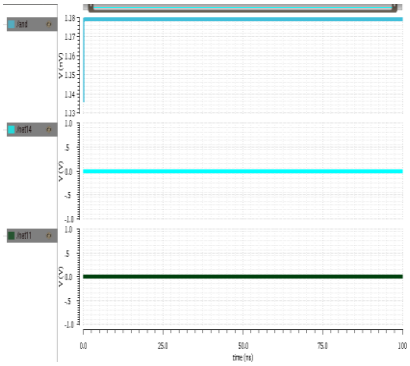


Figure 7: Memristive implementation of D – Flip Flop

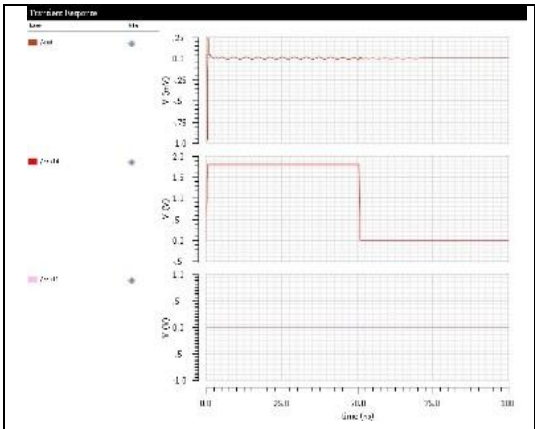
V. RESULTS

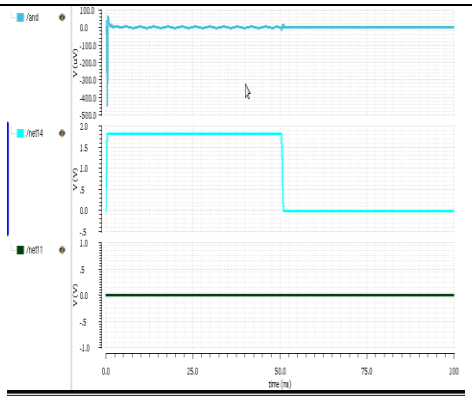
We observe from the following waveforms that the memristor based logic circuits behave in the similar fashion as that of CMOS based logic circuits. The advantage with memristor based circuits is that it consumes less chip area and speeds up the performance. The usage of linear ion drift model leads to more delay when compared with that of TEAM model. Hence TEAM model is suited best.

Therefore all the memristor based basic logic gates are analyzed efficiently and accurately with less delay using TEAM model than that compared to linear ion model.

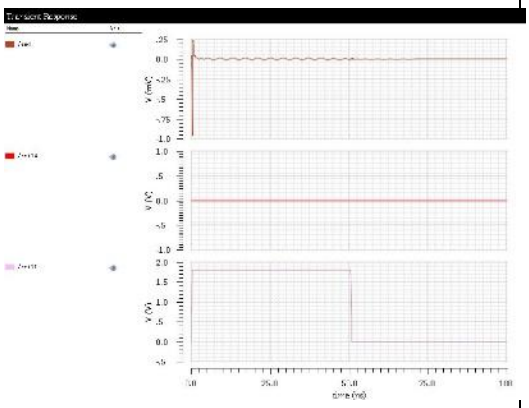
LINEAR ION DRIFT MODEL AND GATE REALIZATION Input case : 00 ; Output : 0	TEAM MODEL AND GATE REALIZATION
	
Input case :01; Output : 0	

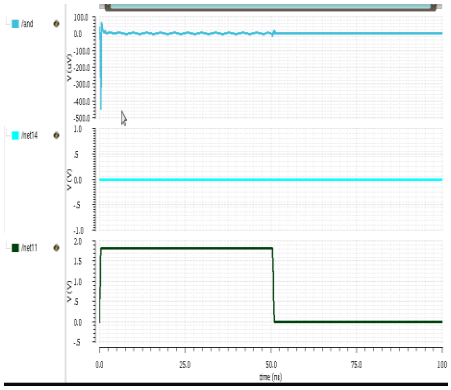
@IJAERD-2014, All rights Reserved



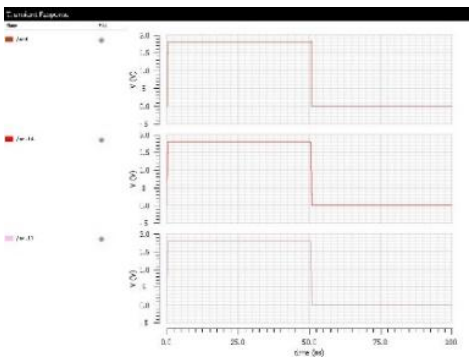


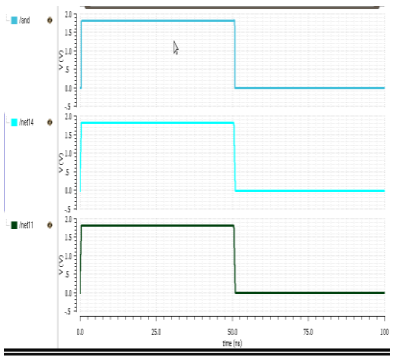
Input case :10; Output : 0





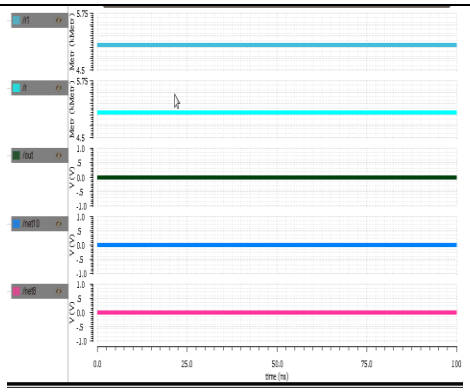
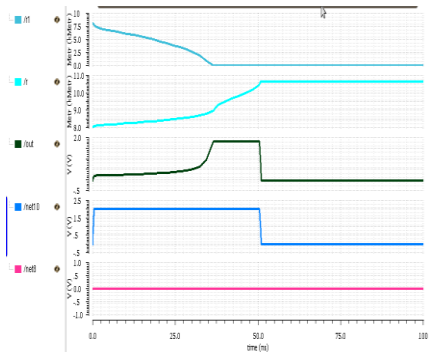
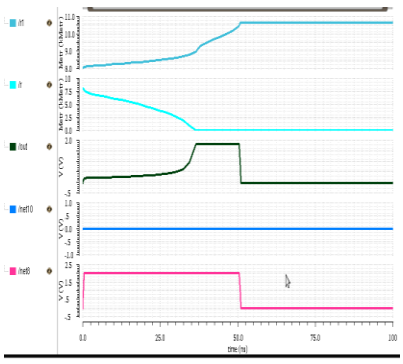
Input case :11; Output : 1



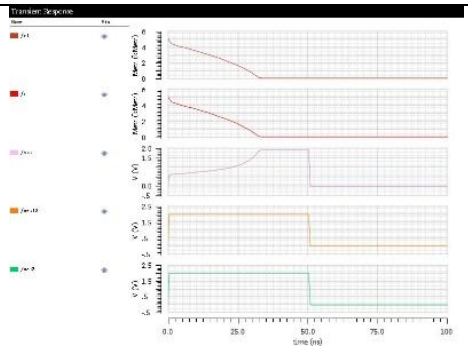


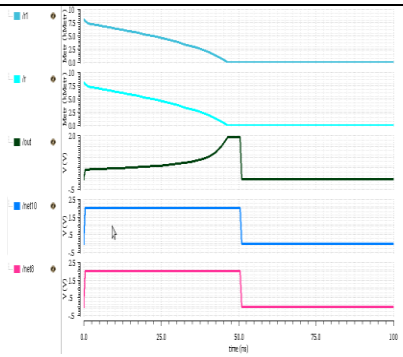
TEAM MODELOR GATE REALIZATION	LINEAR ION DRIFT MODELOR GATE REALIZATION

@IJAERD-2014, All rights Reserved

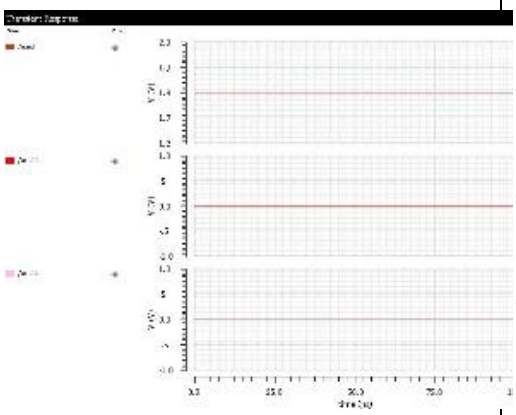
Input case : 00 ; Output : 0	
Input case :01; Output : 1	
Input case :10; Output : 1	
Input case :11; Output : 1	

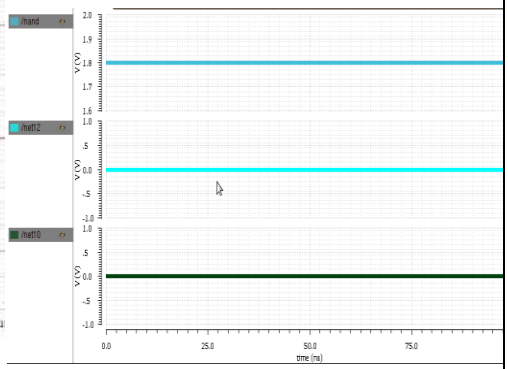
@IJAERD-2014, All rights Reserved

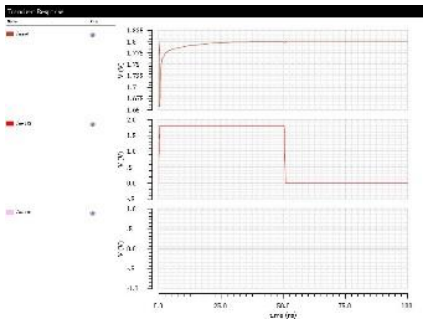


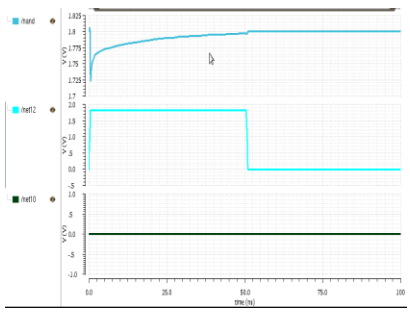


LINEAR ION DRIFT MODELNAND GATE REALIZATION	TEAM MODELNAND GATE REALIZATION
Input case : 00 ; Output : 0	Input case : 00 ; Output : 0
Input case :01; Output : 0	
Input case :10; Output : 0	

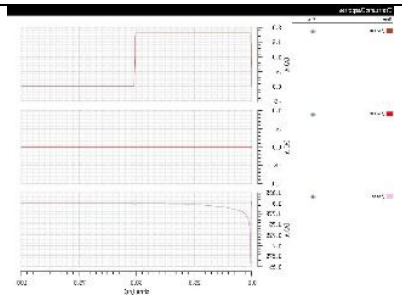
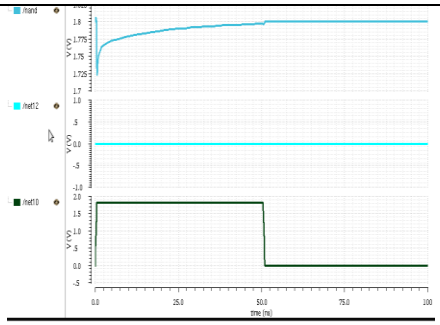
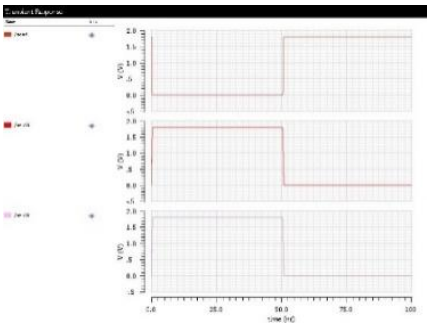
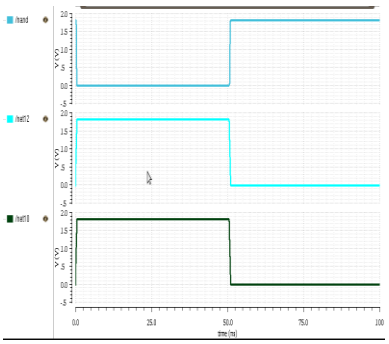


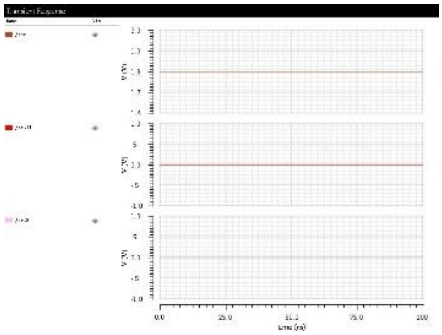
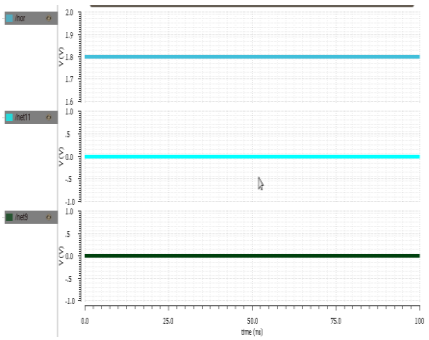




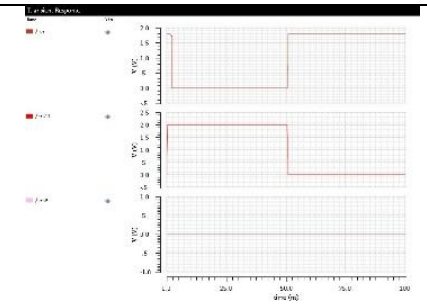


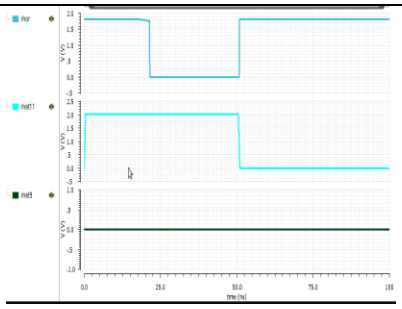
@IJAERD-2014, All rights Reserved

	
Input case :11; Output : 1 	

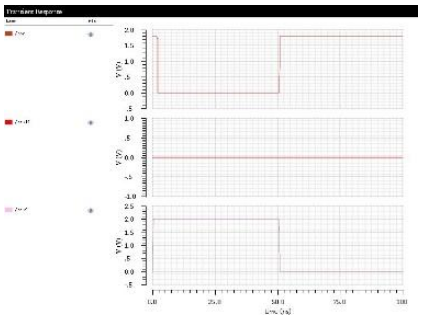
TEAM MODELNOR GATE REALIZATION Input case : 00 ; Output : 0 	LINEAR ION DRIFT MODEL NOR GATE REALIZATION 
Input case :01; Output : 0	

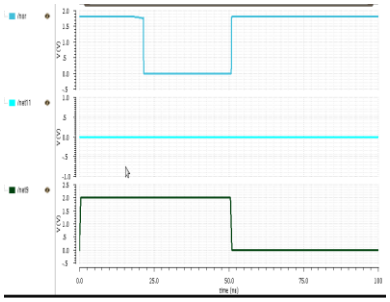
@IJAERD-2014, All rights Reserved



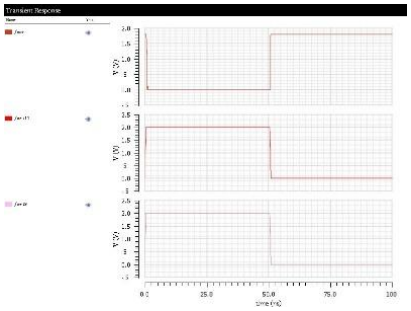


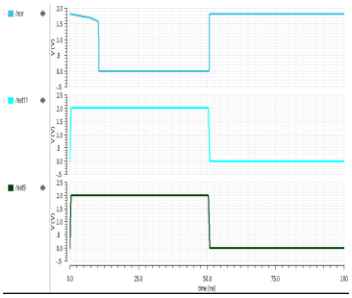
Input case :10; Output : 0





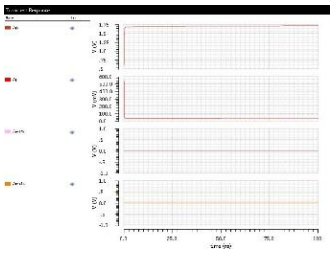
Input case :11; Output : 1





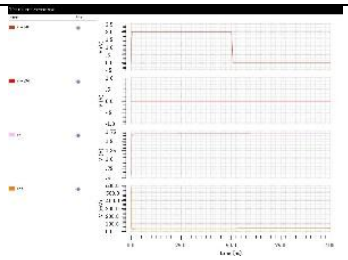
SR FLIP- FLOP REALIZATION

Input : 00 ; Output : 0

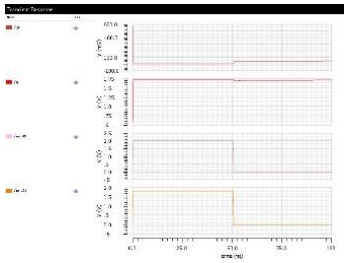


Input : 01 ; Output : 0

@IJAERD-2014, All rights Reserved

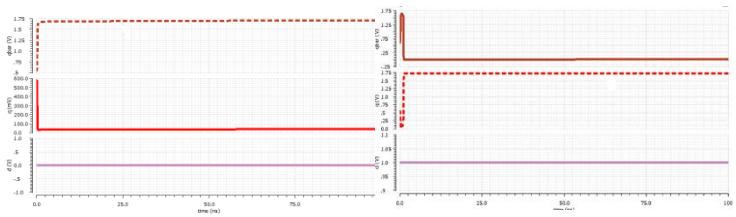


Input : 11 ; Output : 1



D FLIP- FLOP REALIZATION

Input : 0 ; Output : 0 Input 1; Output 1



VI. CONCLUSION

The memristor logic implied here is a hybrid CMOS technology. This logic family uses comparatively less die area than that of CMOS. By using memristor logic NOR and NAND logic gates, the design efforts can be reduced. The memristor logic design circuits are analysed for the two models viz; linear ion drift model and TEAM model. It is found that the TEAM memristor model suits and behaves efficiently for any type circuit when compared with that of linear ion drift model. The case study shows that the memristive model is successfully implemented for flip flops. The table 7 shows the comparison of number of gates used for CMOS and memristor based logic gates.

GATES	CMOS LOGIC GATE	MEMRISTOR LOGIC GATE

@IJAERD-2014, All rights Reserved

AND	6 transistors	2 memristors, 4 transistors
OR	6 transistors	2 memristors, 2 transistors
NAND	4 transistors	2 memristors, 2 transistors
NOR	4 transistors	2 memristors, 2 transistors

Thus by using memristive logic gates, efficient circuits for logic gates can be built which is is non-volatile and consumes less chip area without compromising the performance.

REFERENCES

[1] L. Chua, "Memristor-the missing circuit element", IEEE Trans. Circuit Theory, vol. 18, no. 5, pp. 507_519, Sep. 1971.
[2] D. Struckov, G. Snider, D. Stewart, and R. Williams, "The missing memristor found," Nature, vol. 453, no. 7191, pp. 80_83, 2008.
[3] L. O. Chua, "Device modelling via basic nonlinear circuit elements", IEEE Trans. Circuits Syst., vol. CAS-27, pp. 1014–1044, Nov. 1980.
[4] Taciano Perez, César A. F. De Rose, "Non-Volatile Memory: Emerging Technologies And Their Impacts on Memory Systems" Porto Alegre, September 2010
[5] Shahar Kvatinsky "Memristor ratioed logic" 978-1-4673-0289-0/12/$31.00 ©2012 IEEE
[6] Ioannis Vourkas, Georgios Ch. Sirakoulis "Memristor-based combinational circuits: A design methodology for encoders/decoders " MicroelectronicsJournal45(2014)59–70
[7] S. Kvatinsky, E. G. Friedman, A. Kolodny, and U. C.Weiser, "TEAM: ThrEshold Adaptive Memristor Model," IEEE transactions on circuits and systems—i: regular papers, vol. 60, no. 1, january 2013
[8] "Fourth element : modeling, characteristics and electromagnetic theory of memristor " March 2010 the royal society.
[9] Shahar Kvatinsky, Keren Talisveyberg, Dmitry Fliter,Avinoam Kolodny, and Uri C. Weiser "Models of Memristors for SPICE Simulations" 2012 IEEE 27-th Convention of Electrical and Electronics Engineers in Israel
[10] www.bioimpedence.net
[11] www.memristor.org

@IJAERD-2014, All rights Reserved