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Analysis and Comparison of PD, POD, APOD PWM Techniques For Symmetrical Multilevel Inverter

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ABSTRACT: *A multilevel inverter is a power electronic device made to synthesize a desired AC voltage from several levels of DC voltages. These types of inverters are suitable in high power application due to its lower total harmonic distortion, switching losses and voltage stress on switches than conventional inverter. This paper presents a Symmetrical Multilevel inverter (SMLI) topology with three phase system. In comparison to CHB topology, SMLI topology requires less no. of isolated DC sources. The symmetrical multilevel inverter is simulated for the Phase Disposition, Phase Opposition Disposition and Alternate Phase Opposition Disposition pulse width modulation (PWM) switching control technique with Resistive load. The total harmonic distortion (THD) of the output Phase Voltage are observed for three PWM control techniques. Also comparing this three PWM techniques in terms of THD. The performance of the symmetric MLI is simulated using MATLAB/Simulink.*

Keyword*: SMLI,THD,PD,POD,APOD,PWM*

I. INTRODUCTION

In today era multilevel inverter are emerging as a new breed of power inverter for high application. They synthesize a near sinusoidal voltage (staircase waveform) from several DC sources that approaching a desired waveform[1].A multilevel inverter has been the main focus for most researchers in the power electronic field due to its ability to deal with medium and high power application besides various advantages it offers when comparing it to the conventional two-level inverter operating at the same rating. The multilevel inverter produces less harmonic contents in its output voltage and current. In addition, the power switches in multilevel inverter experience low voltage stress and low electromagnetic interferences (EMI)[2]. The numerous of multilevel topologies and modulation techniques have been introduced and studied in the recent literature. All these topologies have their own combinations and features.

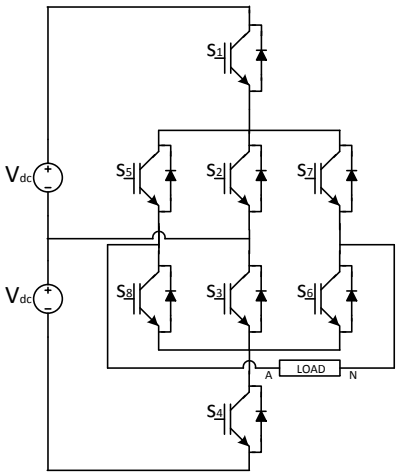
Classifying the multilevel inverter according to the type of voltage synthesis leads to basically three types of inverter namely, 1) Diode Clamped Multilevel Inverter 2) Capacitor Clamped Multilevel Inverter 3) Cascaded Multilevel Inverter with Non Isolated DC Source. Cascade multilevel inverter are further subdivided into hybrid/non-hybrids and symmetrical/asymmetrical type topology. Symmetrical multilevel inverters are inverters with symmetrical DC sources[3],[4],[5],[6].

This paper presents a performance analysis of five level inverter with reduced isolated DC source and PD, POD& APOD PWM control techniques is discussed. The main objective is to improve the inverter topology to achieve high resolution output voltage waveform with less switching losses and improved harmonics spectrum, reduced THD and simple gate driver circuit. SMLI topology are generate nine level line voltage and five level phase voltage. As compared with a H – Bridge Cascaded multilevel inverter, the number of isolated DC source are reduced in the SMLI[6], but, the number of semiconductor device remain the same[7],[8],[9],[10].furthermore by reducing the number of isolated DC sources, the number of cables connecting the input transformer terminals to the rectifying bridges is reduced.

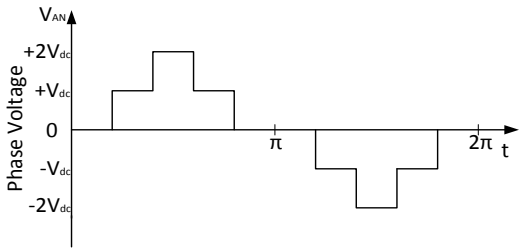
In this paper, a MATLAB/Simulink analysis and compared thefive level output phase voltageTHD between the PD, POD and APOD PWM techniques for symmetrical multilevel inverter. This paper is organized as follows. The derivation of five level switching sequence of symmetrical multilevel and single& three phase SMLI concept is presented in section II. The modulation techniques are explained in sections III. In section IV simulation results and comparison of different modulation are discuss. Finally conclusions are given.

II. SYMMETRICAL MULTILEVEL INVERTER

Single phase SMLI, shown in Figure. 1 (a) which gives five output voltage levels. Switches S5 to S8 are connected as a full bridge inverter that is responsible for switching the load terminals according to the gate signals. Figure. 1(b) shows the possible load voltage Van levels for the specified switching condition. It is seen that the pairs S5 / S8 and S6 / S7 are turned on in complimentary order to generate the negative and positive voltage. The three level inverter switches S1 to S4 are switched according to a proper modulation pattern in order to generate a desired load voltage.



(a) Topology



(b) Output Phase voltage

Figure1. Single Phase Symmetrical Multilevel Inverter

The inverter shown in Figure 1(a) is a five level singe phase inverter where, all switches operate with high frequency. In cascaded H-bridge multilevel inverter output voltage is given by 2N+1 [11] ,[12] similarly, output voltage for SMLI can be obtained by expression 2N + 1 where N is the Number of DC sources[9]

Table I. Switching States And Respective Voltage Levels Per Inverter Leg

V_{AN}	S_1	S_2	S_3	S_4	S_5	S_6	S_7	S_8
$+2V_{dc}$	1	0	0	1	1	1	0	0
$-V_{dc}$	1	0	1	0	1	1	0	0
	0	1	0	1	1	1	0	0
0	0	1	1	0	1	1	0	0
	0	1	1	0	0	0	1	1
$-V_{dc}$	0	1	0	1	0	0	1	1
	0	1	0	1	1	1	0	0
$-2V_{dc}$	1	0	0	1	0	0	1	1

Table 1 is shown to explain how the staircase voltage is synthesized across the load AN. The five-level phase-leg 'a' output with respect to the neutral point 'n', V_{an} can be obtained by following switching combinations.

1. For voltage level $V_{AN} = +2\ V_{dc}$, turn on S_1 , S_4, S_5, S_8
2. For voltage level $V_{AN} = +\ V_{dc}$ there are two combinations , turn on S_1, S_3, S_5, S_6 or S_2, S_4, S_5, S_6
3. For voltage level $V_{AN} = 0$, turn on S_2, S_3, S_6, S_8, or S_2, S_3, S_7, S_8
4. For voltage level $V_{AN} = -\ V_{dc}$ there are two combinations, turn on S_1, S_3, S_7, S_8 or S_2, S_4, S_7, S_8
5. For voltage level $V_{AN} = -\ 2\ V_{dc}$, turn on S_1, S_4, S_7, S_8

For voltage level $+\ V_{dc}$, 0 and $-\ V_{dc}$ the redundancy conditions are available.

Three phase SMLI is formed by connecting the single phase module in a Y – configuration supplying a three phase load through terminals A, B, and C, as shown in Figure 2.

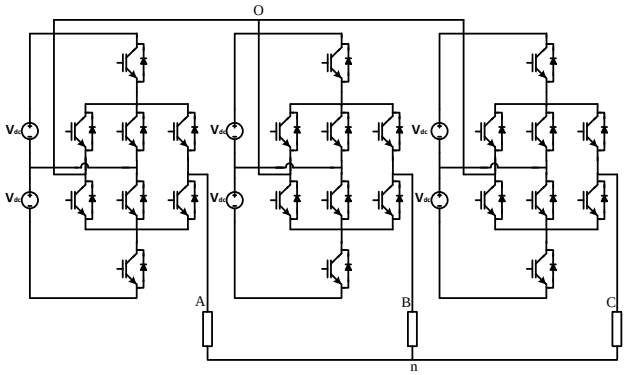


Figure2. Three Phase Symmetrical Multilevel Inverter

The common point of the inverters is called "O", whereas the common point of the load star connected will be named "N". In three phase SMLI the number of isolated DC Source reduces from six to three as compared to the three phase cascaded multilevel inverter. Point O that connects the three inverter legs and serves as a reference for the modulation techniques. Each one of the reference signal is displaced by 120^{O} with respect to each other.

III. MODEL DEVELOPMENT AND CONTROL

The matlab Simulink is used for the simulation of five level symmetrical multilevel inverter. In SMLIIGBTs are used, because of high power handling capability and simple gate drive circuit. The applied voltage is 220 V and load resistance is 20 Ω using the simulation. Inverter output is controlled by using the PWM techniques. In this techniques (n-1) carriers of same frequency f_{cr} and amplitude A_{mc} are used for n level inverter. In this techniques a reference signal of amplitude A_{mr} and frequency f_{mr} is continuously compare with caries signal. Shown in table II parameter used for thesimulation of SMLI.A PWM signal is obtain such that, where the amplitude of the reference signal is higher than the carrier signals than comparing the reference signal and carrier signals it's generates the gate pulse. Figure 3 shown that the one leg control scheme of SMLI. For other two leg carrier signal is remain same but reference signal is 120^{0} phase shifted. In figure 3 Vc1, Vc2, Vc3, and V4 are four carrier signal and VM is a one reference signal. The PWM techniques used for the controlling of inverter are PD, POD and APOD. These techniques are discussed as following.

Table II. Simulink Parameter Values

Sr. No.	Parameter	Symbols	Values
1	Input Voltage	V_{dc}	220V
2	Switching Frequency	F_{cr}	1.6 kHZ
3	Modulation Index	M_i	0.95
4	Frequency Index	M_f	32
5	Load resistance	R_L	20 Ω

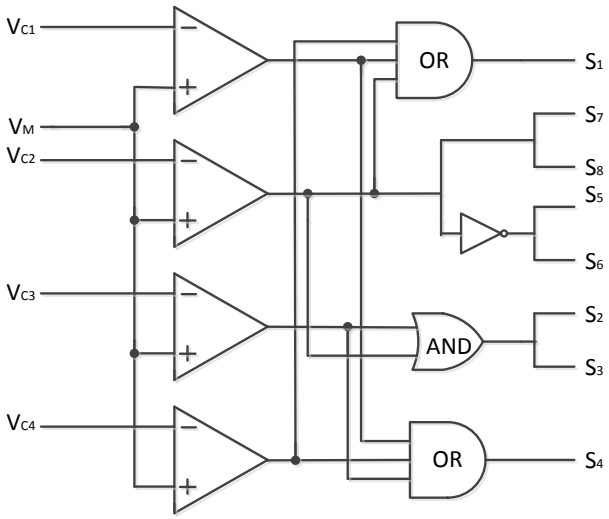


Figure3. Single leg control scheme of SMLI

A. Phase Disposition

In Phase disposition PWM techniques, all the (n-1) carrier for n level inverter are in phase. For five level three phase SMLI there are four carrier and three reference signal. All the four carriers are in phase and all three reference signal 120^0phase shift, shown in Figure 4.

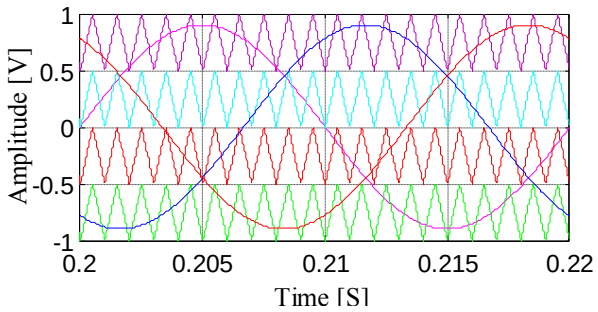


Figure 4.Phase Disposition PWM

B. Phase Opposition Disposition

Phase opposition-disposition techniques is used for n level inverter. In this techniques (n-1) carrier are used in such a way that, carriers above the zero reference are in phase and below the zero reference shifted by180^0
For five level inverter two signal above zero reference are in phase while, the other two are below zero reference with a phase delay of 180^0. These control techniques signals for five level inverter are shown in Figure 5.

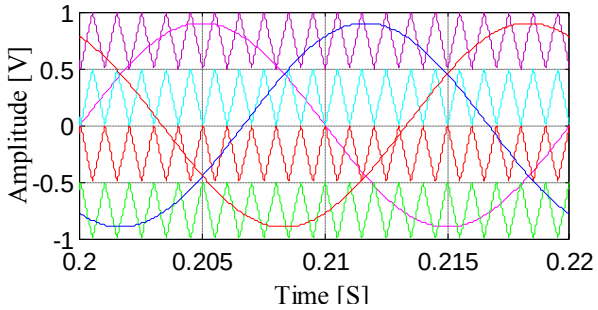


Figure5.Disposition Phase Opposition-PWM

C. Alternate Phase Opposition-Disposition

In this PWM techniques n-1 carrier for n level inverter are out of phase 180^0 alternately. Or five level inverter carrier 1 is out of phase by 180^0 with respect to carrier 2. Carrier 3 is out of phase by 180^0 with respect to carrier 2. Complete phase sequence of five level inverter with 4 carriers and one reference wave form are shown in Figure 6.

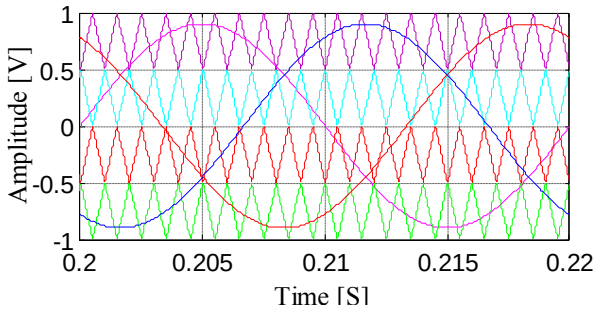


Figure6.Alternate phase opposition disposition PWM

IV. RESULTS AND COMPARISONS

SMLI topology is simulated for five level with output signalfrequency 50 Hz. Simulation parameter are shown in table II. The output voltage of five level acrossload is shown in Figure 7 phase voltage V_{an} and Figure 8 line voltage $V_{ab\ for}$ all three PWM techniques. FastFourier transform (FFT) of the output voltage of the SMLI is analysed by using PO, POD and APOD PWM control techniques as shown in Figure9-11.the FFT analysis of the output voltage by using PDPWM is shown in Figure 9. The magnitude of the fundamental component and THD is lower than the other harmonics .its values is 26.74% & 387 V respectively. The FFT analysis of the output voltage by using PODPWM techniques is shown in Figure10.and it is observed that the harmonic magnitude and THD is comparatively higher the magnitude of fundamental

is 389.7 Vand THD 26.77%.The FFT analysis of APOD PWM is shown in Figure 11.The magnitude of fundamental frequency component and THD is 25.88% & 387.8V at 50 Hz Frequency. Overall analysis conclude in table III. In Table the comparisons of the PO, POD, and APOD techniques in terms of THD and fundamental frequency component.

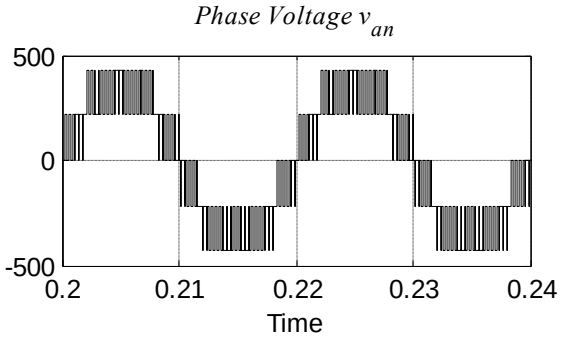


Figure 7. Output voltage across Van for PD,POD AND APOD

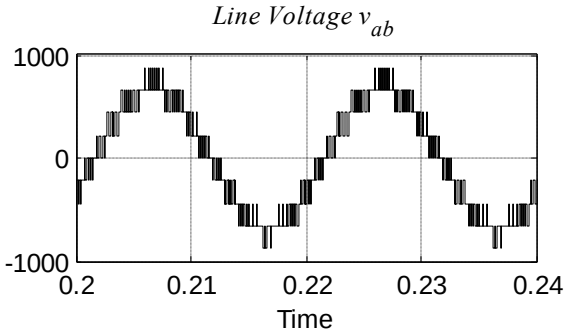


Figure 8. Line Voltage $v_{ab}$for PD,POD AND APOD

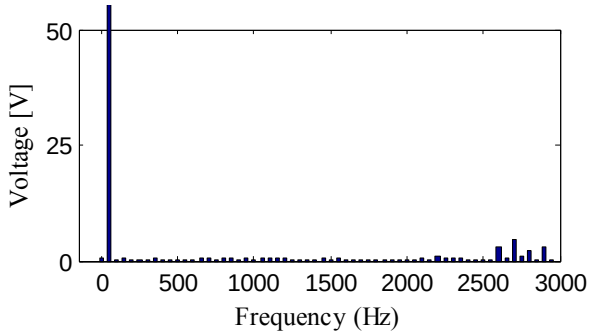


Figure 9. FFT analysis of SMLI by PDPWM

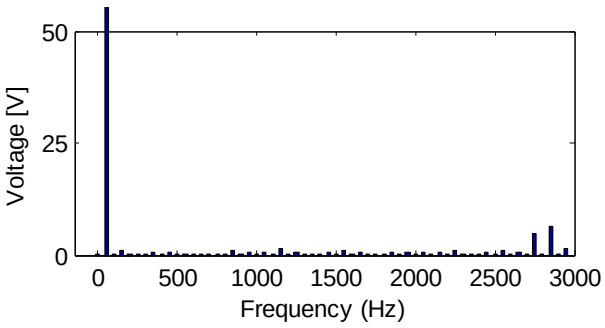


Figure 10. FFT analysis of SMLI by PODPWM

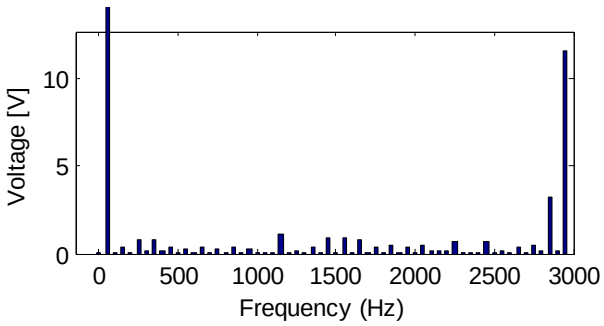


Figure 11. FFT analysis of SMLI by APODPWM

Table III: %THD And Magnitude Of Fundamental Frequency Components

PWM Techniques	%THD	Mag of fundamental(V)
PD	26.74	387
POD	26.77	389.7
APOD	25.88	387.8

V. CONLUSION

The THD analysis of five level SMLI topology using PO, POD, and APOD techniques presented in this paper. Results in terms of THD and Magnitude of fundamental components for all three PWM techniques are compared. It is conclude that the THD of APOD PWM techniques lower as compared to the other two techniques. Symmetricalmultilevel inverter topology reduces the isolated DC source as compared to the cascaded multilevel topology. The future scope of the SMLI can be analysed by using some advance control techniques.

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