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Design and Analysis of Low Power Braun Multiplier using Ladner Fischer Adder

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Abstract — *Multiplier is important in many dsp systems and in many hardware blocks. Multiplier are used in various DSP application like digital filtering, digital communication, this requires parallel array multiplier to achieve high execution speed and to meet the performance. A typical implementation of such an array multiplier is Braun design. Braun multiplier is a type of parallel multiplier, Braun multiplier architecture consist of some carry save adder number of AND gates and Ripple Carry Adder Braun multiplier is proposed with high speed Parallel Prefix Adder instead of using Ripple Carry Adder. This modified Braun multiplier reduced the delay due to the Ripple Carry Adder .The Braun multiplier using Parallel Prefix Adder (PPA) is implemented using Tanner EDA tool.*

Keywords- *Parallel prefix Adder, kogge-stone adder, Ladner Fischer adder, Brent kung adder*

I. INTRODUCTION

The performance of the system is determined by performance of Multiplier. Multiplication is most important among all arithmetic operation. Implementation of vlsi system depends majorly on the multiplication and digital signal processing .In high performance system such as microprocessor multiplier plays a major role. Multipliers consume most of the power in DSP applications. In the low power vlsi design low power multiplier design is necessary.Researchers are trying multiplier which offer high speed ,low power consumption.

An nxn multiplication is conventionally composed of three operational phases: Partial product generation, Carry-free reduction of partial products and Carry propagating addition.The partial product generation is usually a specific time of operation.The minimum delay in the partial product reduction(PPR) and in Additionare both of order of log n.For the fast addition of the partial products fast adders are needed.

The problem occurrence in the speeding up of addition is carry propagation.This gives more interest in the designing of arithmetic circuits. Dsp Application depends not only on the computational capacity also on the power consumption. The area and performance are major consideration but power consumption has more preference than that.The need for low power system in VLSI is due to two reasons. Firstly, with the steady growth of operating frequency and processing capacity per chip, large currents have to be delivered and the heat generated must be removed by proper cooling techniques. Secondly, battery life in portable electronic devices is limited and low power design directly leads to prolonged operation time.

II.EXISTING PARALLEL PREFIX ADDERS

2.1 Parallel Prefix Adder

Parallel prefix adder is most commonly used for binary addition Parallel prefix adder are suited for VLSI implementation. Binary addition is most fundamental and frequently used arithmetic operation the proposed Parallel prefix adder is to optimized**.**The PPA is like a Carry Look Ahead Adder. The production of the carriers the prefix adders can be designed in many different ways based on the different requirements. We use tree structure form to increase the speed of arithmetic operation. Parallel prefix adders are faster adders and these are faster adders and used for high performance arithmetic structures in industries. The parallel prefix addition is done in 3 steps.

1. Pre-processing stage
2. Carry generation network
3. Post processing stage

Pre-processing stage

In this stage we compute, the generate and propagate signals are used to generate carry input of each adder. A and B are inputs. These signals are given by the equation 1&2.

Pi=Ai Bi.....(1)
GI=Ai .Bi.....(2)

Carry generation network

In this stage we compute carries corresponding to each bit. Execution is done in parallel form [4].After the computation of carries in parallel they are divided into smaller pieces. carry operator contain two AND gates , one OR gate. It uses propagate and generate as intermediate signals which are given by the equations 3&4.

P(i:k) =P(i:j) **.** P(j-1:k)…….....(3)
G(i:k) =G(i:j) +(G(j-1:k) **.** P(i:j))……..(4)

Figure3: Carry operator.

The operations involved in this figure are given as.

Post processing stage

This is the final stage to compute the summation of input bits. it is same for all adders and sum bit equation given

Si= Pi Ci……..(5)
Ci+1=(Pi .C0) + Gi……(6)

2.2 Kogge-stone adder

Kogge-Stone adder is one of the parallel prefix form carry look ahead adder. The Kogge-Stone adder was designed by peter M. Kogge and Harold S. Stone .They published in the year 1973. Kogge-Stone prefix adder is the fatest adder design. Its performance plays the major role in the VLSI Implementations. Kogge-Stone adder has large area with minimum fan-out. Among the other parallel prefix adders Koggstone adder is the adder to perform logical addition . Kogge-Stone adder is used for wide adders because of it shows the less delay among other architectures. In the last stage generate bits are produced and the generate bits are XORed with the initial propagate next to the input to generate the sum bits. The 2-bit Kogge- Stone adder is shown below.

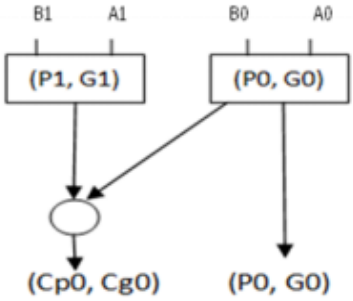

Fig 1. Block Diagram of 2-bit Kogge-stone adder

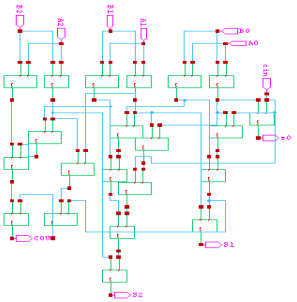

Fig 2. Design of 3-bit Kogge-stone adder

2.3 Brent kung adder

The Brent-Kung adder is a parallel prefix adder. The Brent-Kung adder was designed by Brent and Kung which they published in 1982. Brent-Kung adder may require minimum area and maximum logical depth. A simpler tree structure could be formed, if only the carry at every power of two positions is computed as proposed by Brent and Kung. Intermediate carries are computed by adding inverse carry tree . Its wire complexity is much less than that of a Kogge-Stone adder The number of cells are calculated by using 2(n-1) -Log2n .The 4-bit Brent- Kung adder is shown below.

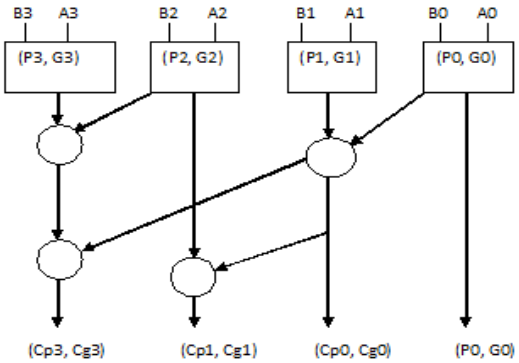

Fig 3. Block Diagram of 4-bit Brent kung adder

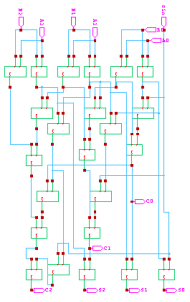

Fig4.Design of 3 bit Brent kung adder

2.4 Ladner Fischer adder

Ladner-Fischer adder is a parallel prefix form carry lookahead adder. A parallel prefix adder can be represented as a parallel prefix graph consisting of carry operator nodes. The time required to generate carry signals in this prefix adder is o(log n). It is a common design for high performance adders in industry. The Ladner-Fischer adder concept was developed by R. Ladner and M. Fischer, which they published in 1980. The better performances of Ladner-Fischer adder are minimum logic depth and bounded fan-out. But it has large area. The 3-bit Ladner-Fischer adder is shown below

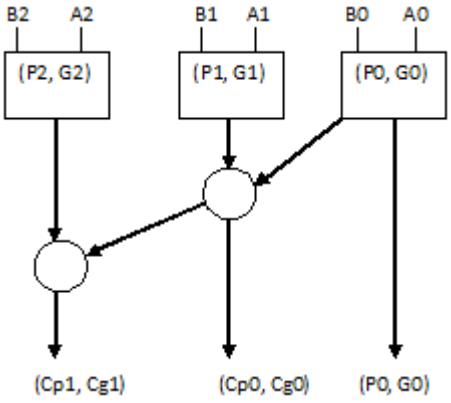

Fig 5. Block Diagram of 3-bit Ladner Fischer adder

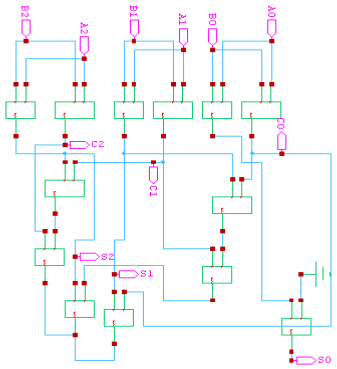

Fig 6. Design of 3-bit Ladner Fischer adder

III.PROPOSED BRAUN MULTIPLIER USING PARALLEL PREFIX ADDERS

3.1 Braun Multiplier

It is parallel multiplier called as carry save array multiplier braun multiplier has cannot be extended to perform signed bits it consist of and gates and adders it is also called as non addictive multiplier it has simple structure comparing to other multiplier each products can be generated simultaneously by means of and gates each partial products can be added with other partial productsby means of adders the carry will be shifted to left or right and then can be added with next sum. The Braun's Multiplier which uses the ripple carry adder block adding the partial product of last stages. In the proposed method we have used the fast addition method i.e. parallel prefix adder so that we are reducing the delay due to carry propagation. The fig. 7 which shows the proposed method of the Braun's multiplier. In the proposed method which consist of the PPA, due to this delay has been very less when compare to the conventional method. In proposed Braun's multiplier, we used PPA in place of ripple carry adder.

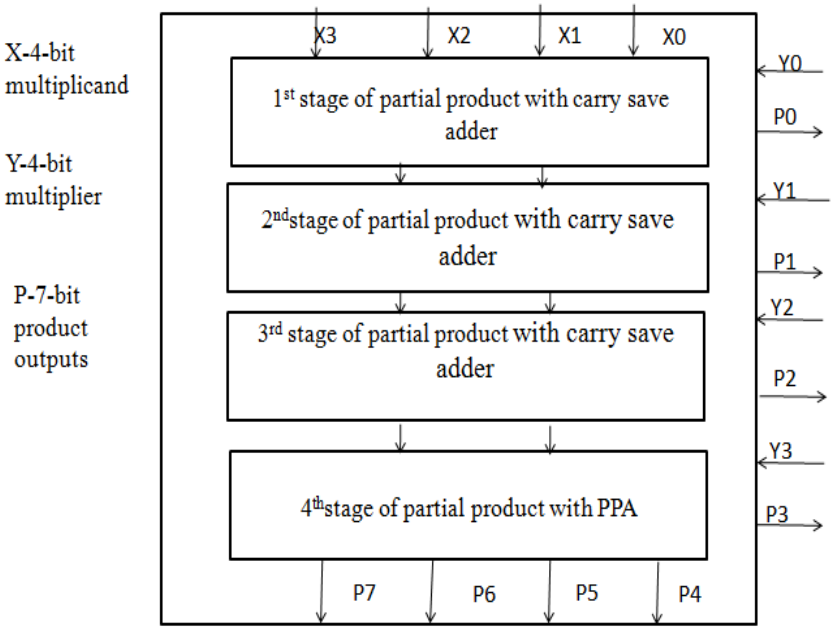

Fig 7.Block Diagram of the Proposed Braun Multiplier

The braun multiplier is successfully implemented using kogge-stone adder, Brent kung adder and Ladner Fischer adder. The implementation of the same is shown in figure 8, 9 & 10 respectively.

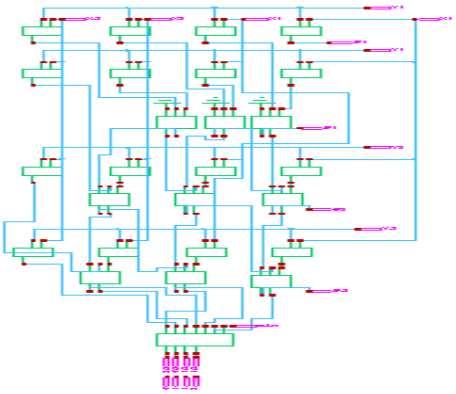

Fig 8.Design of braun multiplier using kogge-stone adder

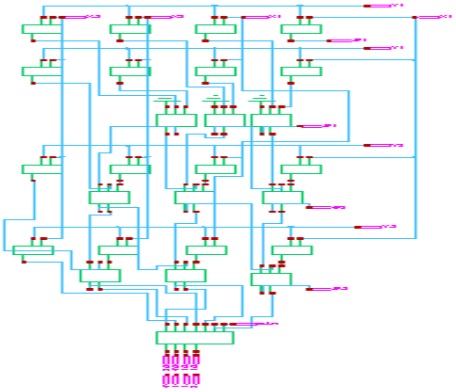

Fig 9.Design of braun multiplier using Brent kung adder

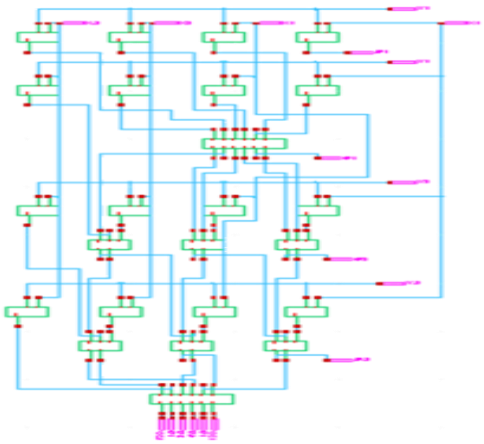

Fig 10.Design of braun multiplier using Ladner Fischer adder

IV.SIMULATION RESULTS & COMPARISON

4.1 Output of Braun multiplier using kogge-stone adder

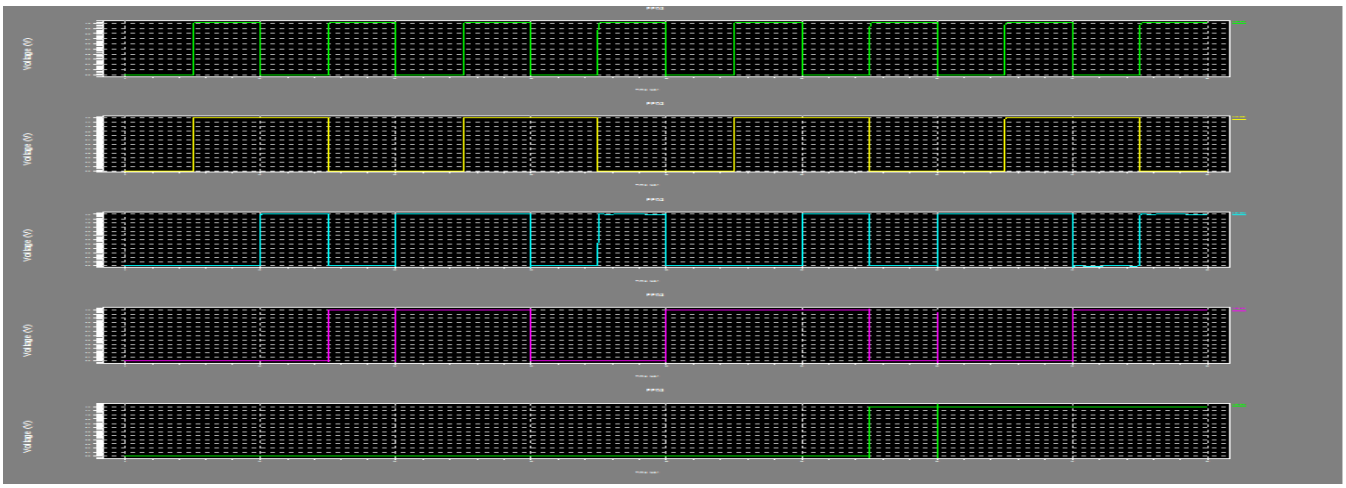

Fig 11. Output of Braun multiplier using kogge-stone adder

4.2 Output of Braun multiplier using Brent Kung adder

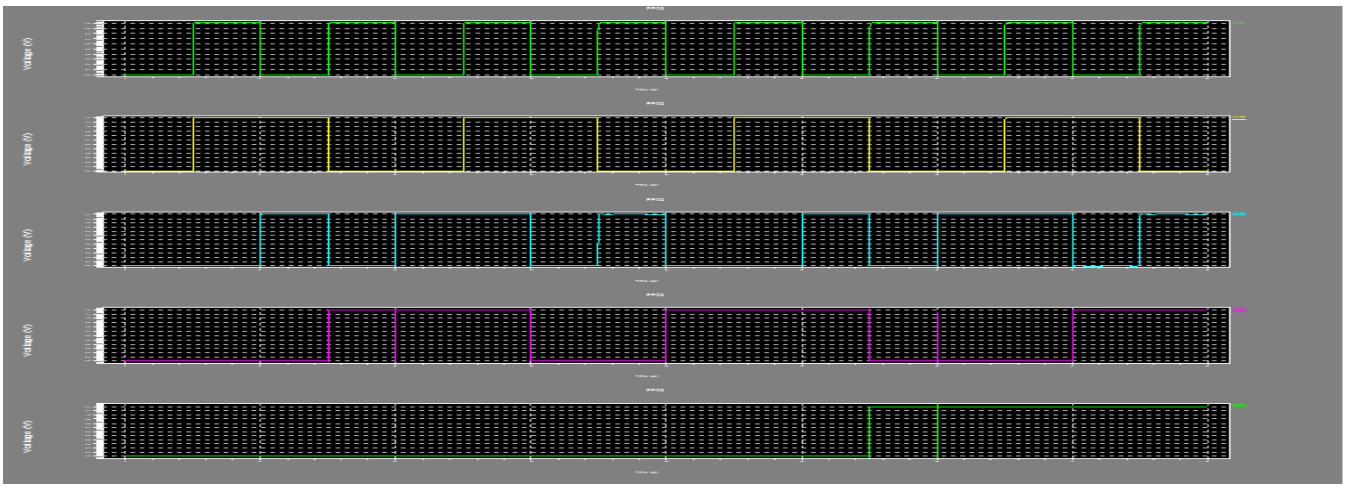

Fig 12. Output of Braun multiplier using Brent Kung adder

4.3 Output of Braun multiplier using Ladner Fischer adder

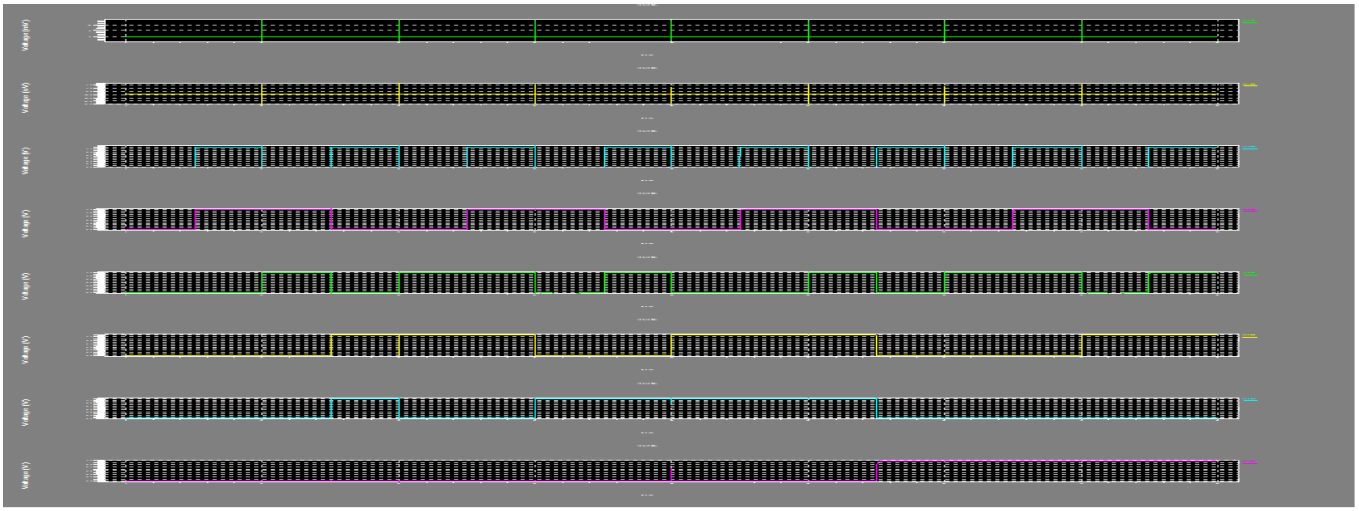

Fig 13. Output of Braun multiplier using Ladner Fischer adder

4.1 **Comparison of braun multiplier in different adders**

Braun Multiplier	Power(mw)	Delay(µs)	PDP(nJ)
Using kogge stone adder	1.07	0.64	0.68
Using Brent kung adder	0.0020	0.52	0.001
UsingLadnerFischer adder	0.0017	0.62	0.002

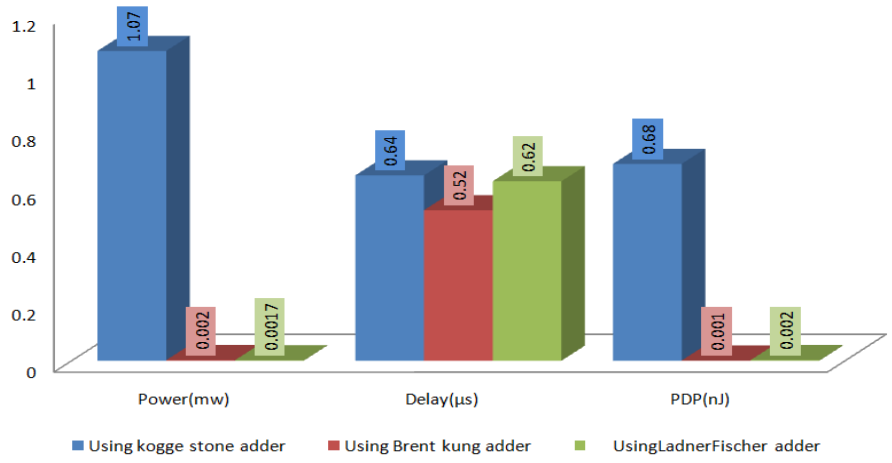

Fig 14.Comparison of Braun multiplier in different adders

V.CONCLUSIONS

From the analysis made above we can conclude that the Braun multiplier using the parallel prefix adder have reduced the delay due the ripple carry adder and also among the above parallel prefix adders braun multiplier using the Ladner Fischer adder consume low power.

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