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Nano crossbar array of Complementary Resistive Switches with nonlinear memristive characteristics

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Abstract—Emerging solid state memory devices based on different materials and volatility has been widely acknowledged like NVRAMs (or Memristor).Evolution of new solid state ionic conductors and in particular (Memristor) brought impetus to the creation of new domain of larger storage capabilities for the future electronic systems. The achievements of these emerging technologies are kind of encouraging when compared with the existing memory types. Accordingly, a new memory architecture called Resistive Random Access Memory (ReRAM) memory faces challenges like sneak path current flowing through neighbouring cells which limits array size. To deal with such issue is to enforce a crossbar array using complementary resistive switch (CRS). CRS has recently been proclaimed as a great beneficiary to conventional charge based memories. But, the nanoscale advantage of these devices poses new challenges in designing such memories as well. In this paper, our purpose is to familiarize Memristor principle and a preliminary note on various understanding of Memristor is also described and a novel non-linear memristive based complementary resistive switch memory model for effective simulation and analysis. The CRS has two memristor connected in anti-serially. Four different state of CRS which significantly reduces sneak path current as compared to memristor based architecture. Here, CRSs can be viewed as primary logic building block in array and two modes of resistance states of CRS stores the information. Thus, our aim is to elucidate as to how CRS is beneficial for reducing sneak path current.

Keywords- Electroforming, Memristor, Complementary resistive switch (CRS), RRAM, Solid State memories, non-volatile memory.

I. INTRODUCTION

The current requirement for high speed, low power random access memory with tremendous packing density has drawn much more interest to build nano-scale solid-state memory devices encountering the timely demands. As reported by ITRS (International Technology Roadmap for Semiconductors) 2013[1], contemporary memory devices endure from uprising static power owing to the leakage current and power consumption which totally depends upon the static power. In order to reduce this power consequence, coming forth non-volatile memories (NVM) based on resistive state changes are under persuasive research. The limitations of conventional CMOS based memories can be overcome by resistive switching based memory namely ReRAM (employing Memristors) which is claimed by Leon Chua [2]. ReRAM primarily arise from 'resistive' switching instead of 'capacitive' (which is in CMOS memory devices), storage of information is done according to the value of variable resistance of the switching material. This led to birth of a new type of solid state memories employing memristors. TiO_2 is one of the latent materials used as insulator for devising ReRAM, owing to its high dielectric constant and wide band gap with adaptability of both unipolar and bipolar switching. In this paper, we attempted to encompass the voyage of TiO_2 based RRAM crossbar structure, towards the improvising the reliability aspects of the device performance in a comprehensive manner.To evoke the advantage of resistive switching, several memristor array architectures have

been proposed and designed like a passive crossbar arrays with Memristor as memory device forming a possible non-volatile random access memories (nvRAMs) [3]. However, this memristor crossbar arrays have the issue with sneak-path currents because of interference from the neighbouring cells within the array while selecting a particular cell. To avoid this sneak-path current, complementary resistive switches (CRS) were proposed [4] which act as combined memory device and storing element as well. Such combination introduces distinct Memristor states that can diminish the sneak-path current effectively [5].

The paper is devised asin section 2, basic principles behind Memristors and CRS i.e. electroforming. In Section 3, detailed understanding of Memristor. In section 4 understanding about CRS. In section 4 we describe the crossbar array architecture. In section 5 of this paper deals with CRS, its crossbar architecture and comparison with Memristor architecture. In final Section 6 describes about the concluding notes of this study.

II. ELECTROFORMING

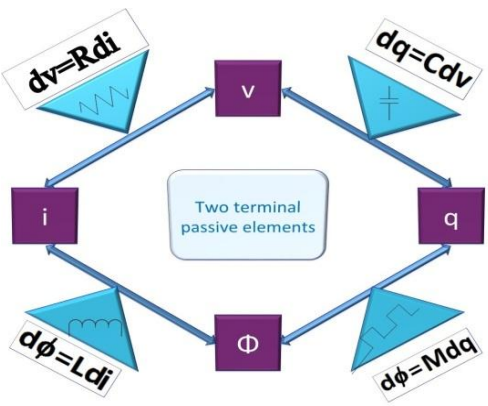
The basic fundamental behind the operation of a Memristor and/or CRS is the electroforming. The origin of resistive switching (RS) phenomenon, originated by forming a conduction path between two electrodes i.e. upper and lower electrodes under the strong impact of a high electric field across the electrodes, is known as electroforming [6]. Electroforming is responsible for the function of the Metal–Insulator–Metal junction. This electroforming procedure demonstrates itself as the change in electrical conductivity due to oxygen ion migration, resulting in the resistive switching phenomenon. Applying particular voltage to the device for the electroforming, oxygen vacancies are created inside the gap between two electrodes and drift it subsequently towards another end, forming a conducting channel between top and bottom electrode. Depends on the oxygen vacancy in the region, the region is discriminated as conductive or resistive [6]. More number of oxygen ions defines low resistance state (LRS) the so-called region of high ionic conductivity and the resistivity which contains less oxygen ions defines high resistance state (HRS). Logic values are given as “1” and “0” to LRS & HRS respectively. It is observed that the electroforming process totally depends on bias polarity (voltage polarity) and dielectric property of the material, thickness of the device and the presence of oxygen ions.

III. MEMRISTOR

A Memristor is a fourth passive two-terminal circuit element invented by Leon Chua in 1971[2] and the other three elements being the resistor, the capacitor and the inductor shown in fig. 1(a). In 2008, researchers from Hewlett Packard (HP) Labs maintained that the Memristor was recognized physically through two-terminal titanium-di-oxide (TiO_2) nanoscale device [3]. The Memristor exhibits nonlinear input-output characteristics i.e. the main difference between other passive elements and Memristor. Memristor is a fundamental element to make a ReRAM memory cell [3]. Memristor has nonlinear relationship between flux and charge i.e. time integral of current and

$$M(q) = d\phi / dq$$

voltage. Memristor is also called memory resistor. A charge controlled memory resistor referred to as memristance (*M*).



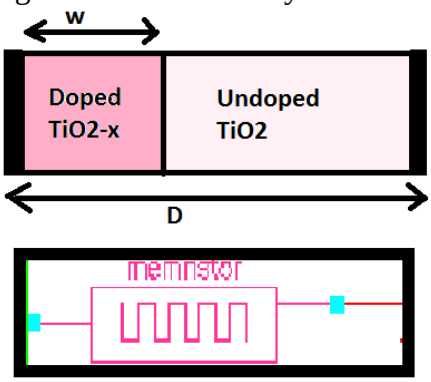


Figure.1 Relation among passive elementsFigure.2 Internal structure of Memristor &circuit Symbol

Memristor is composed of three electrode, top and bottom electrode is of metal like platinum and middle electrode which is very thin film consists switching material like TiO_2 referring here see in figure 2. Thin film consist two layer one is undoped region (pure TiO_2) which is highly resistive and other doped region (TiO_{2-x}) with oxygen vacancies which is highly conductive. In which, *w* represents width of doped region called internal state variable of memristor. Low resistance state called $R_{on,}$ signifies doped region can be expressed as 1 and high resistance state called R_{off}, signifies as undoped region can be expressed as 0. To store Boolean data R_{on} and R_{off} are necessary in Memristor. Both R_{on} and R_{off} performs important role to behave as Memristor. As the positive potential is applied across the Memristor, the oxygen ions (charge) repel into undoped region and *w* can be elongate only up to *D* i.e. Low Resistance State and as negative potential applied, oxygen ions will be attracted or pull in from undoped region and *w* may be vanished at some point i.e. the so-called high resistance state namely R_{off}. The Memristor has memory impact as long as it maintains its resistivity, even if the potential is not applied. In pursuance of the remark device features [1-2,7], oxygen vacancies will become absolutely immobile until the voltage is applied again. I.e. it stores current state when power is off. This means that it stores charges depicting a memory device. The mathematical model for a Memristor as a function of window function (w),

$$R(w) = (R_{on} \times w/D + R_{off} \times (1 - w/D))$$

Physically, the *w* is limited within $0 \le w \le D$. Polarity of the device matters meaning that increase or decrease of charge depends totally on applied positive or negative voltage. Hysteresis loop of a Memristor is shown in fig.3.

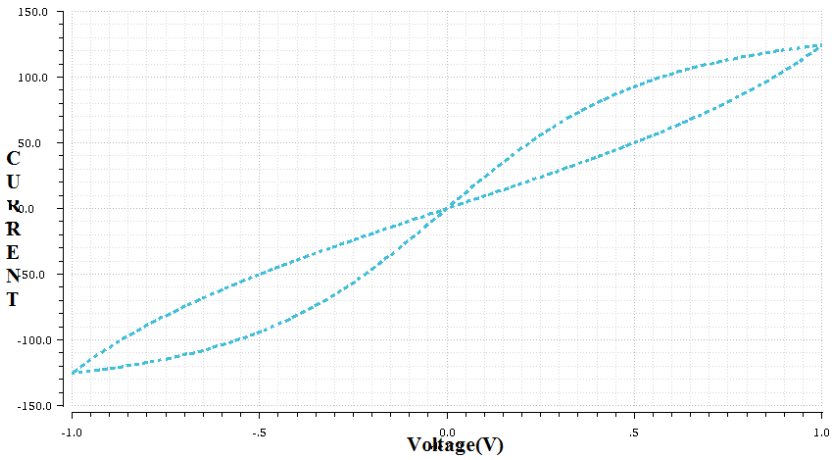


Figure 3. Pinched hysteresis loop of Memristor [present work]

IV. COMPLEMENTARY RESISTIVE SWITCH

According to Rosezin et al, CRS is very much flexible in crossbar array architecture. CRS is simply a series combination of two Memristors [8]. It represents High Resistance State (HRS) andLow Resistance State (LRS) in combining to denote logic state 0 and 1 respectively because they are connected anti-serially due to which overall resistance state is always high that gives reduction in leakage current flowing through unselected cells. If Memristor device A and Memristor device B are present then four different states can be inspected which is shown in following Table 1.

Table 1. States of CRS

State	Device A	Device B	Total Resistance
'0'	HRS	LRS	~HRS
'1'	LRS	HRS	~HRS
'ON'	LRS	LRS	LRS+LRS

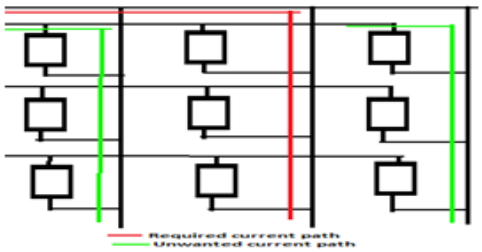
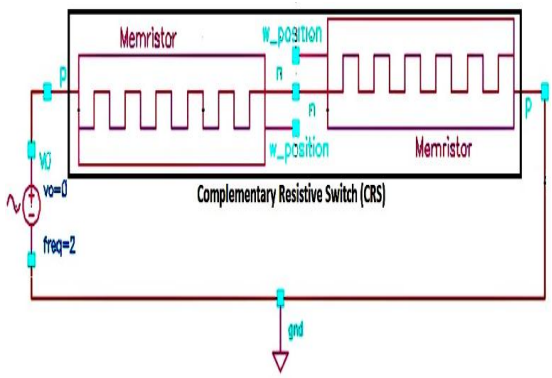


Figure 4.Crossbar structure using Memristor and current flow

If LRS(L) is written in Memristor A and HRS(H) in Memristor B. Combinations H/L and L/H for A and B represent logic "0" and logic "1" respectively. Combinations H/L and L/H shows that either one is in conductive or resistive. In H/H state both Memristor are in resistive state. The H/H state only happens one time i.e. in starting of device and for rest it is off state only. L/L represents always ON state. This state shows that both devices are in conductive state [9]. In crossbar structure with CRS as device current from unselected path is less because of its HRS state due to which sneak current automatically gets reduced.

Moreover, appropriate study of CRS can be done in pulse mode which is required to check the feasibility for real operations on memory and logic applications. We analyzed the CRS characteristics for how exactly it behaves. In Figure 6, the characteristic of non-linear memristive based complementary resistive switch is shown. CRS does the voltage division like for particular voltage it assigns in the ON state (L/L), and then according to voltage it switches to HRS/LRS to LRS/HRS state. We analysed the CRS I-V characteristics using the given Verilog-A approach [10-11].We have chosen specification as per published literatures [10-11].The I-V characteristics are determined by simulations using in Cadence Virtuoso applying a sinusoid potential to the CRS device. In Figure 5, circuit diagram for analyzing the characteristic is shown and in Figure 6 the typical current response to applied voltage sweep is portrayed.



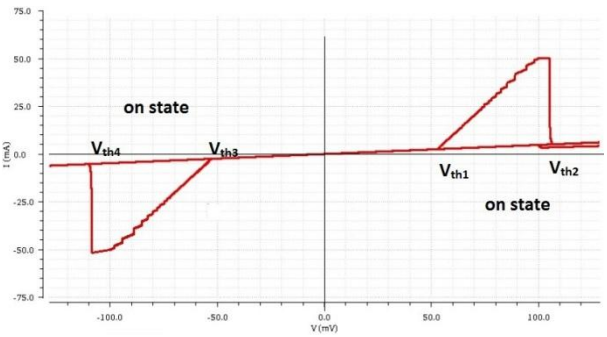


Figure 5. Circuit diagram for analyse the characteristics.Figure 6. I-V characteristics of CRS with R_{off}/R_{on}20:1 ratiowith off20MΩ

If memristor device A is in LRS and memristor device B in the HRS then all voltage drops over memristive device B until it reached to V_{th1}. At this voltage device B shifted to the LRS and device A still in the LRS. The reason being the voltage drop at A is very below than reset voltage. Then the state of CRS is defined as `ON' state, with both memristior devices are in low resistive state and with an equal potential drop. When voltage reaches to threshold $V_{th2}$ memristor device A shifts to HRS, because voltage drop almost equal to reset voltage and defined as `0' state. For voltage greater than V_{th3}, the memristor device A still in high resistive state and device B shifts to low resistive state. When voltage comes under the range $V_{th4} < V < V_{th3}$ the HRS of device A shifts to the LRS and then both memristor devices are in the low resistance state which defines `ON' state. As negative voltage passes V_{th4}, then device B shits again to the HRS state and equivalent state is "1" [12] as shown in Figure 6. It is observed that in order for the CRS operation in crossbar architecture, there is no need of giving any connection to the middle electrode.

V. NANO CROSSBAR ARRAY

Memristor has given the new opportunity to build a high density memory which is enhanced in crossbar architecture. Crossbar architectures were basically developed to overcome the limitation on density of any memory and give you high data storage capacity. In cross-bar array architecture, word-lines and bit-lines are perpendicular to each other, and memory devices are imposed between intersections of word-lines and bit-lines". In this array architecture we connected resistive switching device as Memristor. A load can be connected at the end of bit-lines for the read operation. The state of the memory device is determined by the electric current through devices.

In crossbar architectures employing Memristors as memory device, leakage current occurs due to read disturbance in arrays, called sneak current. This sneak current flows through unselected neighbouring cells because of memristive states. Due to this leakage current it limits the proper utilization of the crossbar array. To resolve the problem of sneak path current, Linn et al. [4] proposed an approach employing memristor as basic element by connecting two Memristors in series with opposite polarity i.e. anti-serially [8].

VI. SNEAK PATH CURRENT ANALYSIS

To overcome the issue of sneak path current, we worked on crossbar array architecture with complementary resistive switches, as also shown in [6]. Our CRS model uses the memristor model as per [10-11]. To find out how the effective our CRS model, many number of experiments are took out for depicting the sneak current path for a crossbar architecture. Crossbar structure we design with combination of 2x2 and 4x4 array.

To read/write onto particular CRS device, we used 2:4 decoders for 4x4 crossbar structure as shown in figure 8. According to decoder logic it will select that particular device for storing the information for e.g. input 00 of decoder will select first row of array, for 01 combination it will select second row likewise for all four separate selection lines are provided for all rows. To measures the currents we need to apply voltage for that particular selected row & need to measure the current in the selected column of that particular device. For simulation in Cadence Virtuoso we used values of OFF resistance (R_{off}) of 20MΩ and ON resistance (R_{on}) of 100KΩ. The crossbar structure with 2x2 and 4x4 array shown in figure 7 &8.The resultant currents are measured & calculated and compared with crossbar array of Memristor with different read currents i.e. when device is in OFF state and device is in ON state. The sneak current is calculated with current through unselected cell.

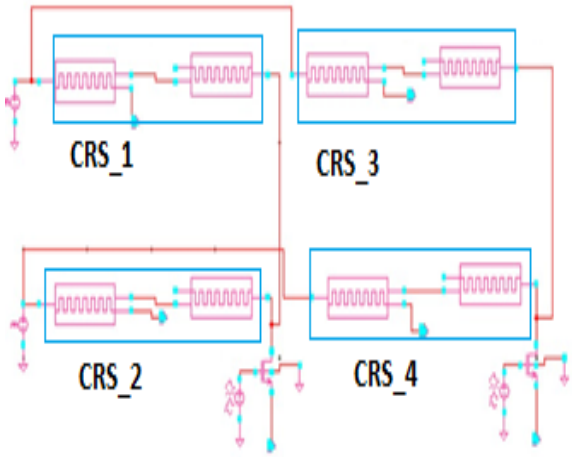


Figure 7. 2x2 array.

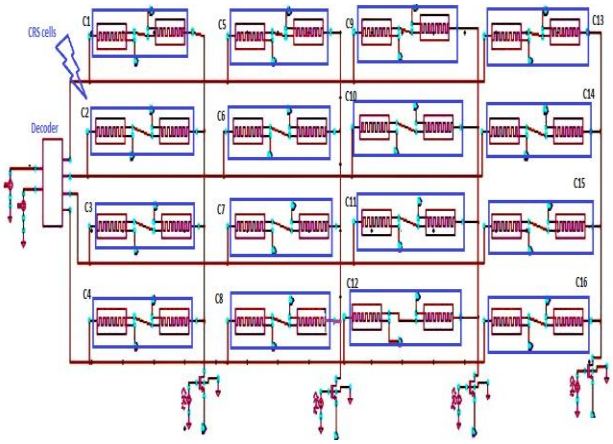


Figure 8. 4x4 array with CRS devices

In Figure 9 it shows the selection of the CRS devices in 4x4 array according decoder inputs and current flowing through CRS device. This current waveform shows very less leakage current as compare to Memristor based array. CRS device gives proper response to applied potential moreover current through unselected devices are very less which means sneak path current can reduced using CRS.

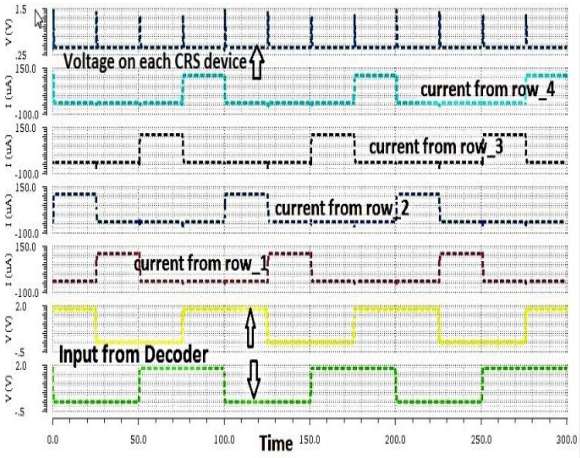


Figure 9. Current flowing through CRS devices

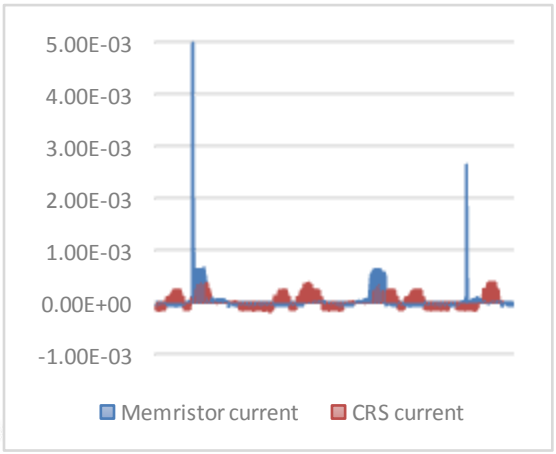


Figure 10. Sneak Current Comparison between Memristor & CRS

Figure 10.shows the comparison of current values with memristor and CRS as device in crossbar architecture. We observed that as the size of increases, sneak current in memristor based crossbar architecture increases gradually. But, as in the case with CRS model based crossbar architecture, the sneak current is significantly lower, and moreover it is approximately remains same for different

architecture sizes. One thing we observed that, to measure the read current, it is depends on state of the device in memristor based array and as in CRS based array it is independent of content of the state. We compared the calculations obtained from paper [13]. We have obtained the perfect difference in comparison between memristor and CRS as demonstrated

VII. CONCLUSION

A complementary resistive switch (CRS) based on Verilog-A is modeled. Comprehensive simulations and various analyses have been conducted using Cadence virtuoso tools to demonstrate the how effective CRS over memristor is in crossbar architecture. Our model showed the explicit non-linear characteristics with applied potential. We proved that due to CRS construction, sneak path current can be reduced over memristor array.

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