Scientific Journal of Impact Factor (SJIF): 5.71
e-ISSN (O): 2348-4470
p-ISSN (P): 2348-6406

International Journal of Advance Engineering and Research Development

Volume 5, Issue 03, March -2018

Comparison of Wallace, Vedic and Dadda Multipliers

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ABSTRACT: *There are various multiplication methods that are known. of the many, three structural multipliers, Wallace, Vedic and Dadda are compared in this paper. For comparison, the three multipliers are simulated in cadence. Simulated results of the multipliers are attached. Later comparison is done among the multipliers based on the delay, area and power requirements.*

KEYWORDS : *Multipliers, Wallace, Dadda,Vedic , Vertical Crosswise, Xilinx, LUTs, delay.*

I INTRODUCTION: Multiplication is the most critical operation in every computational system. Multiplication can be well thought-out as a series of repeated additions. Since, in today's world, speed is a major factor hence multiplication must be performed faster as multiplication is the base of any signal processing device. The three structural multipliers that are compared are: 1. Wallace Multiplier. 2. Vedic Multiplier 3. Dadda Multiplier.

II WALLACE MULTIPLIER Wallace multiplier is a multiplier which multiplies two numbers in a structural format. It was devised by Australian Computer Scientist Chris Wallace in 1964. Wallace introduced parallel multiplier architecture. The Wallace tree has three steps:

1. Partial Product Generation
2. . Partial Product Reduction
3. Partial Product Addition

In the first stage, as per normal multiplication process, partial products are generated. More the number of partial products more will be the height of the set of partial products generated. In the second stage, this height is reduced by placing half adders or full adders to a height of two. Here adders are placed wherever possible. Once the height of the partial products is reduced to two, then addition is performed between them to yield the final result.

In Wallace multiplier, adders are used height wise or in other words column wise. In order to proceed to next step, first the unused bits are written column wise and then the sum of the adder of that stage followed by the carry of the previous stage.

Step 1: Generation of Partial Products.

Step 2: Reduction of Partial Products generated. In this step, the height of the partial products is reduced step by step till it reaches to the height of two. The height of the intermediate steps is such that uniformity is maintained with respect to the previous stage or intermediate matrix. For reducing heights adders are used. So the reduced intermediate matrix is given below which has the height of six. Notice that vacant or unused bits are placed first followed by the sum of the adder followed by the carry of the previous step. Here calculation starts from the LSB side.

Step 3: Addition of partial products. Then the matrix of height two is added by any known adder like carry select adder or parallel adder etc. The final sum which will be the result of the multiplication

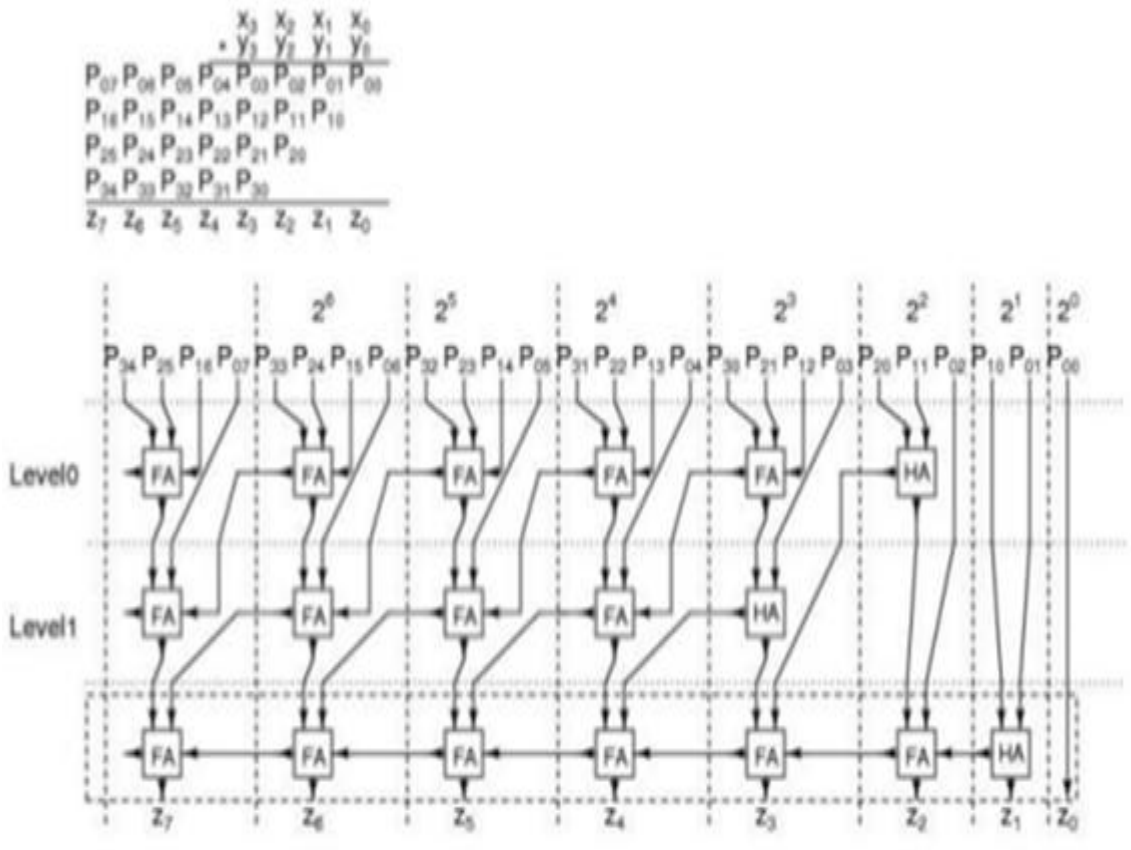

Figure 1.Wallace tree multiplier

III VEDIC MULTIPLIER

The structure of Vedic Multiplier is a Vertical Crosswise. It generates all partial products and their sum in one step. Since the partial products and their sum are calculated in Parallel. The Vedic Multiplier is one of the fastest multiplier. The Vedic Multiplier works under Algorithmic basis.

Algorithm

- Divided the Multiplicand A and Multiplicand B into two equal parts, each consisting of [N to (N/2) 1] bits and [N/2 to 1] bits respectively, where first bit parts indicates the MSB and other represents LSB.
- Represents the parts of A as Am and Al and parts of B as Bm and Bl. Now represents A and B as Am,Al and Bm,Bl respectively.
- These inputs are multiplied with Vertical and Crosswise basis,
- Am x Bm, Am x Bl, Al x Bl Al x Bm
- The individual multiplication products can be obtained by the partitioning method and applying the basic building blocks.

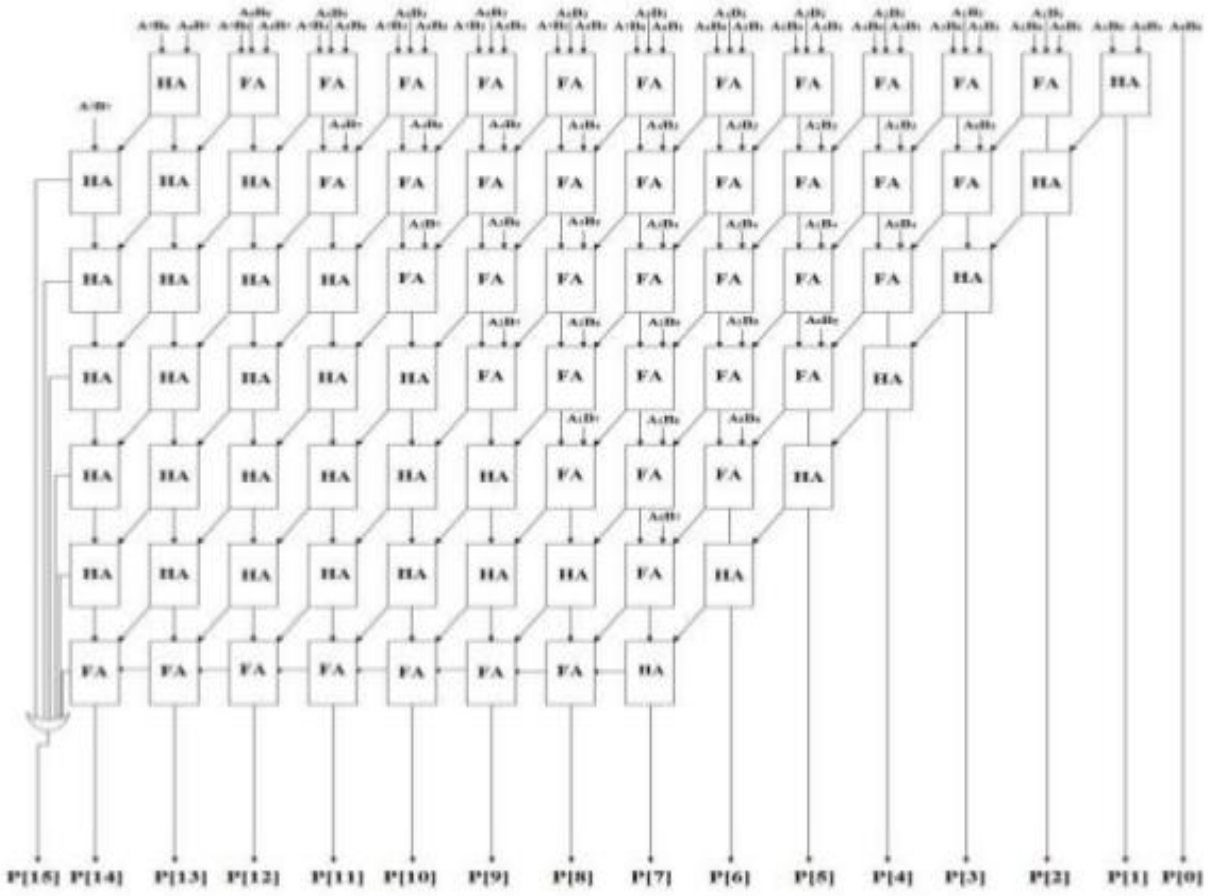

Figure 2. Vedic multiplier

IV DADDA MULTIPLIER: Dadda multiplier is another type of structural multiplier. This multiplier was invented by computer scientist Luigi Dadda in 1965. Dadda multiplier undergoes four stages i.e. generation of partial products, formation of delta structure and reduction of partial products and addition of reduced matrix. In order to realize the minimum number of reduction stages, the height of each intermediate matrix is not more than 1.5 times the height of its successor. Here also, the adders are used to add the bits height wise or column wise. Here adders are not extensively used as in case of Wallace multiplier. Here adders are used just to make the height apt of each intermediate matrix. A. Example Taking the same example that was taken in case of Wallace multiplier, that is we have two decimal numbers 99 and 78 which are to be multiplied. Step 1: Generation of Partial Products.

Step 2: Formation of delta structure. In this step, all columns of the matrix are shifted upwards to form an inverted delta structure. The structure of the inverted delta so formed

Step 3: Reduction of partial products. In Dadda multiplier, height of the partial products are reduced but after forming an inverted delta structure, as described in step 2. Here also adders are used to reduce the height of the matrix. In Dadda multiplier, first the sum from the adder is placed followed by the vacant or unused bits and later the carry from the previous stage is placed. This is the format of arrangement of heights in case of Dadda multiplier.

Step 3: Addition of partial products. Then the matrix of height two is added by any known adder like carry select adder or parallel adder etc. The final sum which will be the result of the multiplication

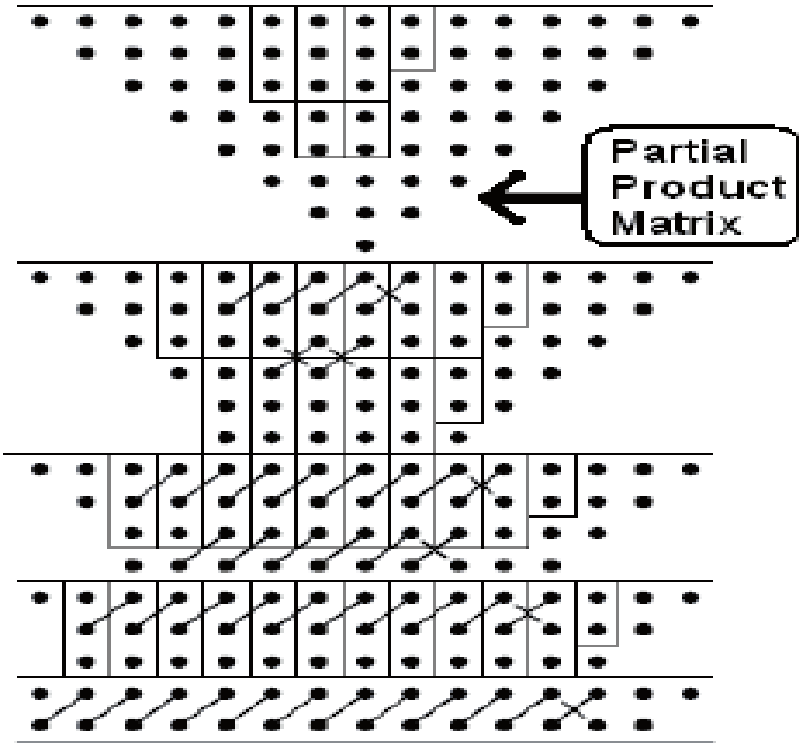

Figure 3. Dadda 8 bit multiplier

V SIMULATION RESULT: Wallace multiplier, Vedic multiplier and Dadda multiplier are simulated in cadence. The Simulation results include schematic and area, power and delay of all the three multipliers.

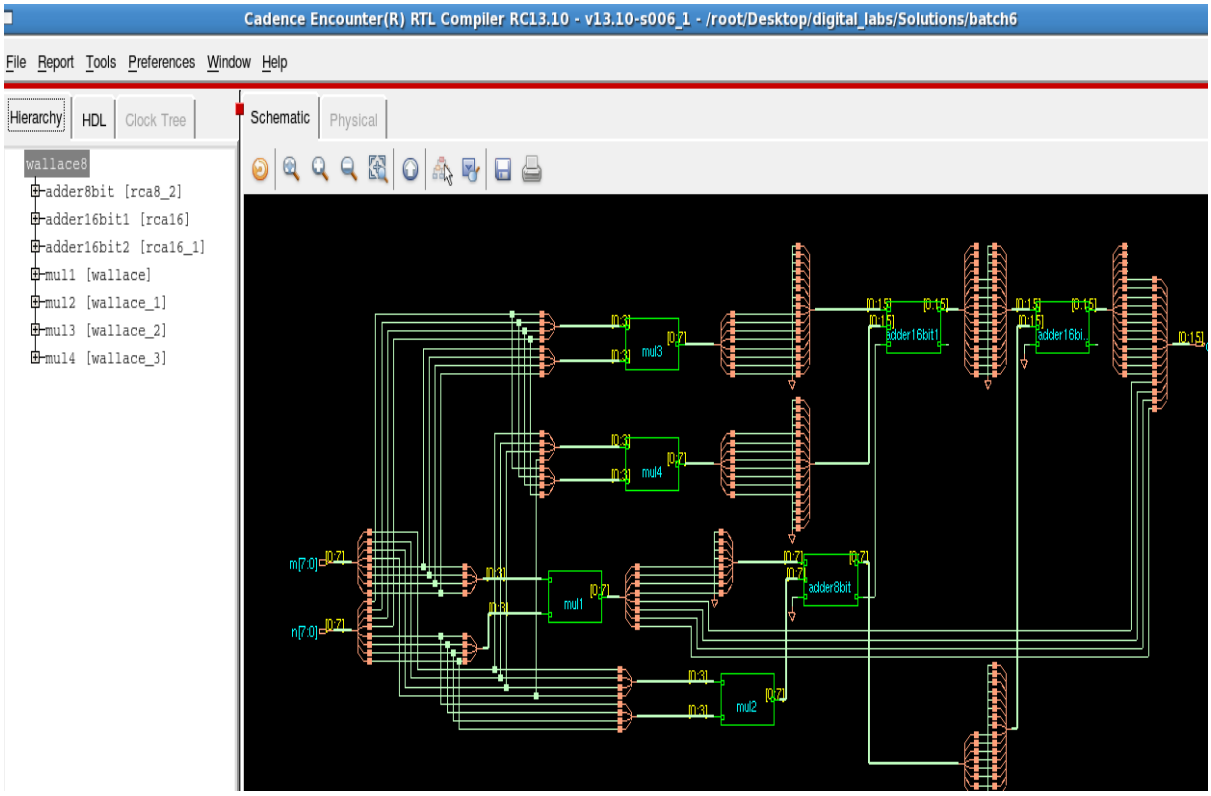

Figure 4.Wallace 8 bit multiplier schematic

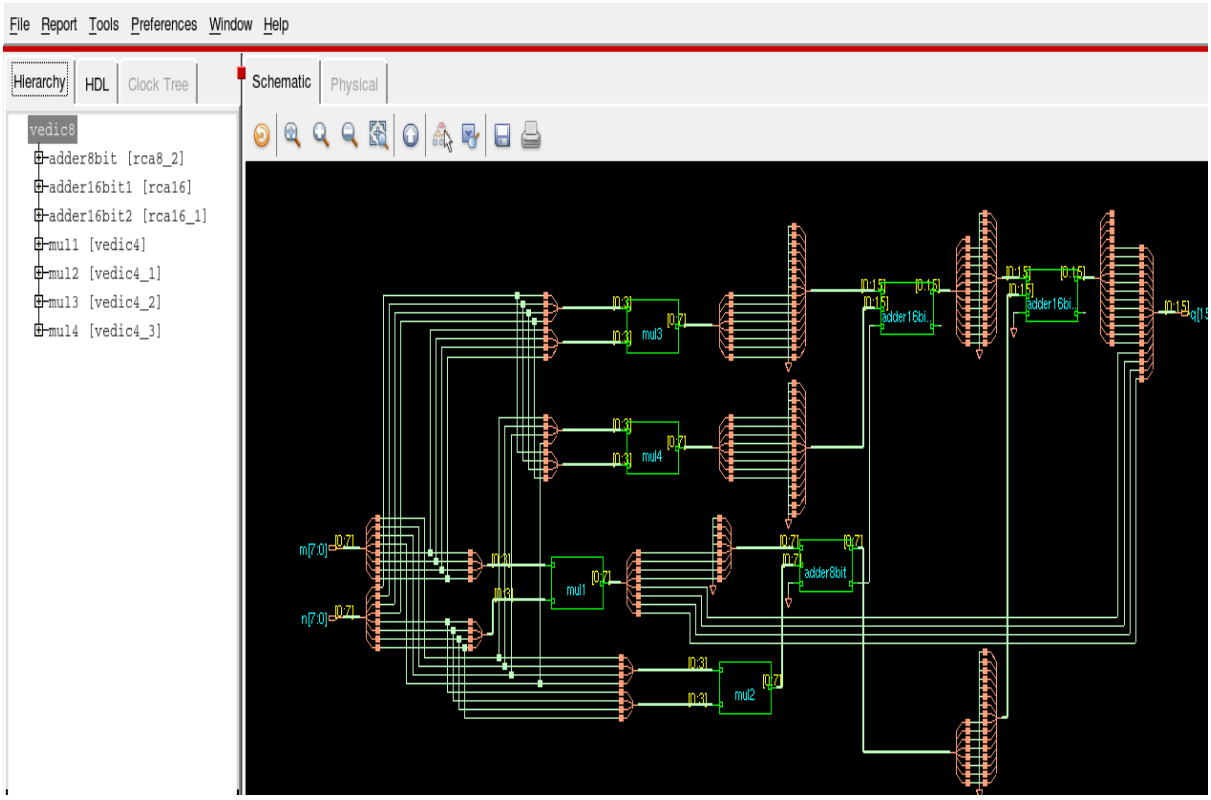

Figure 4.Vedic8 bit multiplier Schematic

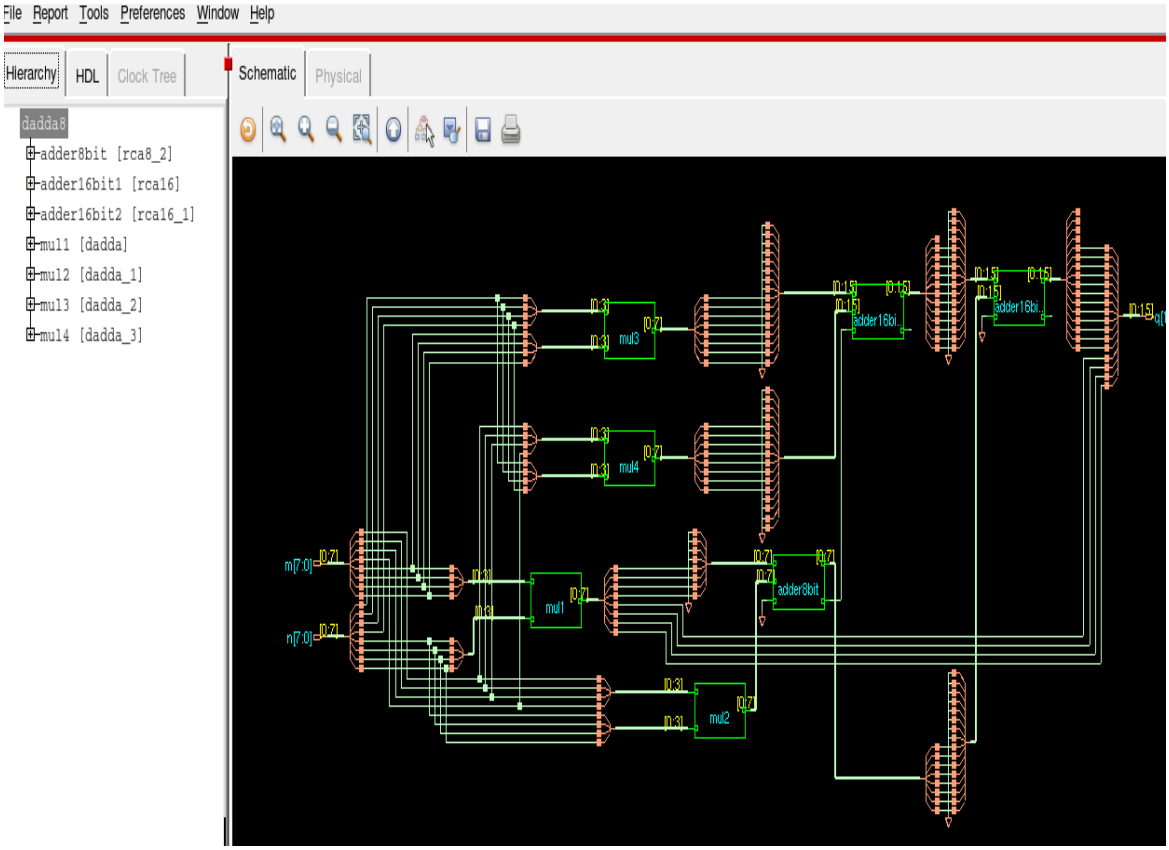

Figure 4.Dadda8 bit multiplierSchematic

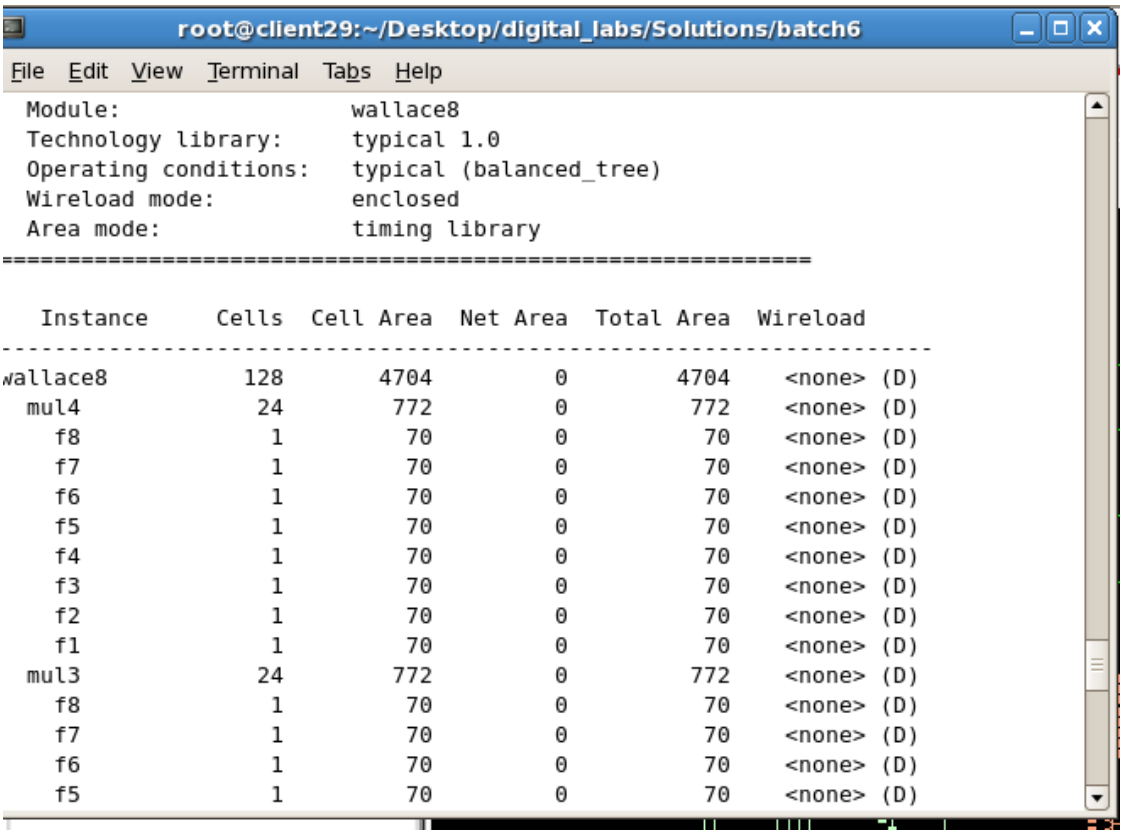

Figure 4.Wallace 8 bit multiplier area

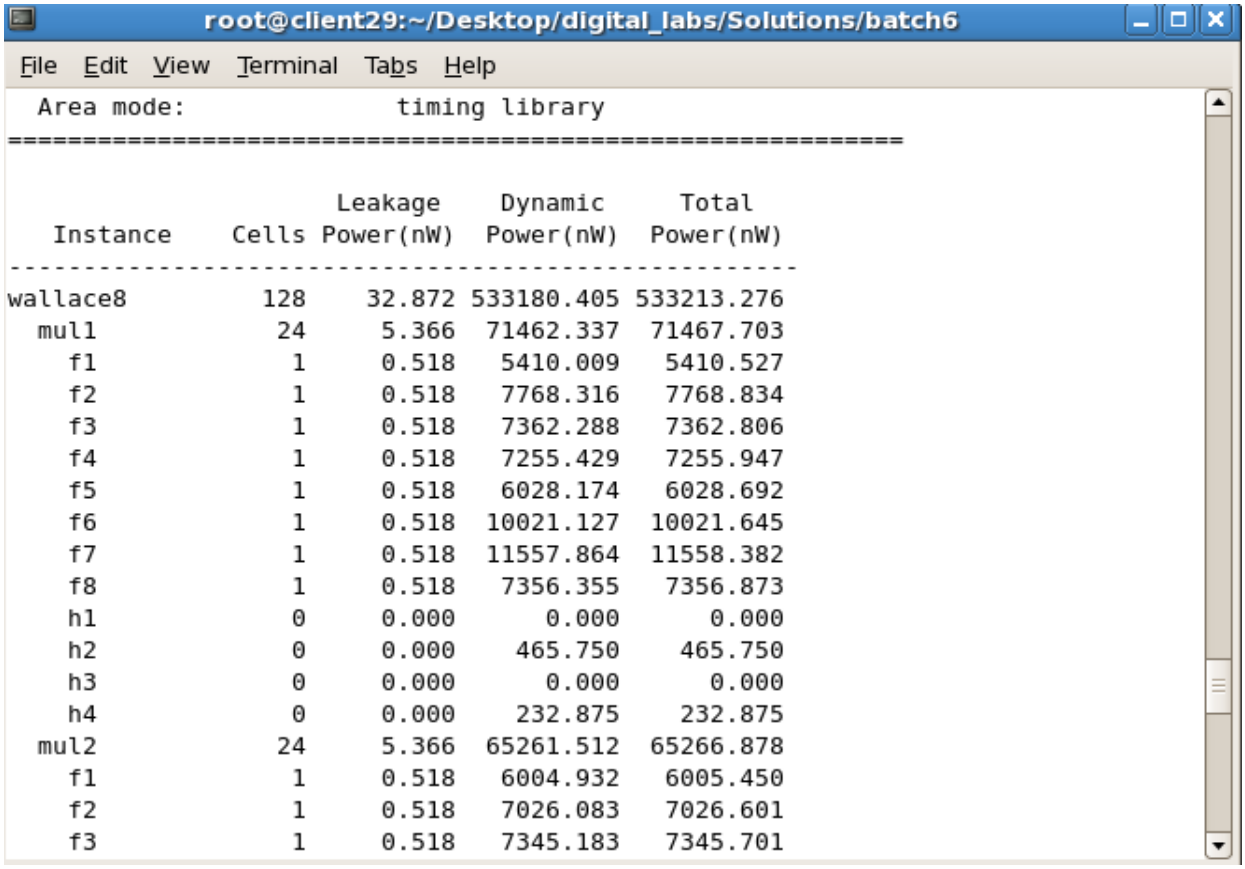

Figure5.Wallace 8 bit multiplier power

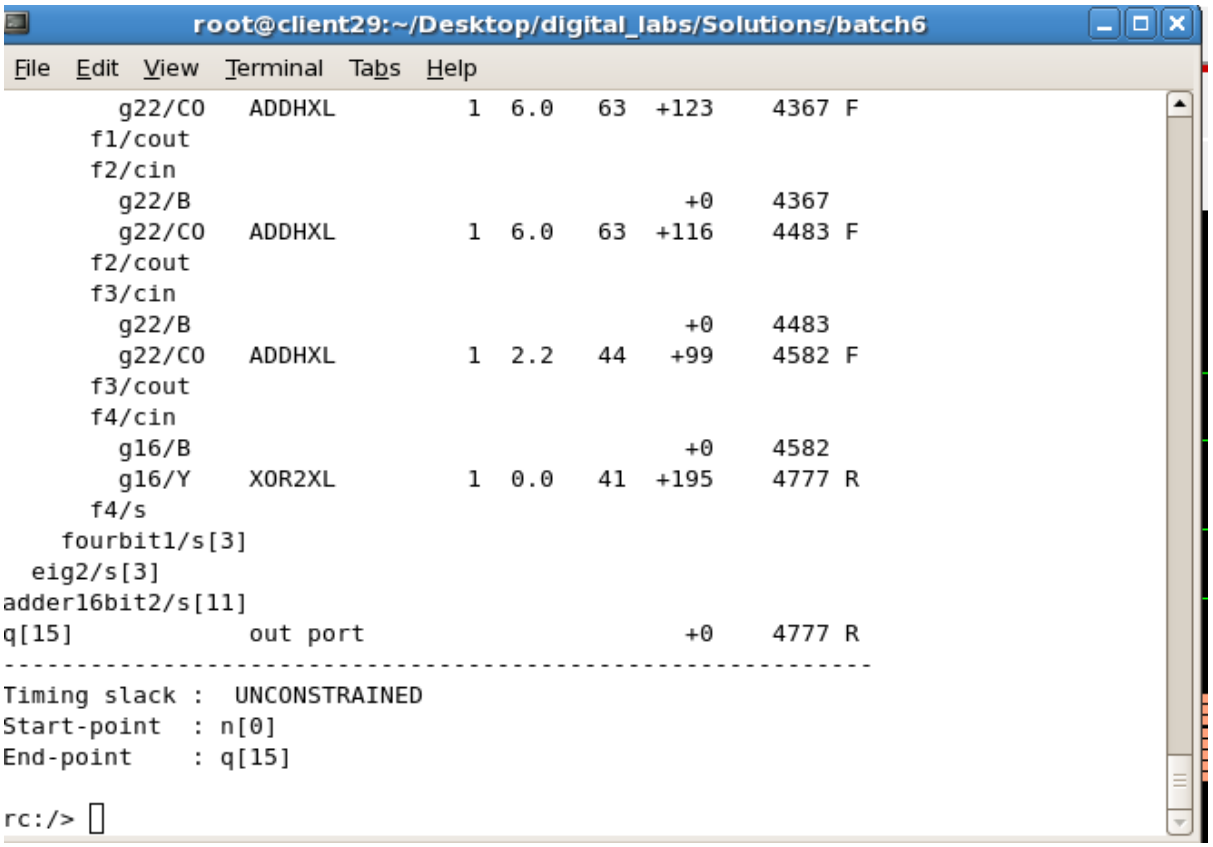

Figure6. Wallace 8 bit multiplier delay

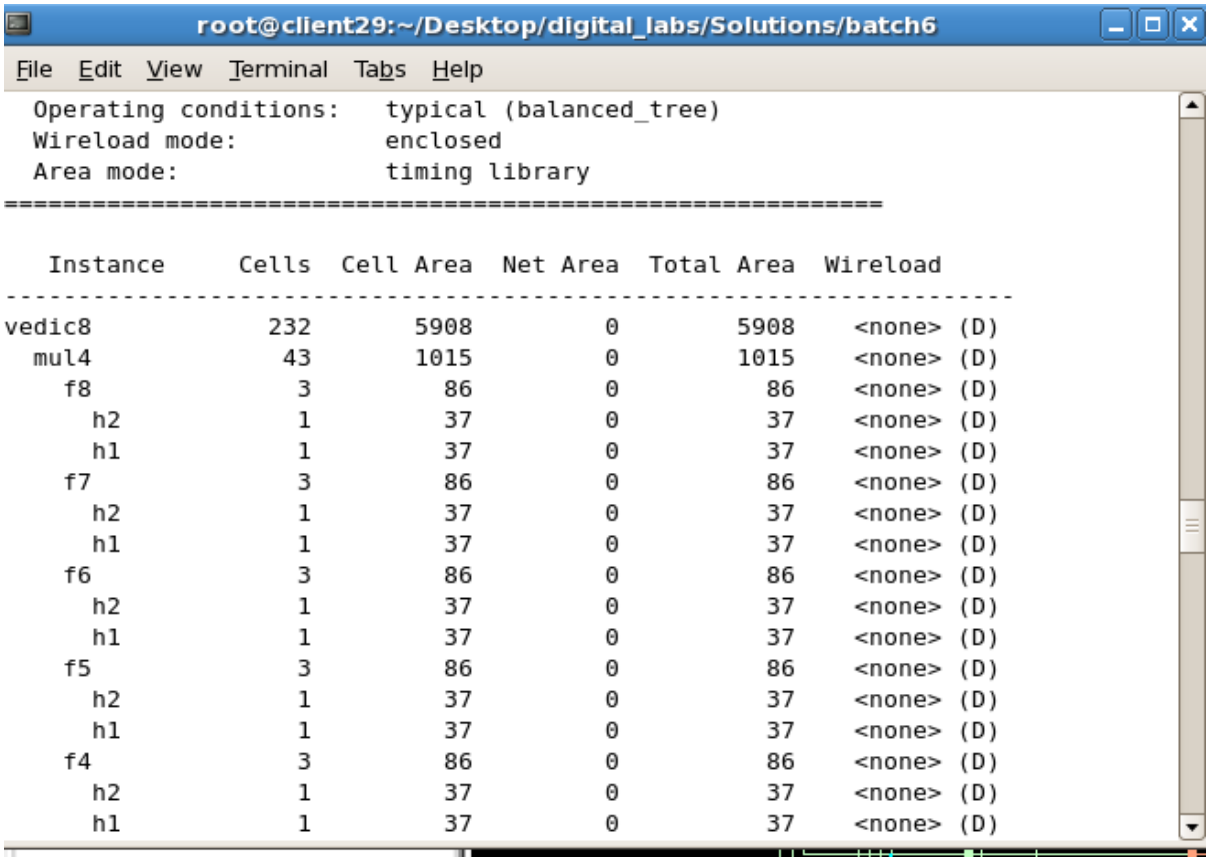

Figure 7.Vedic 8 bit multiplier area

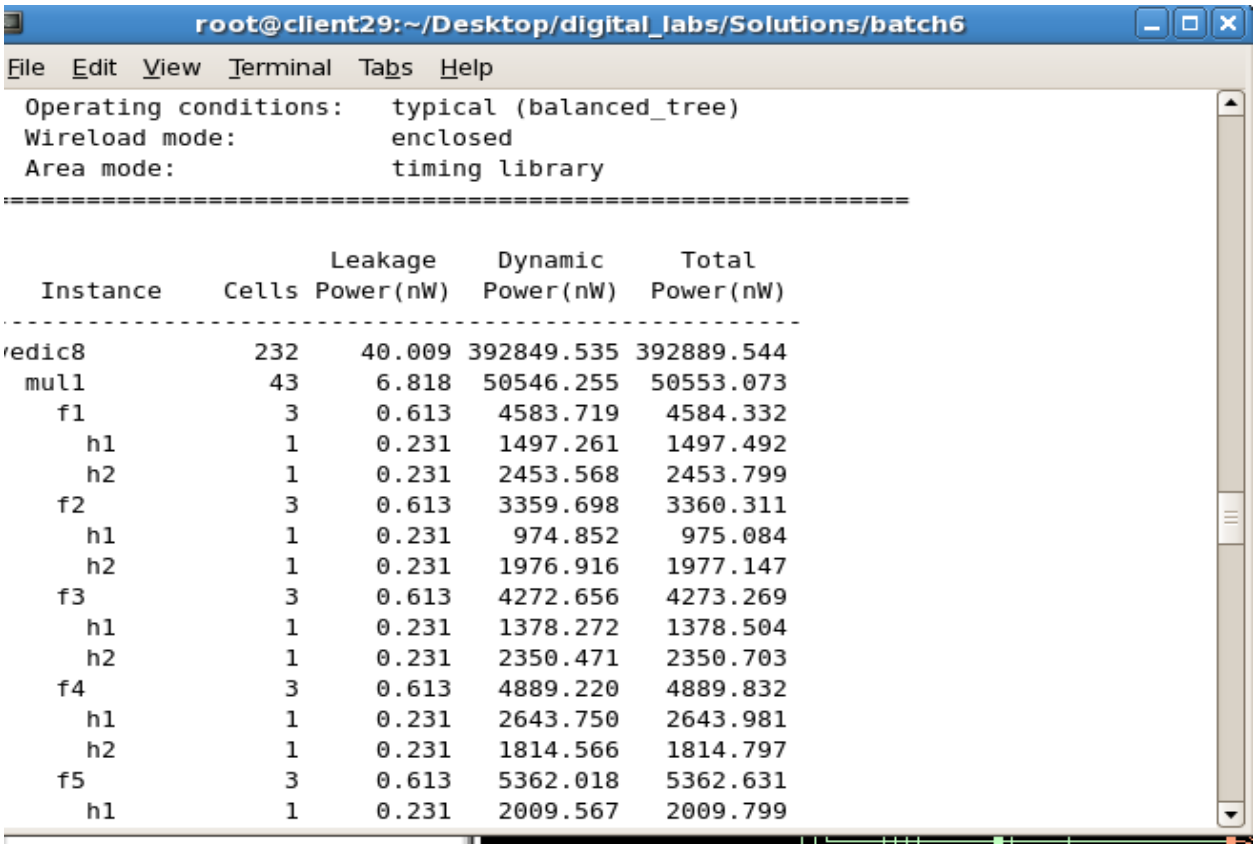

Figure 8.Vedic 8 bit multiplier power

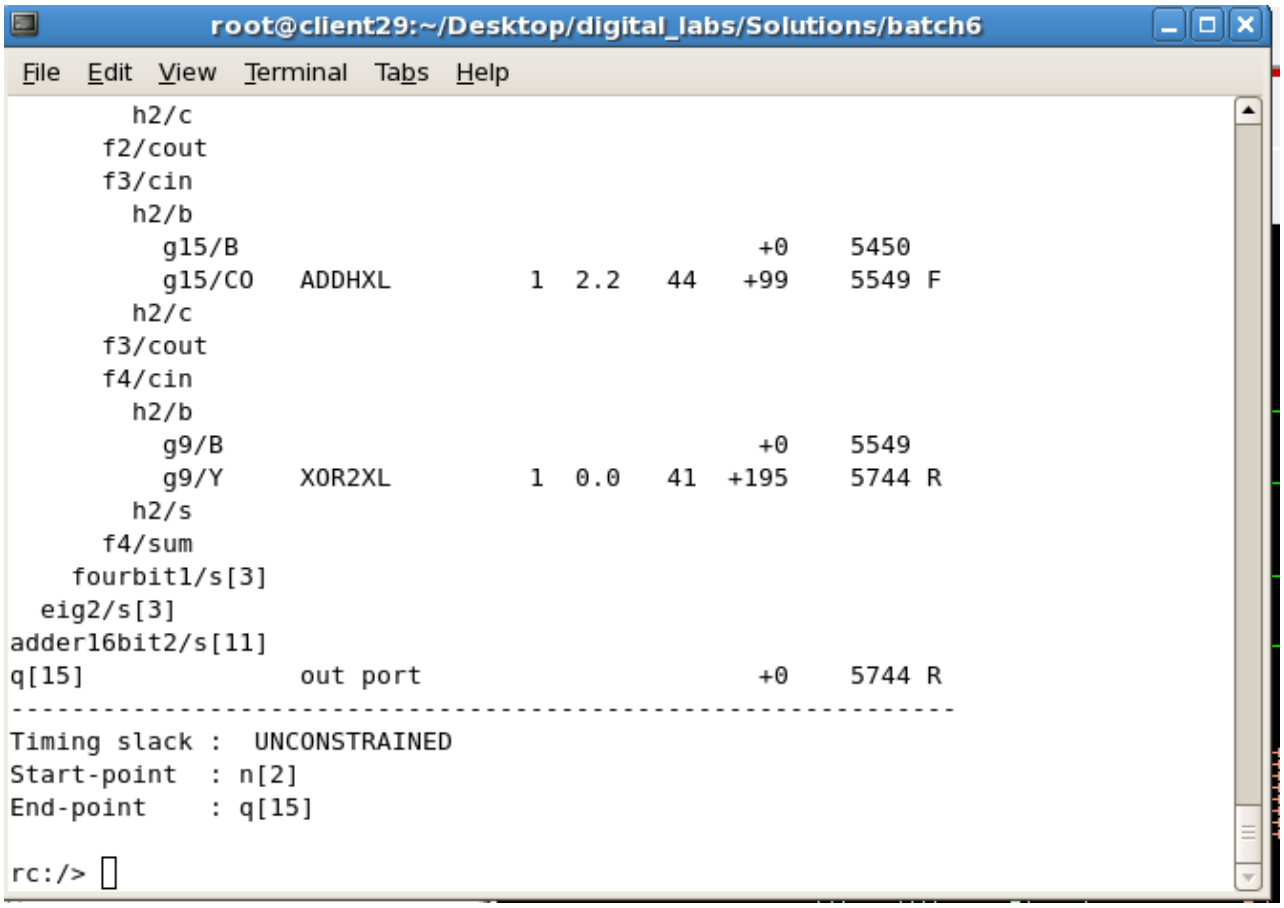

Figure 9.Vedic 8 bit multiplier delay

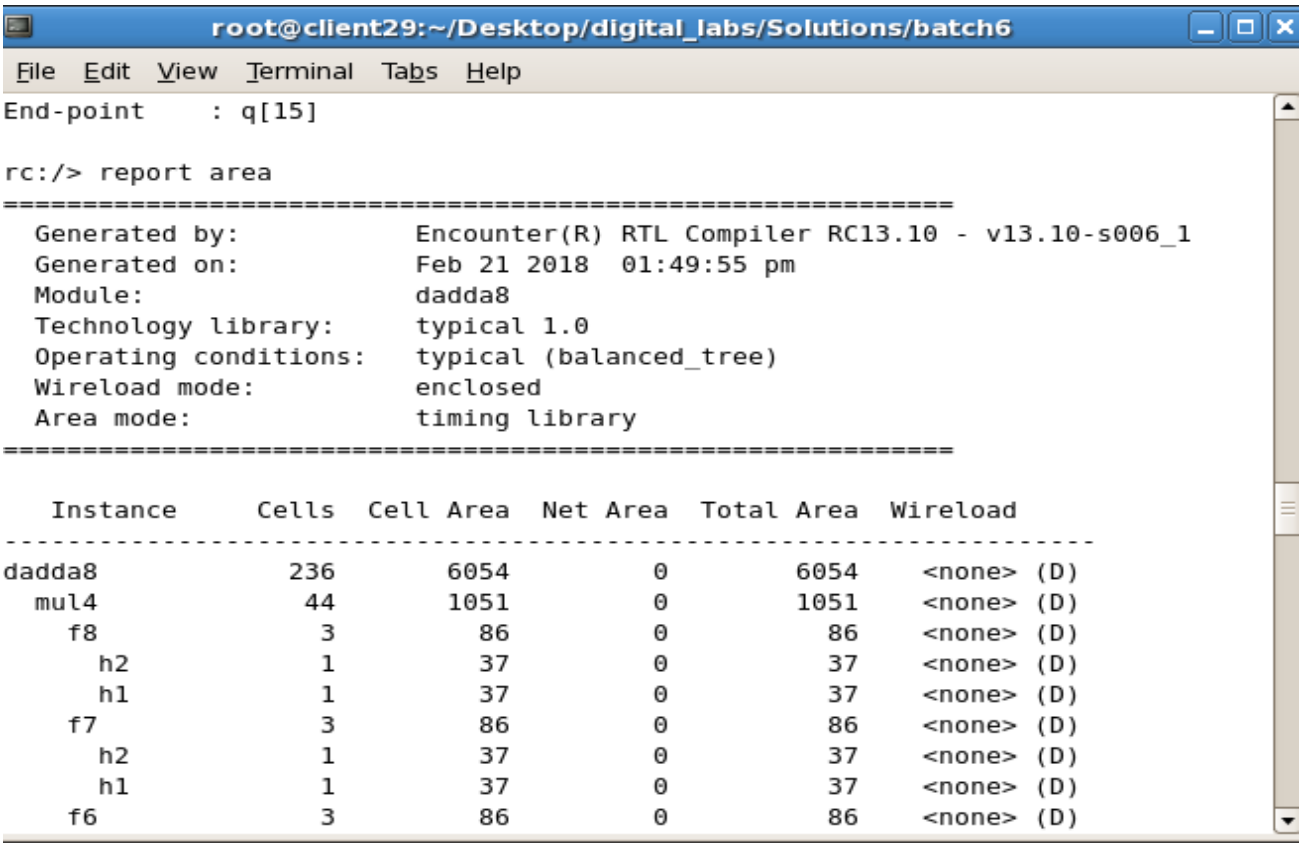

Figure10. Dadda 8 bit multiplier area

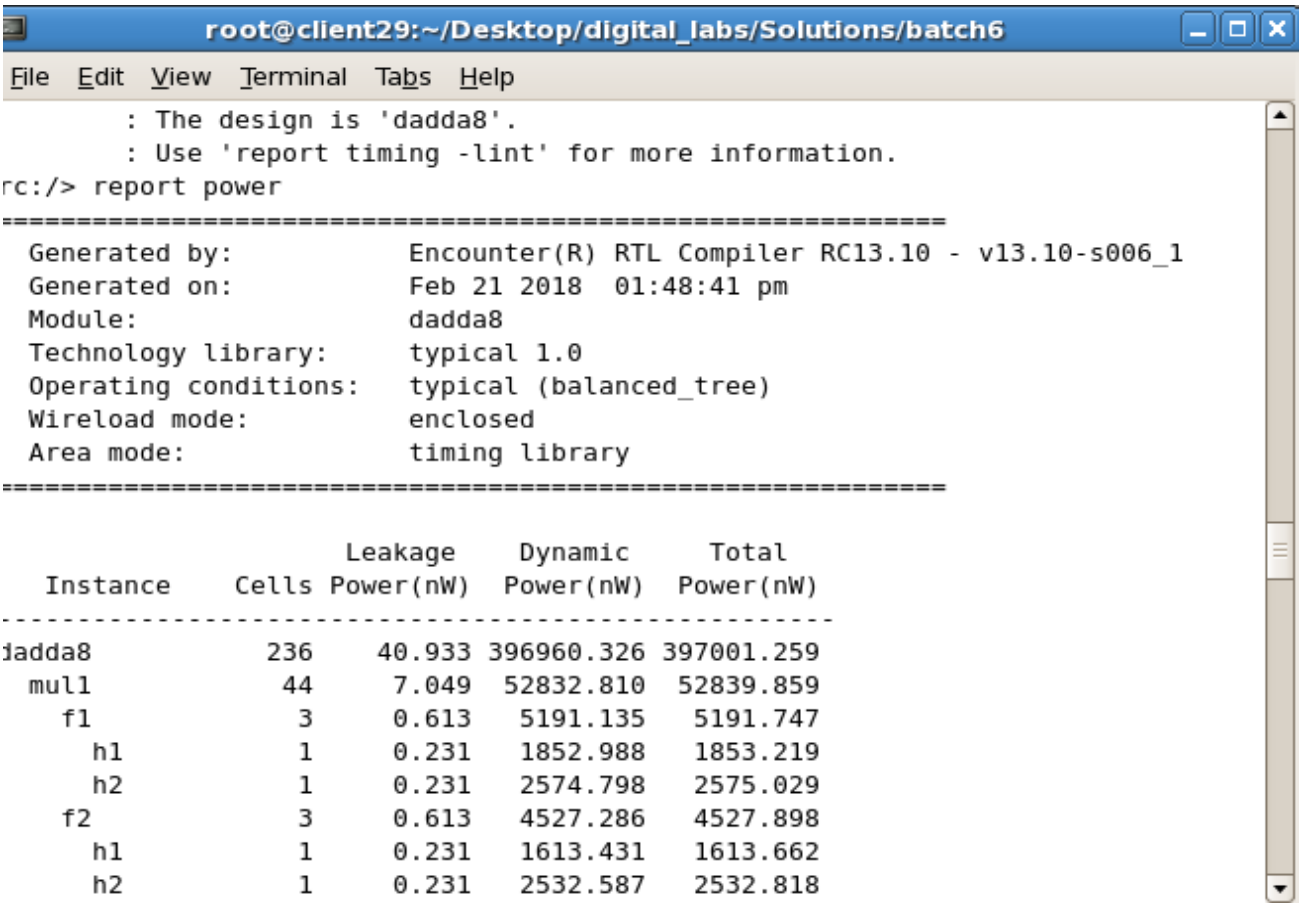

Figure 11.Dadda 8 bit multiplier power

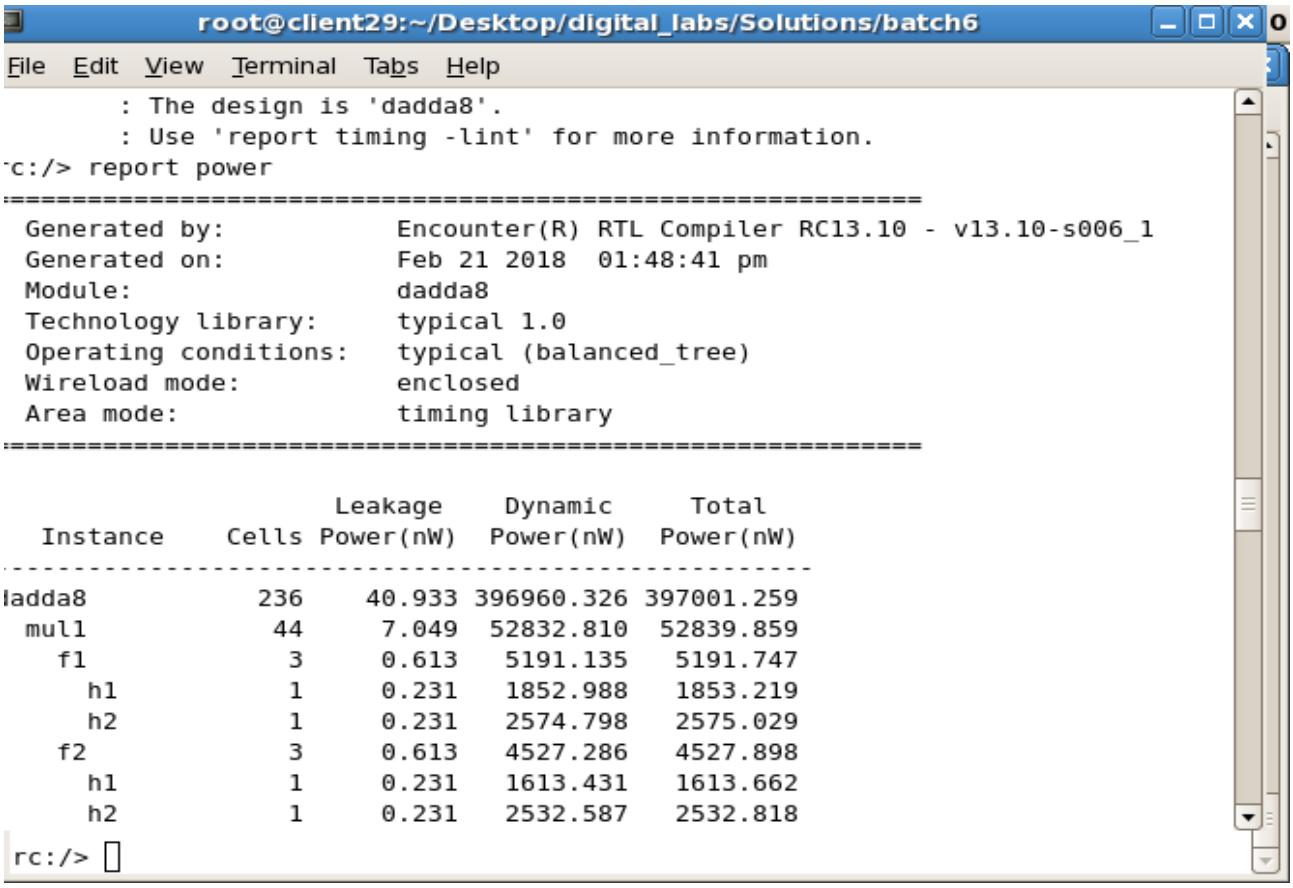

Figure 12.Dadda 8 bit multiplier delay

VI COMPARISON

Comparison of Wallace, Vedic and Dadda multipliers are shown below where parameters arearea, power requirement and delay.

Parameters	Area(μm^2)	Delay(ps)	Power(µW)
Wallace	4704	4777	533.21
Vedic	5908	5744	392.88
Dadda	6054	6012	397.00

On the basis of simulation performed, it can be concluded that Area and delay required by Wallace multiplier is less i.e, 4704$\mu m^2$and 4777ps respectively and power requirement is less for Vedic multiplier. The above comparison is done using RCA(Ripple carry adder).

