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Comparative Analysis of Full Adders Using different MOS Technologies

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Abstract- *With the development in the fabrication techniques the numbers of the transistors on a chip are increasing at much faster rate, results in the very large scale integration. This paper discusses the comparative analysis of full adder circuits in terms of higher speed and size. All these three parameters depend upon each other and trade-off exists within these. A 4bit adder is designed using different MOS technologies These Techniques include CMOS technology designing with transmission gate and designing adder with combination of Complimentary Pass Logic and Transmission gate & simulated using 180nm, 130nm & 100nm technology files*

Keywords-CMOS Transmission Gate (TG), Pass-Transistor Logic (PTL), Complementary Pass transistor Logic (CPL),), full adder Power, Delay, Channel Length.

I. INTRODUCTION

The extensive development in the field integrated circuits has intensified the research efforts in low power microelectronics. The low-power, high speed, small size design has become a major design consideration. This largely affects the design complexity of many Function units such as multiplier and algorithmic logic unit (ALU). The limited power supply capability of present battery technology has made power consumption an important issue in portable devices. The speed of the design is limited by size of the transistors, parasitic capacitance and delay in the critical path. The driving capability of a full adder is very important as full adders are mostly used in cascade configuration, where the output of one provides the input for other. If the full adders lack driving capability then it requires additional buffer, which consequently increases the power dissipation. In the last decade, the full adder has gone through substantial improvement in power consumption, speed and size, but at the cost of weak driving capability and reduced voltage swing. However, reduced voltage swing has the advantage of lower power consumption [1]. There is no ideal full adder cell that can be used in all types of applications [2]. Hence novel architectures such as CMOS Transmission Gate (TG), Pass-Transistor Logic (PTL), Complementary and Pass-transistor Logic (CPL) [3] their combinations (Hybrid) are commonly used in designing full adder cells are proposed to meet the requirements. Each design style has its own share of advantages and disadvantages. In this paper, a brief description of the evolution of full adder circuits in terms of lesser power consumption, higher speed and lesser chip size given. Initially the most conventional 28 transistor full adder is implemented and then gradually full adders consisting of as less as 14 transistors are discussed which are simulated using different technology files 10nm, 130nm and 100nm.

II. EXPERIMENTAL WORK

Designing is started at the transistor level in tanner schematic editor tool from a logic diagram along with design specifications. The logic circuit is first translated into a CMOS circuit and the initial layout is done in S-Edit tool. From the layout, a circuit extraction program calculates all of the important parasites. Once a full circuit description is obtained from the initial layout, we analyze the circuit for DC and transient performance by using the circuit level simulation program, T-SPICE, and then compare the results with the given specifications. If the initial design fails to meet any one of the specifications, we devise an improved circuit design to meet the design objective. Then the improved design will be implemented into a new layout and the design analysis cycle will be repeated until all of the design specifications are met. Lastly output waveforms are generated using W-Edit.

Further simulation results shown below are for 4-bit adders and schematics are for 1 bit only but it may also be configured for 4-bit. figure1, figure2, figure3 represents the schematic for 1 bit full adder using CMOS, combination of Transmission Gate and CPL and Transmission Gate logic families. Similarly analysis based on size and speed for adders using aforesaid MOS designing techniques. Table1-9 shows the delay calculations.

Delay parameter results also shown here down in table1 for the respective supply voltages in 100 nm technology node for 14T, table2: Delays for the respective supply voltages in 130 nm technology node for 14T, Table 3: Delays for the respective supply voltages in 180 nm technology nodes for 14T. Table 4: Delays for the respective supply voltages in 100 nm technology nodes for 16T Delays for the respective supply voltages in 100 nm technology node for 16T Table 5: Delays for the respective supply voltages in 130 nm technology node for 16T. Table 6: Delays for the respective supply voltages in 180

nm technology node for 16T. Table 7: Delays for the respective supply voltages in 100 nm technology node for transmission gate. Table 8: Delays for the respective supply voltages In 130 nm technology nodes for transmission gate Table9: Delays for the respective supply voltages in 180 nm technology node for transmission gate.

2.1 **Schematic design of 1 bit adder using different MOS technologies**

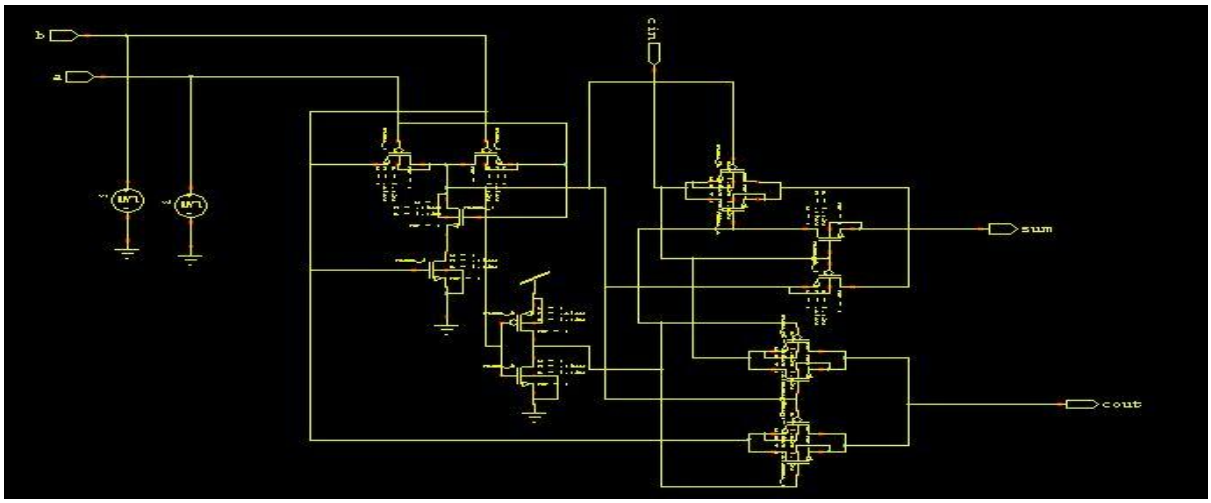

Figure 1: Schematic design of 1bit adder using CMOS

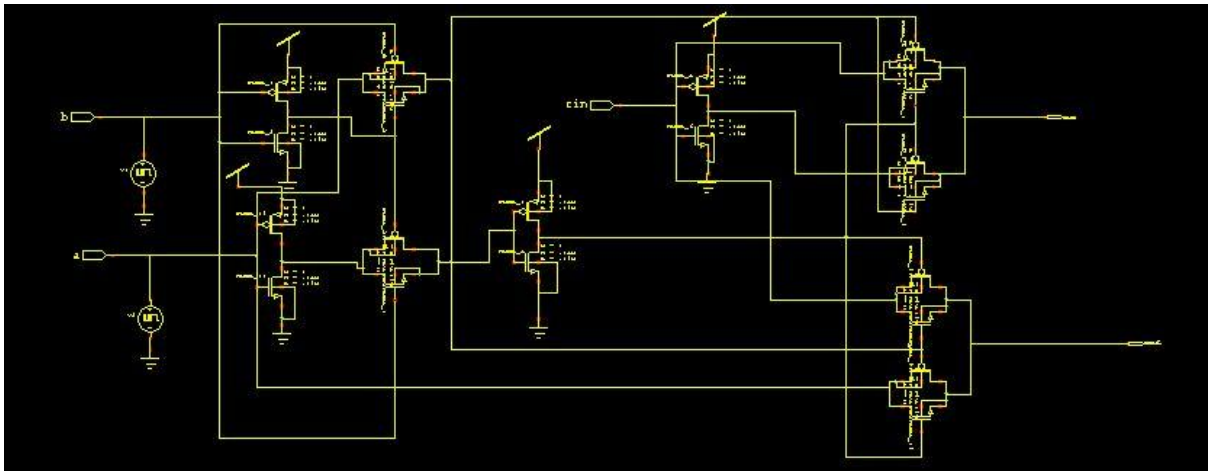

Figure 2: 1 bit Full adder using transmission gate

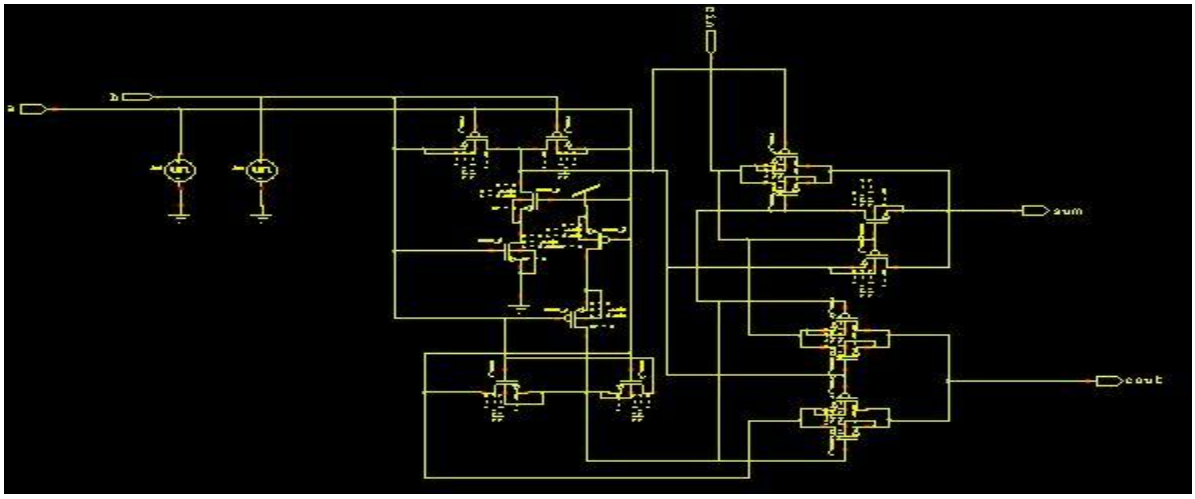

Figure 3: 1 bit full adder using CPL and transmission gate

2.2 Delay calculation

Table 1 : 4 bit Delays for the respective supply voltages in 100 nm technology node for 14T

Technology node (nm)	Input	Output	Rise time (ns)	Fall time (ns)
100	A	sum	262.1780p	38.0241n
	B	sum	18.7378n	24.1315p
	cin	sum	56.7378n	75.9763n
	A	cout	38.2324n	38.0035n
	B	cout	19.2321n	3.5282p
	cin	cout	18.7678n	75.9964n

Table 2: Delays for the respective supply voltages in 130 nm technology node for 14T.

Technology node (nm)	Input	Output	Rise time (ns)	Fall time (ns)
130	A	sum	348.2076p	1.4100n
	B	sum	18.6517n	36.5899n
	cin	sum	56.6517n	112.5900n
	A	cout	38.1707n	38.0039n
	B	cout	19.1707n	3.9140p
	cin	cout	18.8292n	75.9960n

Table 3: Delays for the respective supply voltages in 180 nm technology node for 14T.

Technology node (nm)	Input	Output	Rise time (ns)	Fall time (ns)
180	A	sum	367.8073p	38.0254n
	B	sum	18.6321n	25.3989p
	cin	sum	56.6321n	75.9746n
	A	cout	38.3180n	38.0045n

	B	cout	19.3180n	4.5804p
	cin	cout	18.6819n	75.9954n

Table 4: Delays for the respective supply voltages in 100 nm technology node for 16T.

Technology node (nm)	Input	Output	Rise time (ns)	Fall time (ns)
100	A	sum	391.3723p	62.1647p
	B	sum	18.6086n	37.9378n
	cin	sum	56.6086n	113.9378n
	A	cout	38.2621n	38.0127n
	B	cout	19.2621n	12.7196p
	cin	cout	18.7378n	75.9872n

Table 5: Delays for the respective supply voltages in 130 nm technology node for 16T.

Technology node (nm)	Input	Output	Rise time (ns)	Fall time (ns)
130	A	sum	37.6767n	94.4702n
	B	sum	323.2388p	18.4702n
	cin	sum	19.3232n	19.5297n
	A	cout	18.0830n	75.0434n
	B	cout	19.9169n	956.6019p
	cin	cout	38.9169n	38.9566n

Table 6 : Delays for the respective supply voltages in 180 nm technology node for 16T.

Technology node (nm)	Input	Output	Rise time (ns)	Fall time (ns)
180	A	sum	362.8550p	16.6425p
	B	sum	18.6371n	37.9833n
	cin	sum	56.6371n	113.9834n
	A	cout	38.2644n	38.0129n
	B	cout	19.2644n	12.9256p
	cin	cout	18.7355n	75.9870n

Table 7 : Delays for the respective supply voltages in 100 nm technology node for transmission gate.

Technology node (nm)	Input	Output	Rise time (ns)	Fall time (ns)
100	A	sum	197.5460p	38.1455n
	B	sum	18.8024n	145.5171p
	cin	sum	56.8024n	75.8544n
	A	cout	33.4896p	18.7205n
	B	cout	18.9665n	56.7205n

	cin	cout	56.9665n	132.7205n

Table 8 : Delays for the respective supply voltages in 130 nm technology node for transmission gate.

Technology node (nm)	Input	Output	Rise time (ns)	Fall time (ns)
130	A	sum	146.2342p	38.1154n
	B	sum	18.8537n	115.4752p
	cin	sum	56.8537n	5.8845n
	A	cout	38.2396n	38.0113n
	B	cout	19.2396n	11.2999p
	cin	cout	18.7604n	75.9887n

Table 9: Delays for the respective supply voltages in 180 nm technology node for transmission gate.

Technology node (nm)	Input	Output	Rise time (ns)	Fall time (ns)
180	A	sum	220.7258p	38.0707n
	B	sum	18.7792n	70.7452p
	cin	sum	56.7792n	75.9292n
	A	cout	27.0261p	18.8258n
	B	cout	18.9729n	56.8258n
	cin	cout	56.9729n	132.8258n

III. CONCLUSION

The objective of this research was to implement the low transistor count 14T and 16T and TGA full adders and compare them with the reduced technology files for Delay and the power consumption of the full adders. The primary process variation parameters were identified to determine the effect of technology files and the power consumption as we going down toward technology file. it is observed that the power consumption is also reduces as we goes toward a low technology file,. For a 100nm technology file supply voltage is 1v and for 130 supply voltage is 1.3v and for a 180nm he supply voltage is 1.8 in these cases a good waveform results is coming. The 14T full adder dissipated low power compared to the 16 T and TGA. With the change in process variations, the TGA adder has the minimum absolute variance in delay.

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