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A 2.5GHz CMOS FOLDED CASCODE OPERATIONAL AMPLIFIER

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Abstract – *In most operational amplifiers, speed and accuracy are basically determined by the settling behavior in time domain. High speed calls for a single pole response and a large unity gain frequency. In this paper a folded cascode operational amplifier of general purpose is presented. The results presented are obtained through schematic level simulation using the pyxis schematic in mentor graphics tool and a standard 130nm technology process. The results obtained include open-loop gain of 58 dB, the Gain Bandwidth product of 2.5GHz. Without additional components, the high frequency response of the classical folded cascode operational amplifier is improved.*

Keywords *– Folded cascode operational amplifier, Gain Bandwidth product, Schematic level simulation, High frequency response, open-loop gain.*

I.INTRODUCTION

Operational amplifier is an integral part of analog and mixed signal system. The design of high performance operational amplifier has always been one of the hotspots of analog integrated circuit design as its performance directly affects the overall performance of circuits and system. With each generation of CMOS technology, the decrease in supply voltage and transistor length continuously brings more complex issue for the design of operational amplifier. Cascode amplifiers can have quite large gains and reduce significantly the miller effect, which gives them an improved frequency response compared with that of other amplifiers [7].

Speed & accuracy are two of the most important properties of analog circuits; however optimizing circuits for both aspects leads to contradictory demands. In a wide variety of CMOS analog circuits, such as switched-capacitor filters, sample and hold amplifiers and pipeline A/D converters. Speed and accuracy are determined by the settling behavior of the operational amplifiers. Fast settling requires a high unity gain frequency and a single pole settling behavior of the operational amplifier where as accurate settling requires a high dc gain [1].

The realization of a CMOS operational amplifier that combines high dc gain with high unity gain frequency has been a difficult problem. The high gain requirement leads to multistage designs with long channel devices biased at low current levels, where as the high unity gain frequency requirement calls for a single stage design with short channel devices biased at high bias current levels [1].

The design of high frequency circuits fabricated in CMOS technologies is very attractive, mainly for RF circuits & other applications. The scaling down of the transistor dimensions allows increasing the frequency range of operation of the MOS circuits. For actual advanced technologies, unity gain frequency (f_t) of the order of 2-10GHz is commonly found. The folded cascode operational amplifier is commonly preferred for high frequency applications [4].

In nanometer CMOS technologies, the folded-cascode amplifier is attractive because of its advantages such as wide input common-mode range and relatively large output swing. Therefore, among many operational amplifier topologies, Folded- cascode operational amplifier topology is one of the most common topologies that have high open-loop DC gain and proper frequency response [7]. Thus, folded cascode operational amplifier offers self compensation, good input common mode range, and gain of a two stage operational amplifier.

MOS transistors provide DC gain and amplification in saturation region only. To ensure the device is working under saturation region, bias potentials are turned accordingly. Also, the current distribution in input and output stages along with the overdrive voltages of each branch is chosen according to meet the design specifications. The disadvantage of folded cascode operational amplifier is high power consumption [7] in comparison with the telescopic operational amplifier.

The folded cascode operational amplifier designed achieved a unity gain frequency of 2.55GHz with a 1pf load at 130nm node CMOS technology. Open-loop gain obtained at nominal conditions is 58dB. The high unity gain frequency enables the CMOS folded cascode operational amplifier suitable for high frequency applications.

II.FOLDED CASCODE AMPLIFIER

Folded cascode operational amplifier, compared to the ordinary operational amplifier, is a high gain, a single-pole operational amplifier with large output swing, because compared to two stage operational amplifier or multi stage operational amplifier, the biggest advantage of single pole amplifiers is that the phase margin is very high and stable. Secondly, its small signal gain can be very large [7].

Folded cascode operational amplifier uses a cascading in the output stage combined with an unusual implementation of differential amplifier to achieve good input common-mode input range. Thus, folded cascode operational amplifier offers self compensation, good input common mode range, and gain of a two stage operational amplifier. In case of telescopic cascode topology, although the current required is less as compared to folded cascode but to ensure every transistor to be in saturation region is quite harder than in folded cascode topology. The name "folded cascode" comes from folding down n-channel cascode active loads of a differential pair and changing the MOSFET to p-channel. This operational amplifier has good PSRR as compared to two stage operational amplifier and telescopic operational amplifier [7].

The folded cascode operational amplifier has a push pull output stage which can sink or source current from the load. The exact match of the currents in the differential amplifier is not demanded by the folded cascode op amp since extra current can flow in or out of the current mirrors. While the bias current of the conventional delivers the current to both the input devices and the cascode devices since they are stacked together, the bias current I_{ss} of the folded cascode supplies only the input devices. Additional bias currents are required to add necessary bias current. In general, the folded cascode connection dissipates more power. The gain of folded cascode op amp is normally lower than that of a corresponding conventional folded cascode amplifier due to lower impedances of devices in parallel [7].

The voltage gain of the Op-Amp is given by $A_V = G_m R_o$.

Where $R_o = (g_{m7} r_{07} (r_{01} \| r_{09})) \| (g_{m5} r_{05} r_{03})$.

The maximum output voltage swing of the folded cascode with proper choice of bias voltages, the lower end of the swing is given by $V_{OD3}+V_{OD5}$ and the upper end of the swing is given by $V_{DD}-(|V_{OD7}|+|V_{OD9}|)$. Thus, the peak to peak swing on each side is equal to $V_{DD}-(V_{OD3}+V_{OD5}+|V_{OD7}|+|V_{OD9}|)$. Thus, voltage swing of folded cascode amplifier is slightly greater than that of telescopic configuration.

The folded cascode operational amplifier does not require perfect balance of currents in the differential amplifier because excess dc currents can flow into or out of the current mirror.

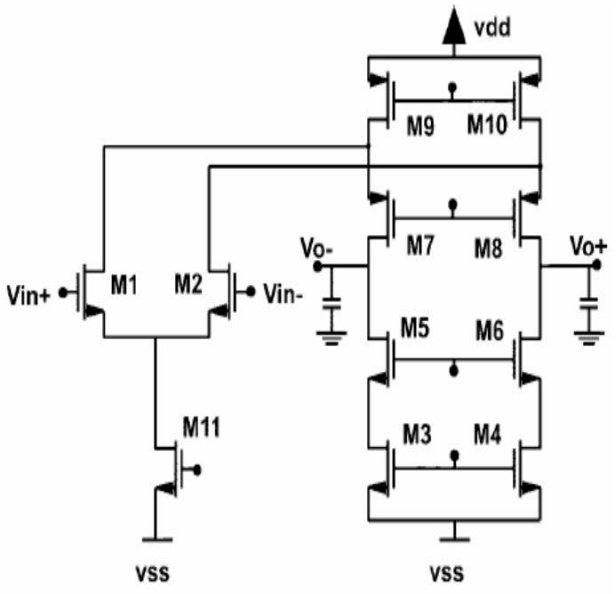

Figure 1.Folded cascode operational amplifier.

The bias currents I_3, I_4 and I_5 of the folded cascode operational amplifier should be designed so that the dc current in the cascode mirror never goes to zero. For example, suppose V_{in} is large enough so that M_1 is ON and M_2 is OFF. Then, all of

I_3 flows through M_1 and none through M_2, resulting in $I_1=I_3$ and $I_2=0$. If I_4 and I_5 are not greater than I_3, then the current I_6 will be zero. To avoid this, the values of I_4 and I_5 are normally between the values of I_3 and $2I_3$.

III.DESIGN OF FOLDED CASCODE OPERATIONAL AMPLIFIER

The design procedure involves the following sequence of steps. Firstly selecting a specific topology, secondly determining the DC currents, thirdly calculating the W/L ratios of each transistor, at the end deciding the passive component values used in the circuit.

A folded cascode operational amplifier permits us to achieve high output swing. The design procedure assumes that the DC gain (Av), Unity-gain bandwidth (GB), Input common-mode range [V_{in} (min) and V_{in} (max)], Load capacitance (C_L), Slew rate (SR) and Power dissipation (P_{diss}) are given.

1. The first step of the design gives the estimation of the bias current. Assuming the Slew Rate, we have

$$I_{11} = SR*C_L$$

2. Calculate bias currents in output cascodes using following equation.

$$I_9 = I_{10} = 1.2I_{11} \text{ to } 1.5I_{11}$$

3. Design for S_9 and S_7 using the maximum output voltage, V_{out} (max).

$$S_9 = \frac{8I_9}{K_P' V_{SD\,9}^2} \text{ And } S_7 = \frac{8I_7}{K_P' V_{SD\,7}^2}$$

$$\text{Where } V_{DS9}(\text{sat}) = V_{DS7}(\text{sat}) = \frac{V_{DD} - V_{OUT\ (max)}}{2}$$

$$\text{Let } S_9 = S_{10} \text{ and } S_7 = S_8$$

4. Design for S_3, S_4, S_5 and S_6 using the minimum output voltage, V_{out} (min).

$$S_3 = \frac{8I_3}{K_N' V_{SD\,3}^2} \text{ And } S_5 = \frac{8I_5}{K_N' V_{SD\,5}^2}$$

$$\text{Where } V_{DS3}(\text{sat}) = V_{DS5}(\text{sat}) = \frac{V_{OUT\ (min)} - V_{ss}}{2}$$

Let $S_3 = S_4 = S_5 = S_6$

5. Design S_1 and S_2 to achieve desired gain bandwidth product.

$$S_1 = S_2 = \frac{g_{m1}^2}{K_N' I_{11}} = \frac{GB^2 C_L^2}{K_N' I_{311}}$$

6. Design S_{11} to achieve minimum input common mode range.

$$S_{11} = \frac{2I_{11}}{K_N'[V_{in\ (min)} - V_{SS} - \sqrt{\frac{I_3}{K_N' S_1}} - V_{T1}]^2}$$

7. Design S_9 and S_{10} to achieve maximum input common mode range.

$$S_9 = S_{10} = \frac{2I_4}{K_P'(V_{DD} - V_{in\ (max)} + V_{T1})}$$

All the above steps for the design procedure are taken from E. Allen & R. Holberg, CMOS Analog Circuit Design.

IV.SIMULATION RESULTS

The folded cascode operational amplifier is designed using pyxis schematic 130nm technology and the supply voltages used are ±1.8v. The simulation results of folded cascode operational amplifier are shown below. Figure 2 and figure 3 shows the magnitude response and phase response of the folded cascode operational amplifier respectively. The simulations results shows that the folded cascode operational amplifier has a gain of 58dB, unity gain bandwidth of 2.5GHz, phase margin of 35^0 and gain margin of 20dB.

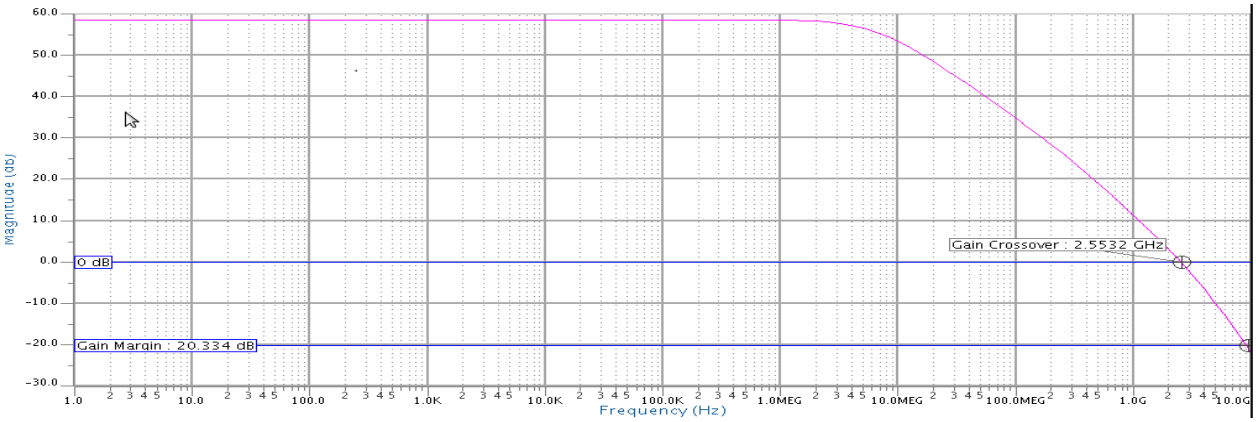

Figure 2.Magnitude response of folded cascode operational amplifier.

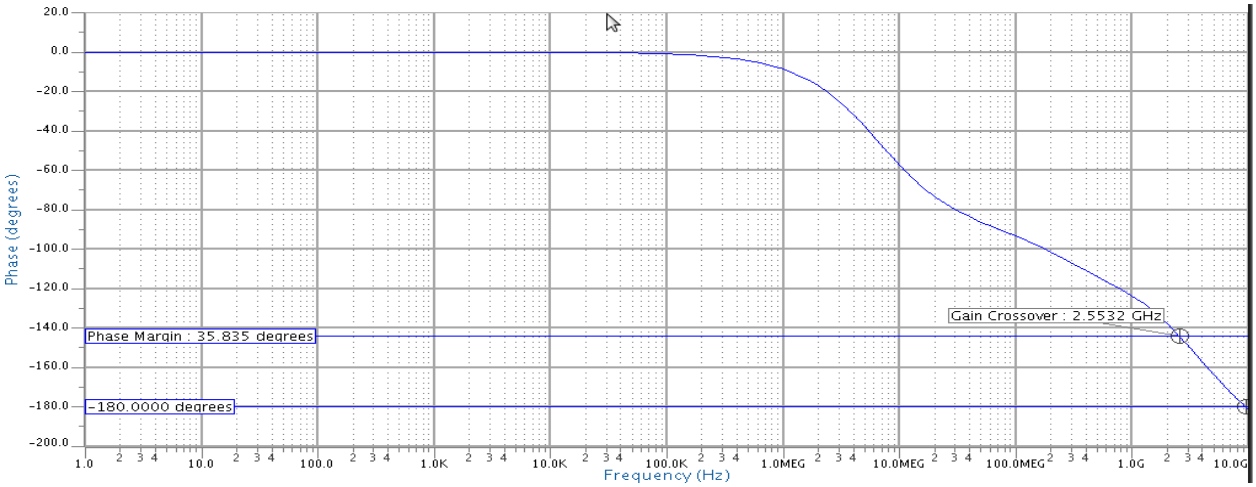

Figure 3.Phase response of folded cascode operational amplifier.

The operational amplifier characteristics found in literature survey and of this work are tabulated as below. Table1 shows that the designed folded cascode operational amplifier has the high unity gain frequency response than other folded cascode operational amplifiers found in literature.

Table 1.Op Amp characteristics found in literature and of this work

	[1]	[2]	[3]	[4]	This work
Node[µm]	1.6	0.18	0.18	1.2	0.13
V_{DD}[v]	±5	±1.5	±1.8	±1.5	±1.8
A_{dc}[dB]	90	80	54	50	58
f_t[GHz]	0.116	0.66	0.134	1	2.55
PM[^{0}]	64	73	70.6	55	35

V.CONCLUSION

In this paper, a folded cascode operational amplifier for high frequency applications is designed. The design procedure is explained in detail. The operational amplifier thus designed is simulated in IC station, mentor graphics tool at standard 130nm technology process. The simulation results show that the folded cascode operational amplifier designed has an open-loop gain of 58dB and unity gain frequency of 2.5GHz.

VI.REFERENCES

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