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DESIGN OF A LOW POWER HIGH SPEED DYNAMIC DOUBLE-TAIL COMPARATOR

G. Suresh[1], V. Siva Reddy[2]

[1]*ECE, VR Siddhartha engineering college*
[2]*ECE, VR Siddhartha engineering college*

Abstract –*Comparator is a major building block of analog to digital converter (ADC) since speed of ADC is determined by the comparator.The need for ultra-low-power, area efficient and high speed analog-to-digital converters is pushing toward the use of dynamic regenerative comparators to improve speed and efficiency of power.In this discuss on high speed, low-power & low-voltage consumption comparators such as dynamic comparator,dynamic double-tail comparator and modified double tail comparators are studied. Based on results a new double tail comparator is proposed and compared to dynamic comparator, dynamic double-tail comparator and modified double-tail comparator in terms of delay and power. So that power consumption and delay time are significantly reduced even in small supply voltage. The simulation results will be shown in Mentor Graphics 130nm technology.*

Keywords- *Double tail Comparator, latching delay, dynamic clocked comparator, analog to digital converter, low-power analog design.*

I. INTRODUCTION

In low power applications such as analog to digital converters (ADCs), comparator is one of the basic building blocks. ADCs with high speed such as successive approximation ADCs, requires high speed and low power consumption comparators with reduced area [1].

In order to convert a small input referred voltage to a full scale level with in a short period of time, these comparators uses positive feedback mechanism with a two back to back cross coupled inverters i.e. .latches [2]. But inverter latch offset voltage, which results from mismatches like threshold voltage (Vth) and oxide capacitance (Cox) variations occurs in the regenerative latch deteriorates the accuracy of such comparator for which body driven technique is adopted [3], it removes the threshold voltage requirement. If outsized devices are preferred in latching stage, the reduction of speed and a low offset voltage can be achieved due to decrease in the regeneration time and the high power dissipation [4]. The pre-amplifier dynamic comparator can amplify minimum input latch offset voltage. Due to the scaling of technology and continuous time the pre-amplifier based dynamic comparators suffer from high power consumption.

Clocked comparators can make fast decisions as they have strong positive feedback in the regenerative latch. There are many analyses such as noise, offset [5]; random decision errors and kick back noise [6] are present. In this, an analysis of existing clocked regenerative comparators such as conventional dynamic comparator [7][8], double tail comparator[9] and modified double tail comparator[10] is analyzed practically. Based on the results obtained a new dynamic double-tail comparator is proposed which improves the performance over existing comparators. This proposed comparator is designed by adding the Domino logic block to the modified double tail comparator [11][12]. Delay and Powers of proposed double-tail comparator is less compared to dynamic comparator, dynamic double-tail comparator and modified double-tail comparator.

II. CLOCKED REGENERATIVE COMPARATORS

Clocked regenerative comparator have found wide application in many high-speed ADCs since they can make fast decision due to the strong positive feedback in the regenerative latch

- Conventional Dynamic comparator
- Conventional Dynamic double-tail comparator
- Modified Dynamic double –tail comparator

A. CONVENTIONAL DYNAMIC COMPARATOR

Conventional dynamic comparator is widely used in A/D converters. The comparator has high input impedance, rail to-rail output swing, and has no static power consumption. It has two phases

- Reset phase
- Comparison phase

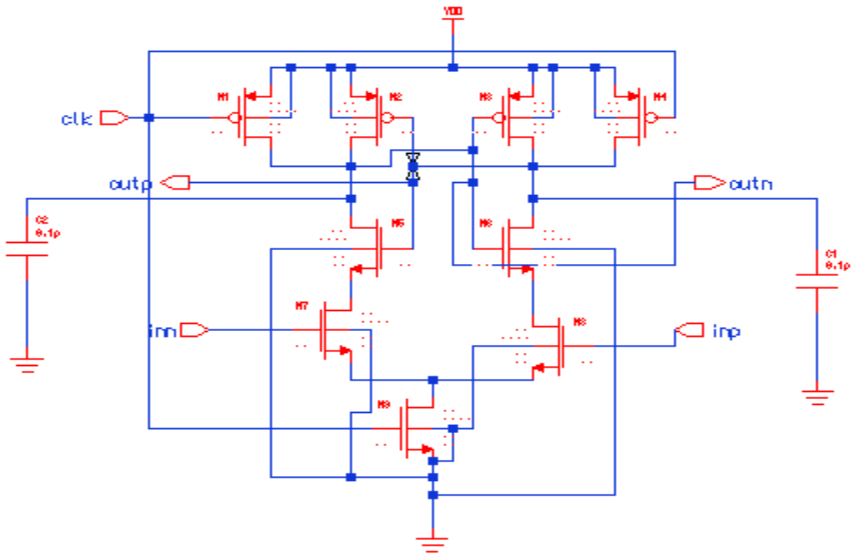

Fig 1: Schematic diagram of the conventional dynamic comparator

The operation of the conventional dynamic comparator is explained below. During the reset phase , when CLK=0 and Mtail is off , the reset transistor M5 and M8 pull both the output nodes Outn and Outp to VDD to define a start condition and to have a valid logical level during the reset. In the comparison phase, when CLK =VDD, transistors M5, M8 are off and Mtail is on. Output nodes (Outp, Outn) which had been pre-charged to VDD, start to discharge at different discharging rates depending on the input voltages (VINP,VINN).Assuming the case where VINP > VINN, the output node Outp discharges faster than Outn, hence with Outp (discharged by transistor M2 drain current), falling down to VDD–|Vthp| before Outn (discharged by transistor M1 drain current), the corresponding PMOS transistor (M6) will turn on to initiate the latch regeneration caused by back-to-back inverters (M3-M6 and M4-M7). Thus, the output node Outn pulls to VDD and Outp discharges to ground. If the input voltage VINP is less than VINN, the circuit works vice versa.

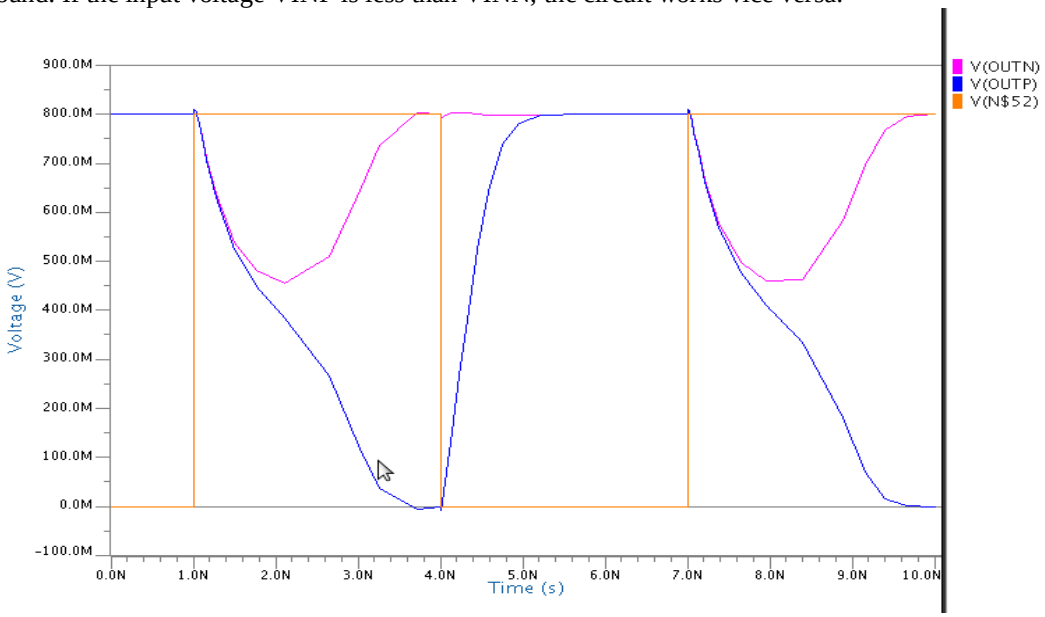

Fig 2: Transient simulation of conventional dynamic comparator

Due to high input impedance, high speed, full output swing output and less power consumption can be seen, the dynamic comparator exhibits excellent benefits for many low power applications such as sense amplifiers, data receivers and Analog to Digital Converters (ADCs).

B. CONVENTIONAL DOUBLE-TAIL COMPARATOR

This structure has less stacking and therefore can operate at lower supply voltages compared to the conventional dynamic comparator. The double tail enables both a large current in the latching stage and wider Mtail2, for fast latching independent of the input common-mode voltage (Vcm), and a small current in the input stage (small Mtail1), for low offset. It has two phases

- Reset phases
- Decision–making phases

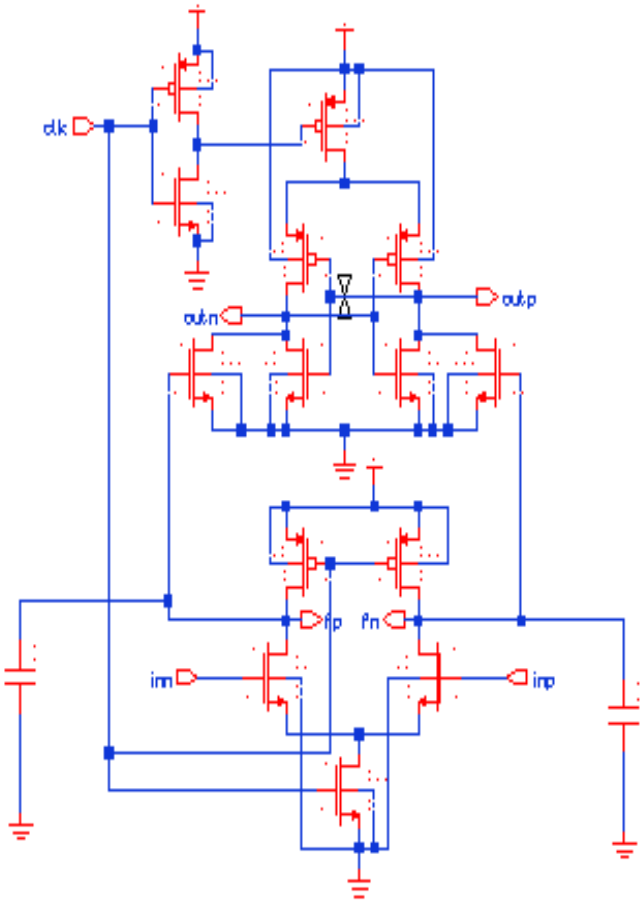

Fig 3: Schematic diagram of convectional double–tail comparator

During the reset phase (CLK = 0, Mtail1 and Mtail2 areoff), transistors M3,M4 pre-charge the nodes fn and fp to VDD, which in turn make MR1 and MR2 to discharge the output nodes Outn and Outp to the ground. During decision making phase (CLK=VDD, Mtail1 and Mtail2 turn on), the transistors M3,M4 turn off and the voltages at nodes fn, fp start to drop with the rate defined by IMtail1/Cfn(p) and an input-dependent differential voltage ΔVfn(p) will also build up. The intermediate stage formed by the transistors MR1 and MR2 passes ΔVfn(p) to the cross coupled inverters and provides a good shielding between to input and output to get a reduced value of kickback noise.

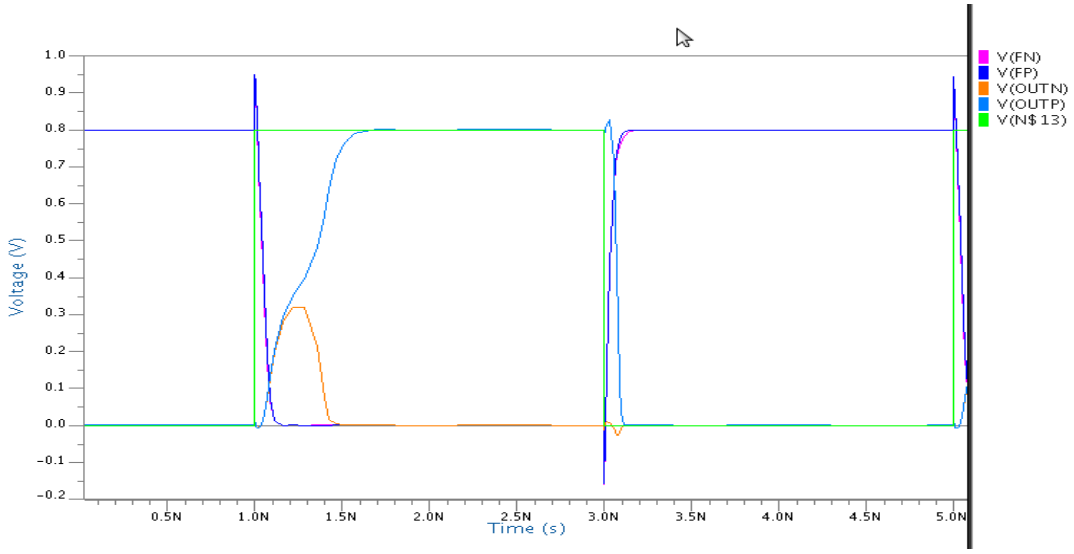

Fig 4: Transient simulation of convectional dynamic double-tail comparator

C. MODIFIED DOUBLE-TAIL COMPARATOR

Fig.5 shows the schematic diagram of the modified double tail comparator. The modified double tail comparator is designed based on the double tail architecture.

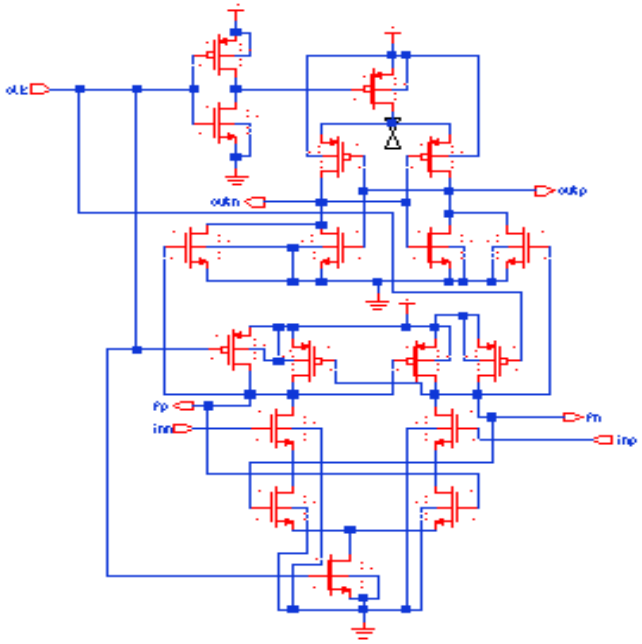

Fig 5:Schematic diagram ofModified double- tail comparator

The idea of this comparator is to increase ΔVfn/fp in order to increase the latch regeneration speed. For this purpose, Mc1 and Mc2 are the two control transistors that have been added to the first stage in parallel to M3/M4 transistors but in a cross-coupled manner.

The operation of the modified double tail comparator is as follows. During reset phase (CLK = 0, Mtail1 and Mtail2 are off, avoiding static power), M3 and M4 pulls both fn and fp nodes to VDD, hence transistor Mc1 and Mc2 are cut off. Intermediate stage transistors, MR1 and MR2, reset both latch outputs to ground.

During decision-making phase (CLK = VDD, Mtail1, and Mtail2 are on), transistors M3 and M4 turn off. Furthermore, at the beginning of this phase, the control transistors are still off (since fn and fp are about VDD). Thus, fn and fp start to drop with different rates according to the input voltages. Suppose VINP > VINN, thus fn drops faster than fp, (since M2 provides more current than M1). As long as fn continues falling, the corresponding PMOS control transistor (Mc1 in this case) starts to turn on, pulling fp node back to the VDD; so another control transistor (Mc2) remains off, allowing fn to

be discharged completely. In other words, unlike conventional double-tail dynamic comparator, in which ΔVfn/fp is just a function of input transistor trans conductance and input voltage difference, in the existing double tail structure as soon as the comparator detects that for instance node fn discharges faster, a PMOS transistor (Mc1) turns on, pulling the other node fp back to the VDD. Therefore by the time passing, the difference between fn and fp (ΔVfn/fp) increases in an exponential manner, leading to the reduction of latch regeneration time.

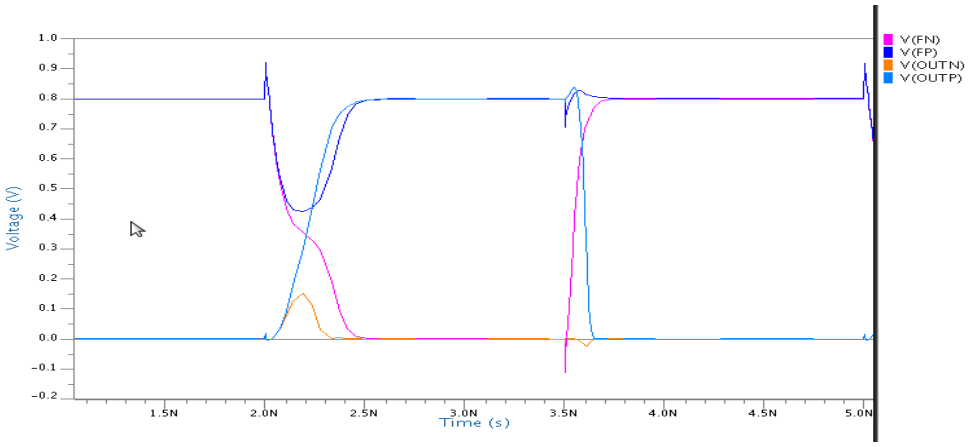

Fig 6: Transient simulation of modified double-tail comparator

III. PROPOSED DOUBLE-TAIL COMPARATOR

The schematic circuit of proposed dynamic double tail comparator is given in Figure7. This schematic circuit is an extension of double tail comparator. At the output side, dynamic/domino logic is included.

Here the outn is given to the one input and outp is given as another input to the dynamic/domino logic circuit. Considering in inverted form and given as input to next stage input. The output of first stage and second stage are considered as out1,out2 respectively.

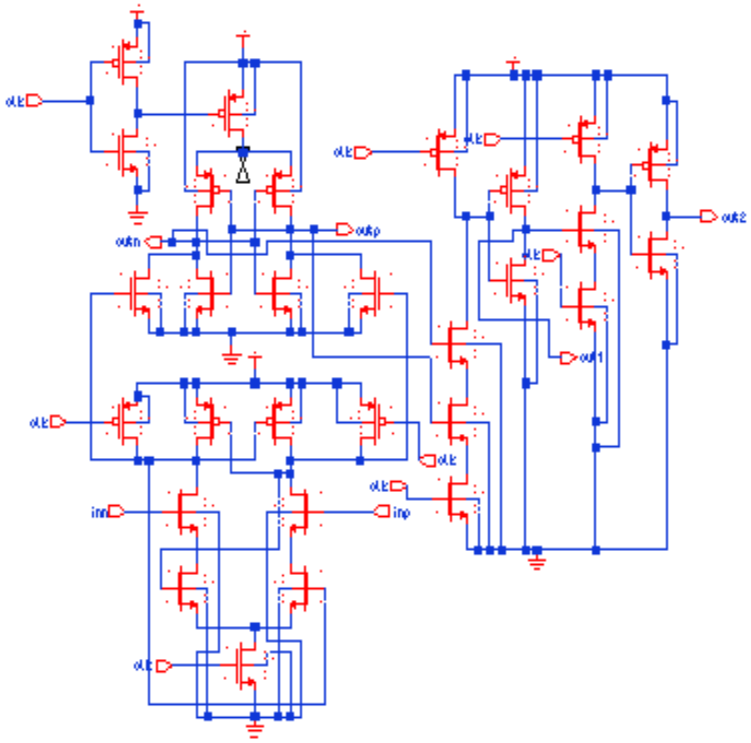

Fig 7:Schematic diagram of proposed double tail comparator

The operation of this proposed circuit is similar to the modified Dynamic double tail comparator. The operation consists of two phases

- Reset phases
- Decision–making phases

When CLK=0, the comparator is operated in Reset phase and CLK=VDD the comparator is in Decision-making phase.

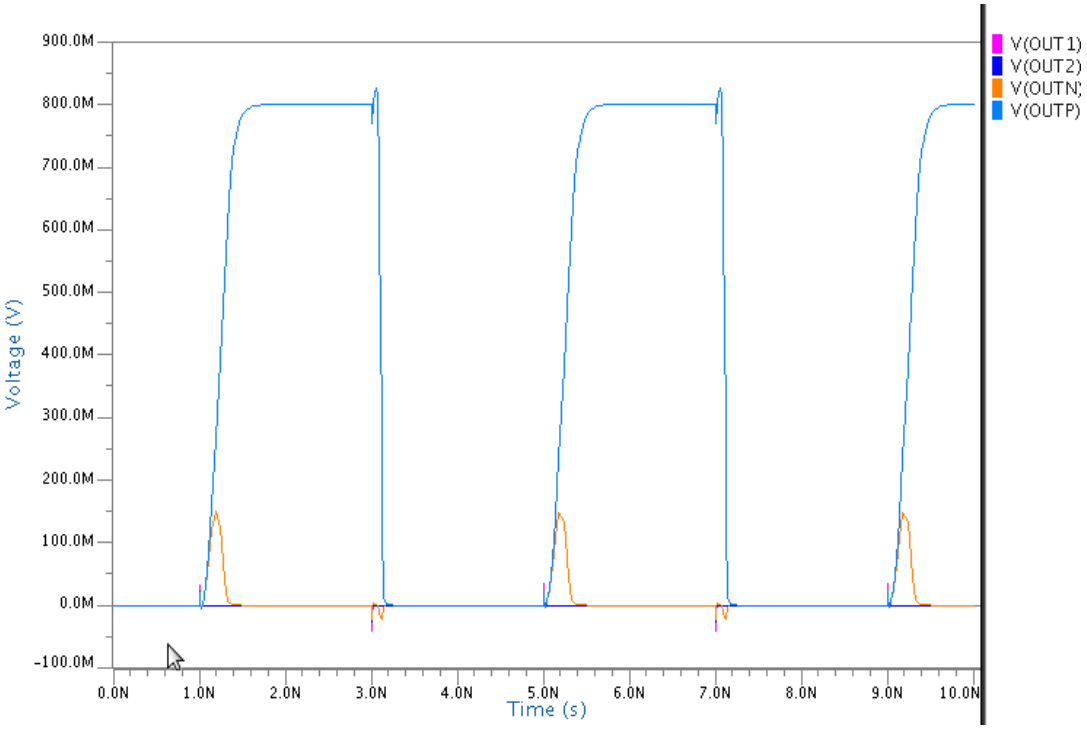

Fig 8: Transient simulation of proposed double-tail comparator

IV. PERFORMANCE COMPARISON

The performance comparison given in table I show the average power dissipation and delay of all the discussed comparators.

TABLE I
Performance Comparison of Various Comparators

Design	Power (uW)	Delay (ps)
Conventional Dynamic Comparator	18.797	333.69
Conventional double tail comparator	16.055	262.31
Modified double tail comparator	13.813	223.09
Proposed double tail comparator	12.796	214.40

From the table, it is observed that the average power consumption and the delay of the proposed comparator are significantly reduced.

V.CONCLUSION

In this work, a novel double tail comparator is designed and simulated using 130nm CMOS technology. From the simulated results it is observed that the delay of the proposed double tail comparator is comparatively less than the earlier comparators. Also the average power consumption of the proposed double tail comparator is less than the earlier comparators. Hence the proposed double-tail dynamic comparator can be used for the design of high speed low power ADCs as the delay and power are reduced and hence resulting in faster operation.

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