0.18μm CMOS Current feedback Amplifier using Negative Current Conveyor

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Abstract - The paper describe a new design for low-voltage CMOS current feedback amplifiers (CFAs). This unconventionally implemented CFA exhibits near gain independent bandwidth. An important feature of the design is that the input resistance looking into the X terminal of the current conveyor is reduced by using an extra opamp. This new architecture results in an amplifier whose bandwidth is potentially constant unlike that of conventional design. Complete analysis and simulation results confirm the design topology. The CFOA operates at supply voltages of ±1.8 V. The circuit exhibits a bandwidth better than 10 MHz. Eldo mentor graphics simulation results using 0.18 µm CMOS technology parameters for the proposed CFOA and its application are discussed.

Keywords: CFA,CC,CCII+,CCII-,CFOA

I. INTRODUCTION

Current mode operation of analog circuits has shown to result in faster and improved performance compared to their voltage mode counterparts. Current Feedback Amplifiers (CFAs) using current mode operation have proved to be quite useful in analog and mixed-signal IC applications because of their higher potential bandwidth and higher slew rate than commonly used voltage feedback amplifiers . This mode of operation results in CFAs whose closed-loop bandwidth is almost independent of the closed-loop gain. CFAs are generally built by cascading a positive current conveyor (CC) with a buffer. The work in introduced a new CFA design topology that employed a second generation positive current conveyor (CCII+) followed by an opamp, and the design could attain amplification, as well as, attenuation of the input signal. It showed that the bandwidth of the CFA was totally controlled by that of the opamp that follows the current conveyor. This paper discusses a modification of the design topology in order for the CFA to be consistent with the regular amplifier gain expressions, by replacing the CCII+ in by a CCII-. Further improvement is made by using an extra opamp in front of the CCII- to reduce the impedance looking into the X terminal of CCII-. The sections that follow describe the design procedures, circuit analysis and simulations results.

II. DESIGN TOPOLOGY

The conventional and the proposed design topologies are shown in Figures 1(a) and 1(b), respectively. Note that Cz. and Rz are the internal capacitance and resistance at the Z node of the CCII, respectively. The design in Figure l(b) was originally proposed by , however, using a CCII+. The distinction between Figures 1(a) and 1(b) lies in the input and the final stages. Figure

l(a) employs a buffer in the output stage. Figure l(c) is an extension of the design in Figure l(b), which incorporates an extra opamp to reduce the input resistance at X node of the current conveyor. Unlike the conventional CFA design, which has a bandwidth setting feedback resistor around the entire CFA, the proposed topology uses an opamp instead of buffer and negative feedback is provided only across the opamp Al.
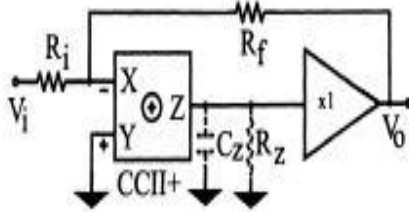
Figure 1 (a): Conventional CFA
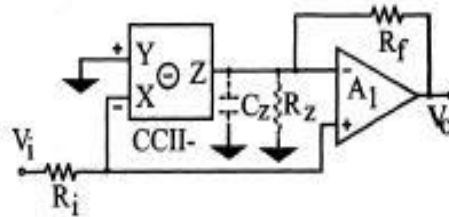
Figure 1 (b): Proposed CFA
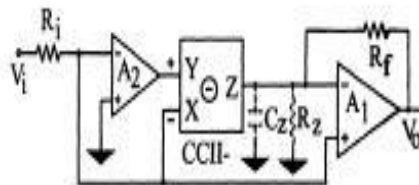
Figure 1 (c): Proposed CFA with additional amplifier

III CIRCUIT DESCRIPTION

A transistor level diagram of the proposed CMOS CFA is shown in Figure 2. It uses a conventional op-amp with a class AB output stage to make the CCII-. The corresponding transistor geometries are provided in Table I. In Figure 3 transistors M25-M33 form the first op-amp Al, M10-M24 the CCII- and MI-M9 the second op-amp section A2.

The proposed CMOS current feedback operational amplifier is shown in fig 2. The performance of the proposed CFOA circuit was verified by performing Eldo mentor graphics simulations with supply voltages ±1.8 V using 0.18 µm CMOS technology parameters and transistor aspect ratios given in Table 1. using 0.18 µm CMOS technology parameters and transistor aspect ratios given in Table 1.

 The calculated (W/L) values of the transistors are given in the table below.

| CMOS	W(um)	L(um)
M1,M2,M12,M13	35	0.18
M3,M4,M10,M11, M27,M28,M33	14	0.18
M5,M9,M14,M18,M20, M22,M24	7	0.18
M6,M15,M30	11.75	0.18
M7,M16,M31	3.5	0.18
M8,M17,M19,M21, M23	21	0.18
M25,M26	6.3	0.18
M29	5.25	0.18
M32	22.75	0.18

Table 1 (W/L) values of the circuit.

IV   SIMULATION RESULTS

To confirm the validity of the design, the circuit of Figure 2 was implemented and simulated using Eldo mentor graphics 0.18 um CMOS technology in a single-ended supply voltage of 1.8 V. The bias voltage Vb was set at 700 mV. The values of the compensation capacitors Cc1, and Cc2, Cc3 and CL were set at 25 pF, 10 pF, 18 pF and 8 pF, respectively. The feedback resistor Rf was set at 1 kΩ.

In order to verify the gain-independency of the bandwidth, the circuit of Figure 3 was configured as a non-inverting voltage amplifier and the frequency response was simulated. Figure 4 shows that the closed loop bandwidth approximately remains constant at 10MHz
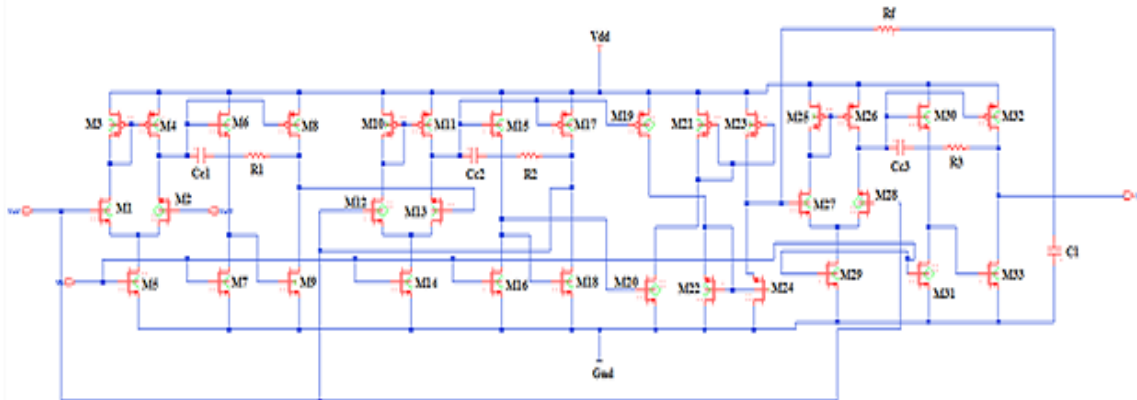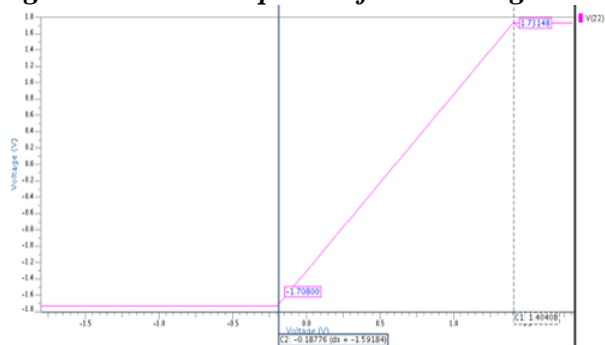

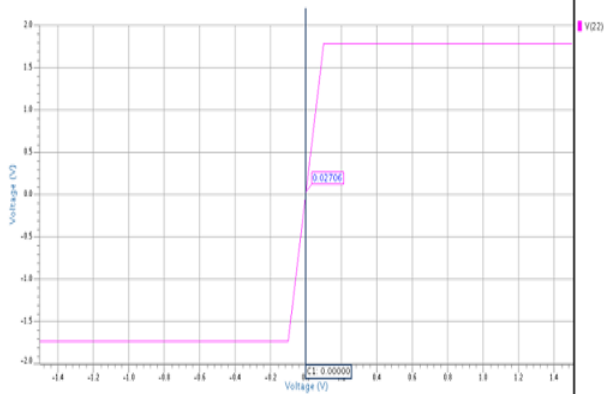*Figure 2: Proposed CMOS CFA using negative current conveyor.*
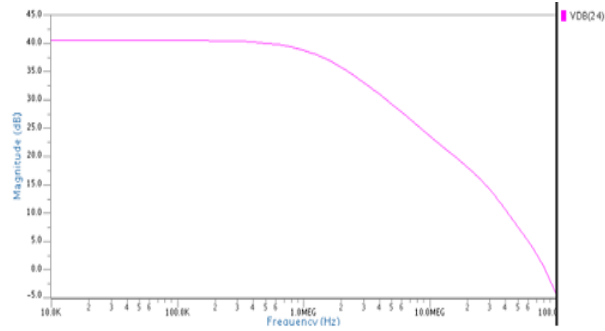
Figure 3: Magnitude response of CFA using CCII-.
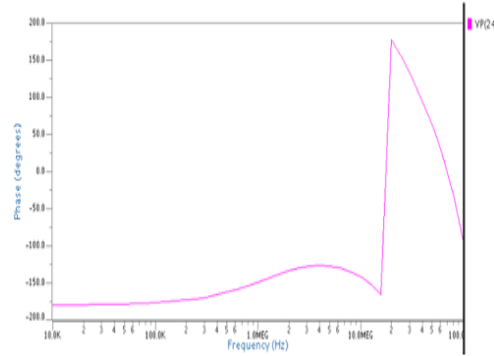
Figure 4 : Phase response of CFA using CCII-.

Figure 5 : ICMR measurement of CFA using CCII-.
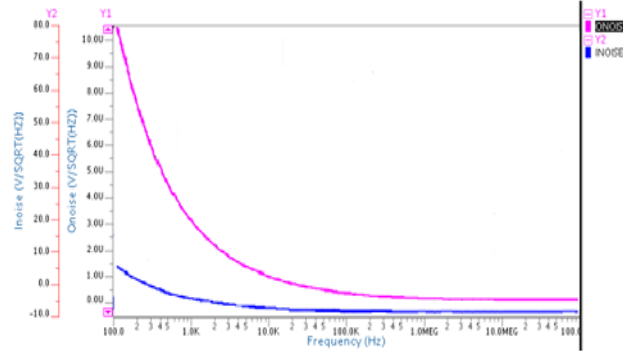

Figure 6 : Offset analysis of CFA using CCII-.

Figure 7 : Noise response of CFA using CCII-.

In this design, 0.18um CMOS technology is used with supply voltage of 1.8 V. The CFOA shows a constant bandwidth for different gains. The CFOA has a 3 dB bandwidth of MHz and a phase margin of 54. The input and output referred noise spectral densities shown in Fig.6 are less than 30 µV/Hz.

IV.   CONCLUSION

A novel design of CMOS current feedback amplifier has been presented. This approach removes the gain dependency of bandwidth and the closed loop gain can be adjusted with a higher precision. Unlike the conventional CFA, finite value of r, practically has no effect on the bandwidth. Simulation results confirm the validity of the design.

Table 2 Performance analysis of proposed CFOA.

Technology	0.18µm CMOS Technology
Supply Voltage (Vdd) Gain	1.8 v 41 db
CFA Bandwidth Slew Rate	10 MHZ 11 V/us
Phase Margins	54 degree
Power dissipation	2.5 mW

V. REFERENCES

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