Scientific Journal of Impact Factor (SJIF): 4.14

e-ISSN (O): 2348-4470
p-ISSN (P): 2348-6406

International Journal of Advance Engineering and Research Development

Volume 3, Issue 5, May -2016

Implementation of 11-Level Inverter with Reducing Number of Switches

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Abstract:- This paper gives implementation of new topology of single-phase8-switch 11-levelmultilevel inverter. The topology is being switched with the use of SPWM control technique which generates the stepped waveform for both output voltage and output current. The SPWM technique reduces the harmonics in output current. Detailed THD analysis is being given in the paper.

Keywords:- Multilevel Inverter;SPWM; Simulation And THD Analysis.

I. INTRODUCTION

In an electric power system DC voltage comes from any energy sources like wind energy, solar energy, hydro energy etc. [2]. So, that energy comes in DC voltage or DC power, then in power system require one type of converter, which converts in a voltage or power. Here this system has required inverter for converting DC to AC voltage.

Alternating staircase waveforms with higher harmonics produce from conventional bipolar inverter [5]. Thus the multilevel inverters (MLI) are developed. Here this multilevel inverters are different from conventional two level or three level inverter. Here this type inverter is less harmonics produce and switching stress for high power application is also reduced from basic inverter [1].

Here in this paper gives comparative study for three basic topology like a diode clamped MLI, capacitor clamped MLI, cascaded H-bridge type MLI and also new topology for 11-level inverter.

Here for this type inverter control from various types of control strategies like sinusoidal pulse width modulation (SPWM), selective harmonic elimination technique and space vector pulse width modulation (SVPWM)[6].

Here for basic topology 11-level MLI used components like in diode clamped MLI require 20 switches, 90 diodes and 10 main DC-bus capacitors per phase, which is produce a staircase as the output voltage wave form, in capacitor clamped MLI require 20 switches, 45 clamping capacitors and 10 main DC-bus capacitors per phase, and cascaded H-bridge inverter require only 24 switches per phase for produce the output wave form [5].

Now here this paper is describing the new topology for 11-level MLI, here this topology is used with only 8 switches. So, this type topology is used, then cost of the inverter is less from switch side, and also stress on the switch is less produce. So this type MLI is efficient for power system or in conversion side like from DC to AC conversion. Here if we want or use for three phase system, there is connection is required in star or delta connection, in which three single phase MLI required and which is connected 120 degree phase angle apart from each single phase MLI.

This paper organized in many sections, in section II introduced to new topology and its circuit diagram and its switching table for the operation of which switch is were conduct. And in section III, which control strategy is used in this new model. And in section IV gives simulation and its total harmonic analysis, then in section V gives the conclusion..

II. NEW TOPOLOGY OF MULTILEVEL INVERTER

The new topology of multilevel inverter is shown in fig. 1. There 8 switches are used for 11-level generated in output voltage. Here three sources are used for different levels, there in which one source is half from both other sources, here also connection of these sources polarities is in the opposite direction to each other sources. Shown in fig. 1 their connection of three sources [5].

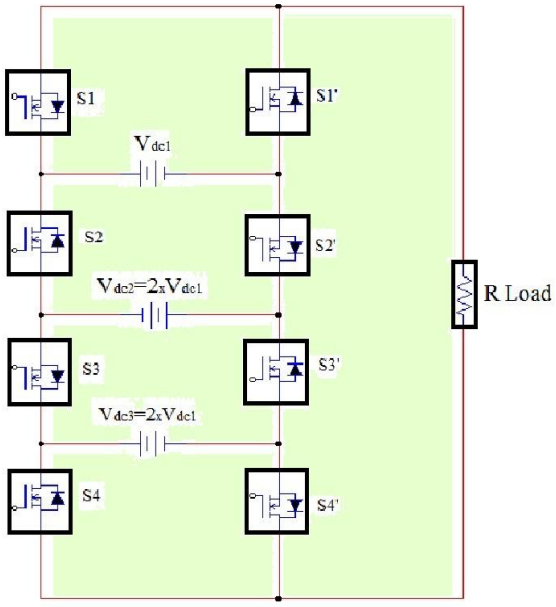

Fig.1. Diagram of new topology 11-level MLI.

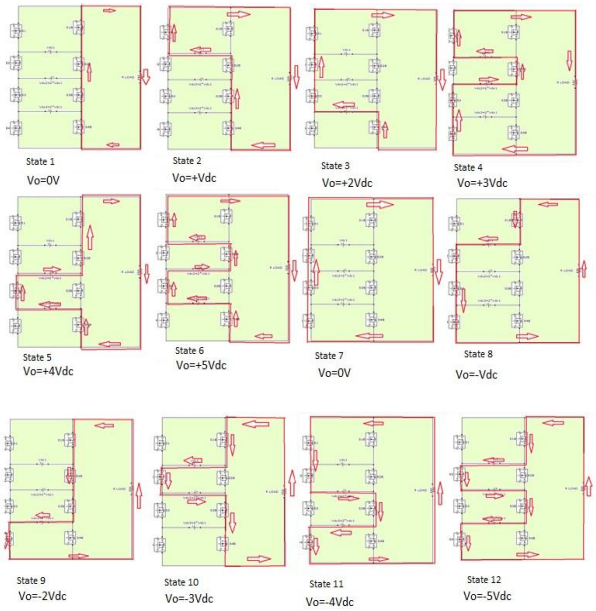

Fig.2. Operation of each state of new topology singlephase11-level MLI.

Here shown in fig.1. Which is describe single phase circuit configuration for any loads like inductive, capacitive and resistive, here in this fig.1 Resistive load is connected. In this new topology 8 switches are used for each different level [5].

Here for conduction of switches, switching states is shown in table1. These switches states are apply in SPWM technique in MATLAB simulation for the generating gate pulses.

TABLE.1
SWITCHING STATES IN 11-LEVEL INVERTER

Output Voltage	**S 1**	**S2**	**S3**	**S4**	**S1'**	**S2'**	**S3'**	**S4'**
+5vdc	1	0	1	0	0	1	0	1
+4vdc	0	0	1	0	1	1	0	1
+3vdc	1	0	1	1	0	1	0	0
+2vdc	1	1	1	0	0	0	0	1
+vdc	1	0	0	0	0	1	1	1
0	0	0	0	0	1	1	1	1
-vdc	0	1	1	1	1	0	0	0
-2vdc	0	0	0	1	1	1	1	0
-3vdc	0	1	0	0	1	0	1	1
-4vdc	1	1	0	1	0	0	1	0
-5vdc	0	1	0	1	1	0	1	0

Shown in fig.2 which is given an understanding of operation for each state. Here for each level four switches are operating simultaneously. Also here S1', S2', S3'and S4' switches operating states for each level is inverse from S1, S2, S3 and S4 switches [5]. Shown in table 1.

III. VARIOUS TYPES OF SPWM CONTROL STRATEGY

In recent topologies of multi level inverter basically three types of control strategy are used like selective harmonic elimination technique, SVPWM and SPWM. Here in which selective harmonic elimination technique is used only for fundamental switching frequency, which is not applied to this type topology of 11 level inverter. Then SVPWM is used for both fundamental and high switching frequency, and which is known for better accuracy.

Here SVPWM technique is used for high level of MLI, but only in software analysis, which is not applicable for the level in for SVPWM technique, which is not applied more than 5level because, more than 5level programming for hardware is very tough. So, here SPWM technique is the use for high frequency, and which is easy to control for high level MLI [8]. Here in this paper SPWM technique is used.

There different types of SPWM methods are available like (A) Phase Disposition PWM (PDPWM), (B) Phase Opposition Disposition PWM (PODPWM), (C) Alternative Opposition And Disposition PWM (APODPWM), (D) Phase Shift PWM (PSPWM), (E) Carrier Overlapping PWM (COPWM) and (F) Multi Carrier Sinusoidal Pulse Width Modulation with Variable Frequency (MCSPWMVF).these techniques are generally used for generating gate pulse for switches. Here in this paper new SPWM generic strategy is used for this type MLI [10].

A. PWM Phase Disposition (PD):

Here in this SPWM technique all the carrier signals are require as same frequency, same amplitude and in phase, but which at different DC offset for different different levels, it compared with a single reference sine wave signal. So, here intersection points of the reference sine signal with the respective carrier signals are the points, then gate pulses are generated for each switches and also for each level. Thus, all carrier signals are selected with the same phase, this method is known as PD. Thi method is completely shown in the Fig.3. In which the number of carrier signals required are as (n-1) where n = number of levels [10].

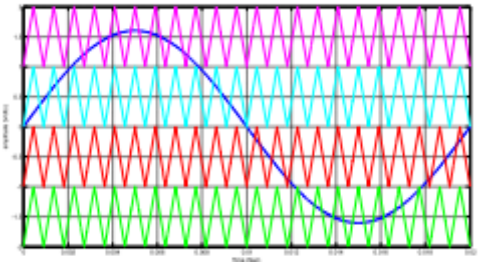

Fig. 3. PWM Phase Disposition [10]

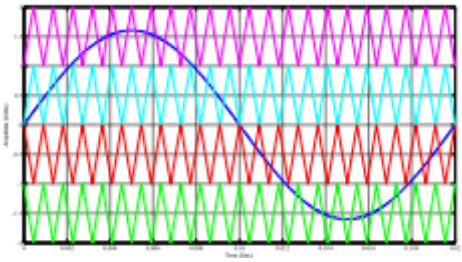

Fig. 4. PWM Phase Opposition Disposition [10]

B. PWM Phase Opposition Disposition (POD):

This method described for positive and negative carriers both are in opposite phase at 180 degrees, and another making of carrier signals for different level is same as PD technique, also same as with the same frequency, amplitude.This method is shown in the Fig. 4.

C. PWM Alternative Phase Opposition Disposition(APOD):

This method also described trianguler signals with the same amplitude and same frequency, here but all carrier wave are appart from 180 degrees out of phase with reaspect adjacent one, this method is shown in the Fig. 5.

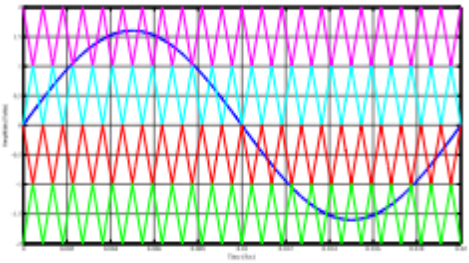

Fig. 5. PWM Technique APOD [10]

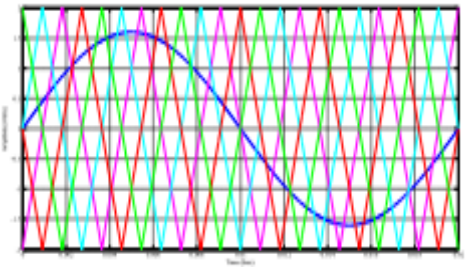

Fig. 6. PWM Phase Shift technique [10]

D. PWM Phase Shift:

Here in which technique all triangular wave have the same frequency and the same ampletude, and here only difference is which is DC offset, and they are phase shifted to each other by 90 degrees, shown in fig. 6.

E. PWM Carrier Overlapping:

This type technique show level shifted trianguler signals of the same ampletude and sane frequency. These all are in phase with respective each other and also overlapping to each other. This type technique and its configuration is shown in fig.7.

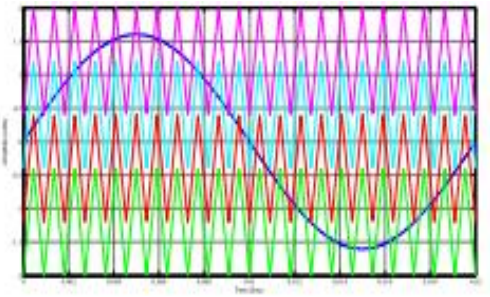

Fig. 7. PWM Carrier Overlapping Technique [10]

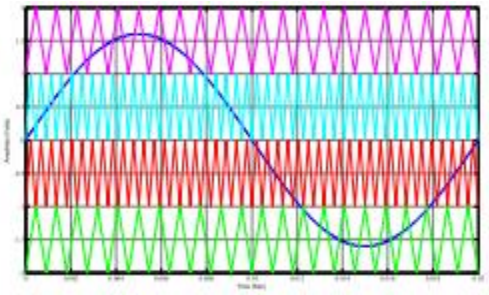

Fig. 8. Variable Frequency PWM Technique [10]

F. Variable Frequency PWM:

In this technique all the level- shifted triangular signles are in same amplitude. Here lowest triangular signal has a very large frequency, 10khz and then upped from lowermost carrier has 8khz, and then step by step adjusted from 6khz, 4khz and the toprmost triangle signal has lower frequency, 2khz. These signsls are compairing with the one reference sine signal with fundamental frequency for produce require gate pulses is shown in fig.8.

G. New Control Technique Of SPWM:

In this new technique, only one parent carrier signal is used for every gate pulse and also one reference sin signal is used for the according to that signal illustrated in fig. 9., and then the trainable pulses are goes into the desired switches at some time intervals for each level and using logic combinations is shown in fig. 10. – fig. 12. Fig. 10. See the confiuration of generation of the parent signal of SPWM techniquie, fig. 11. And fig. 12. See the pulse steering logic configuration to make gating signals for a desired switch. Now in which technique is not defined with time interval, then created gate signal is ANDing with respective to time steering, then generating final gate pulses with defined time value.

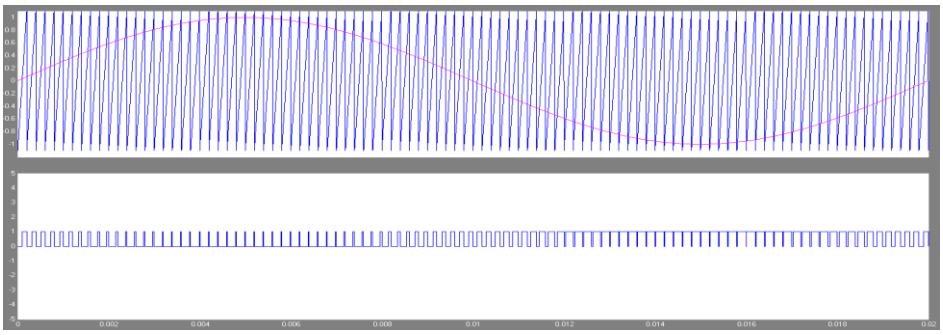

Fig. 9. One Carrier Parent Signal [10]

This new technique use only one sine and one carrier signal and is generic in system. Thus this type method is used in any simulation of power electronic, also which is make any parent signals are generated with the time periode for which switches are operated at which time [10]. Here this types of technique is used in this new topology of 11Level MLI.

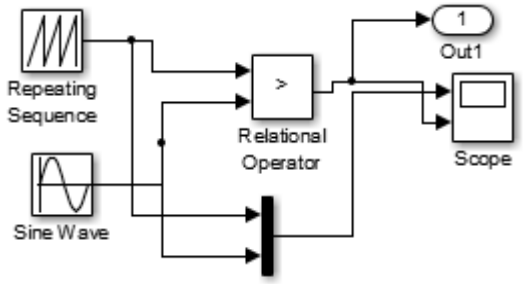

Fig. 10. Generation Of Parent Signal In MATLAB [10]

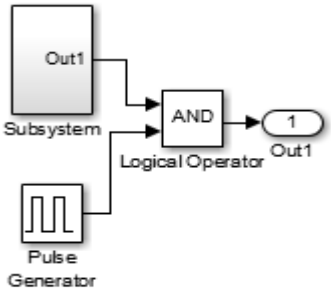

Fig. 11. Generation of with time Defined signal in MATLAB [10]

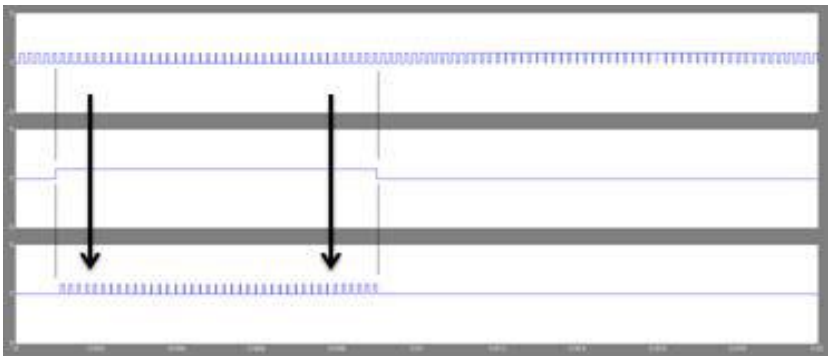

Fig. 12. Illustration Of Pulse Steering [10]

IV. SIMULATION RESULTS AND THD ANALYSIS

Here this type new topology is simulated in MATLAB, here in this simulation topology 8 switches are used and also 3sources are used in shown in fig. 13. Here in this simulation source is one of them 100Vdc and two 200Vdc.This simulations is an open loop simulation and load is connected like resistive and inductive both are connected in series.In this simulation resistive load is 50ohm and inductive is 1mH for single phase configuration.

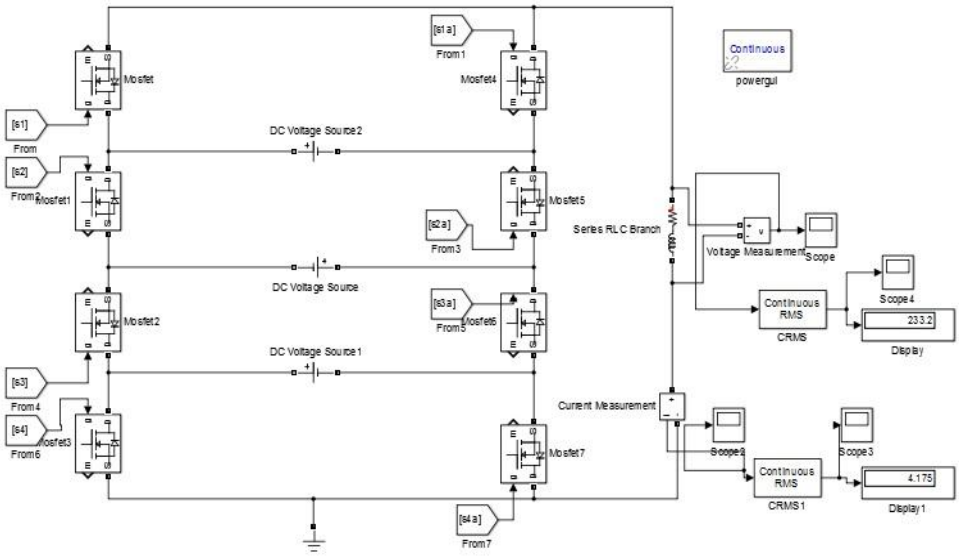

Fig.13. Simulation of new topology single phase11-level MLI.

This simulation is controlled by new control techniques of SPWM. Here in this control strategy one reference sin signal is used, which is fundamental frequency is 50Hz.then this fundamental frequency is compared with one parent signal is shown in fig.9. Here in this control strategy gate pulses is produced by pulse generator for each pulse. Here 2.5kHz switching frequency applied by one parent carrier signal. Here amplitude modulation index ma=1 and frequency modulation index mf=50 used. So, that output voltage and current waveforms are shown in fig.14 and fig.15.

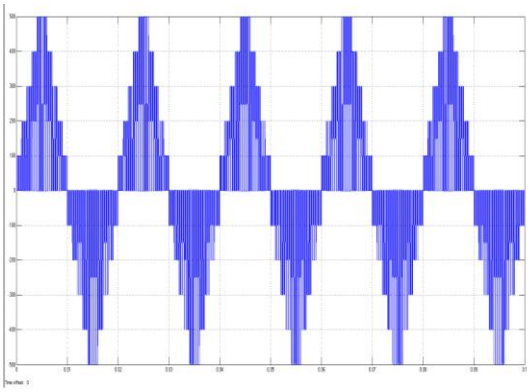

Fig.14. Output Voltage Waveform Of 11level MLI With RL Load

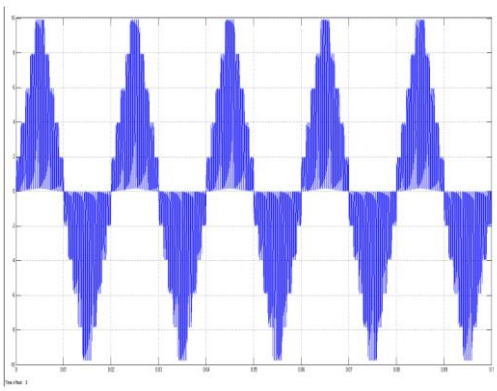

Fig.15. Output CurrentWaveform of 11level MLI With RL Load

The total harmonic distortion for a single phase single 11 level inverter, using the Fast Fourier Transform (FFT) analysis which coming from a powergui block in MATLAB simulation. Here FFT analysis for total harmonic distortion (THD) of output voltage and current waveforms are shown in fig.16 and fig.17.

Here for FFT analysis taken 1khz frequency, and signal considered for 5cycle for better observation. So total harmonic distortion, produce for voltage waveform is 13.92% and its magnitude is 231.3 at fundamental frequency 50Hz. And also for current waveform THD is measured like 13.89% and magnitude of the current is 4.625 at the fundamental frequency.

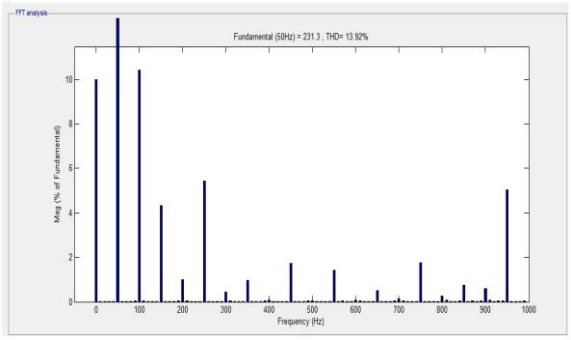

Fig.16. FFT Analysis Of Output Voltage Waveform Of 11level MLI.

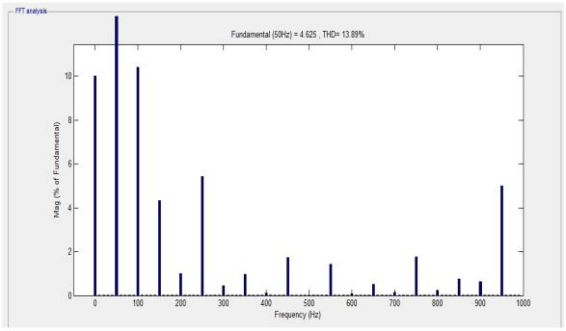

Fig.17. FFT Analysis Of Output current Waveform Of 11level MLI.

Here for FFT analysis taken 1khz frequency, and signal considered for 5cycle for better observation. So total harmonic distortion, produce for voltage waveform is 13.92% and its magnitude is 231.3 at fundamental frequency 50Hz. And also for current waveform THD is measured like 13.89% and magnitude of the current is 4.625 at the fundamental frequency.

Here in FFT analysis of voltage waveform 3^{rd},5^{th} harmonics are coming high like 4.34% and 5.42% simultaneously, in all of them dominant, 5^{th} harmonic is very affected. And also same for in current analysis 3^{rd},5^{th} harmonics are coming high like 4.33% and 5.41% simultaneously, and also here dominant harmonic is 5^{th} is very affected. Harmonic analysis is shown in fig.16 and fig.17.

V. CONCLUSION

Single phase 11- level inverter topology with number of 8-switches is given and simulated. Given information about which control strategy is better for MLI. New control strategy applies of SPWM.

From the simulation results, it was found the new control strategy provides minimum THD of 13.92 % and 13.89% in the inverter output voltage and current waveform simultaneously. From THD analysis 5^{th} harmonic is the dominant component for both voltage and current waveform, on this type MLI.

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