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3- BIT CURRENT STEERING AND THERMOMETER CODE DAC WITH BATTER INL AND DNL

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Abstract: In this paper analysis of 3-bit Current Steering and Thermometer Code DAC designed with the specification of INL & DNL. The simulation & analysis is done using the binary and thermometer code. In Current Steering DAC Maximum INL & DNL is 0.15 achieved. In Thermometer Code DAC Maximum INL & DNL is 0.05 achieved. The circuit simulation is done using the Eldo Spice in Mentor Graphics Tool with the 180nm CMOS process Technology.

Keywords: CS(Current Steering), DAC(Digital to Analog Converter), INL(Integral Nonlinearity), DNL(Differential Non Linearity).

I. INTRODUCTION

Among the most popular architectures are DACs based on resistor ladders and current steering. These architectures are very well suited for implementation in standard occupied area ,power consumption and speed. In general requiring N-bit DAC resolution implies. DAC method uses current throughout the conversion known as current steering, this type of DAC requires precision current sources that are summed in various fashions. Figure 1 illustrates a generic current steering DAC.

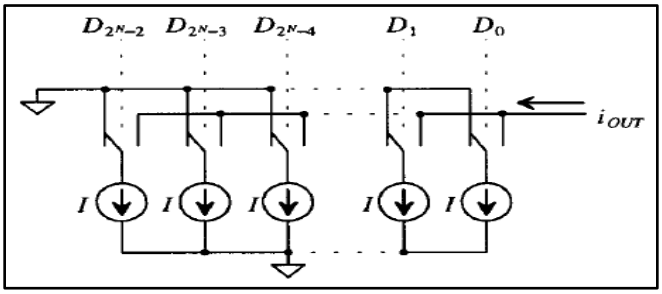

Figure 1: A generic current steering DAC

The remaining of this paper is organized in the following section, a basic concept of R-2R ladder network II. Next a modification of CMOS EQUIVALENT circuit of W-2W Binary-Weight circuit of Current Steering DAC in section III. CMOS EQUIVALENT circuit of Thermometer Code DAC in section IV. In addition, simulated results of the CS and Thermometer Code DAC and conclusion are presented in section V and VI respectively.

II. CMOS EQUIVALENT CIRCUIT OF W-2W BINARY-WEIGHTED CS DAC

The w-2w current mirror is a novel and compact approach of implementing binary-weighted current steering DACs. Figure 2 shows the the implementation of a binary-weighted w-2w current mirror topology.

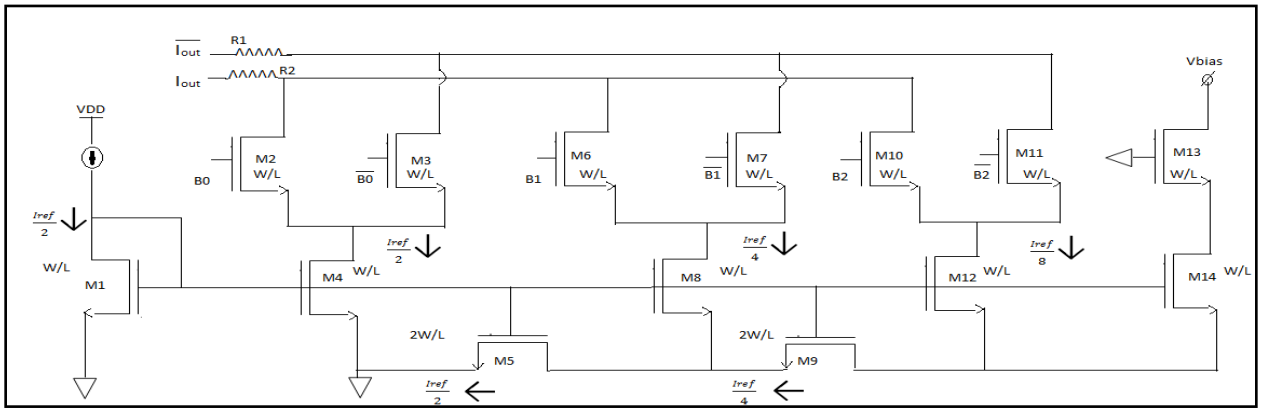

Figure 2: Binary-weighted current mirror, using w-2w topology

It utilizes that fact that when MOSFETs, with the same W/L, are connected in parallel , the result is an equivalent to a device of 2W/L , while in series they are equivalent to a device of size W/2L. for the desired operation of the circuit the current flowing in M1 and M2 should Be the same and equal to the input current. The current in remaining devices should sum up to that value or $I_{REF}/2$ in this case. The advantage of the W-2W topology over a traditional binary-weighted DAC circuit is the significant reduction in layout area for high bit resolution because of fewer number of device employed.

III. CMOS EQUIVALENT CIRCUIT OF THERMOMETER CODE DAC

The thermometer coded DAC architecture utilizes a number of equally weighted elements. Generally, with *N* binary bits, we have $M=2^{N-1}$ thermometer coded bits. Mostly, the encoded DAC shows good monotonicity behavior as well as an improved DNL and INL over the binary architecture. As shown in below figure the Schematic of the Thermometer Code DAC based on CMOS.

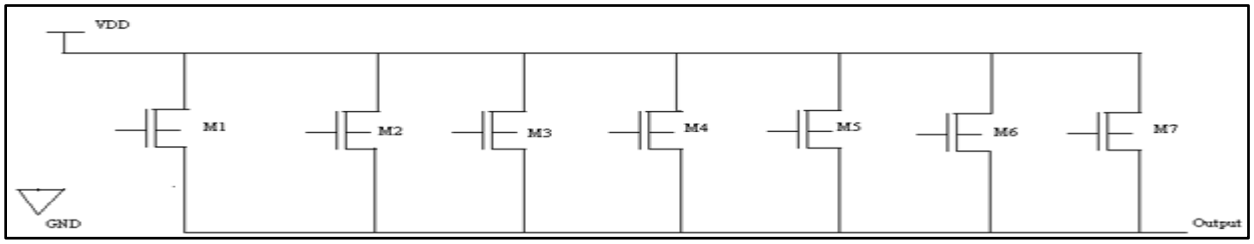

Figure 3: Thermometer Code DAC

IV. SIMULATION RESULTS

Simulation result of 3 bit Binary-weighted Current Steering W-2W DAC in 0.18um CMOS Technology

By applying input volts=2.0v as a pulse and digital input from 000 to 111 for 3 bit I achieved respective voltage and observe respective parameters like INL and DNL Offset, etc

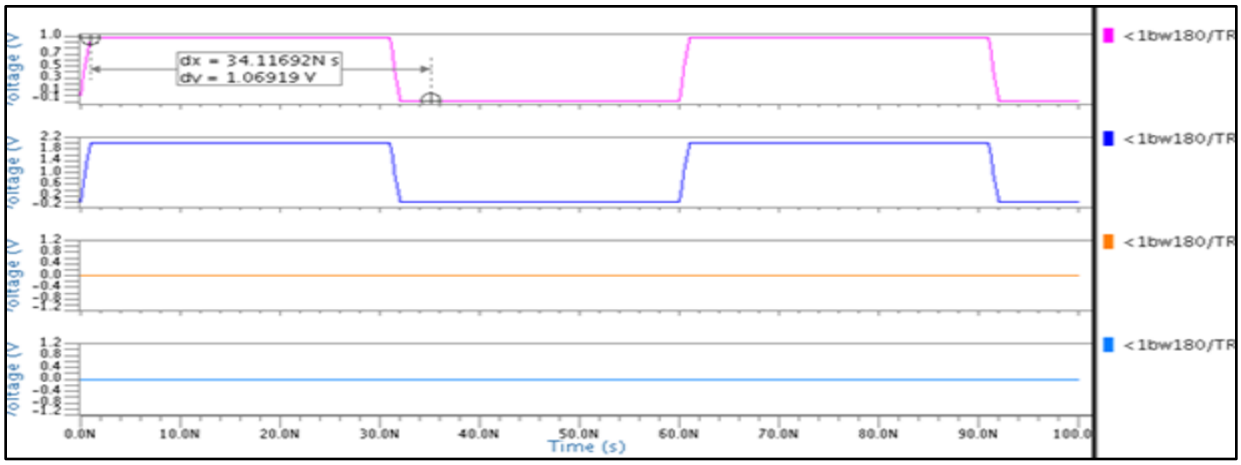

Figure 4: input 100 and output is 1.06V for 3 bit binary weighted Current steering w-2w

Simulation result of 3 bit Thermometer Code DAC in 0.18um CMOS Technology

By applying input volts=2.0v as a pulse and digital input from 0000001 to 1111111 for 3 bit I achieved respective voltage and observe respective parameters like INL and DNL Offset, etc

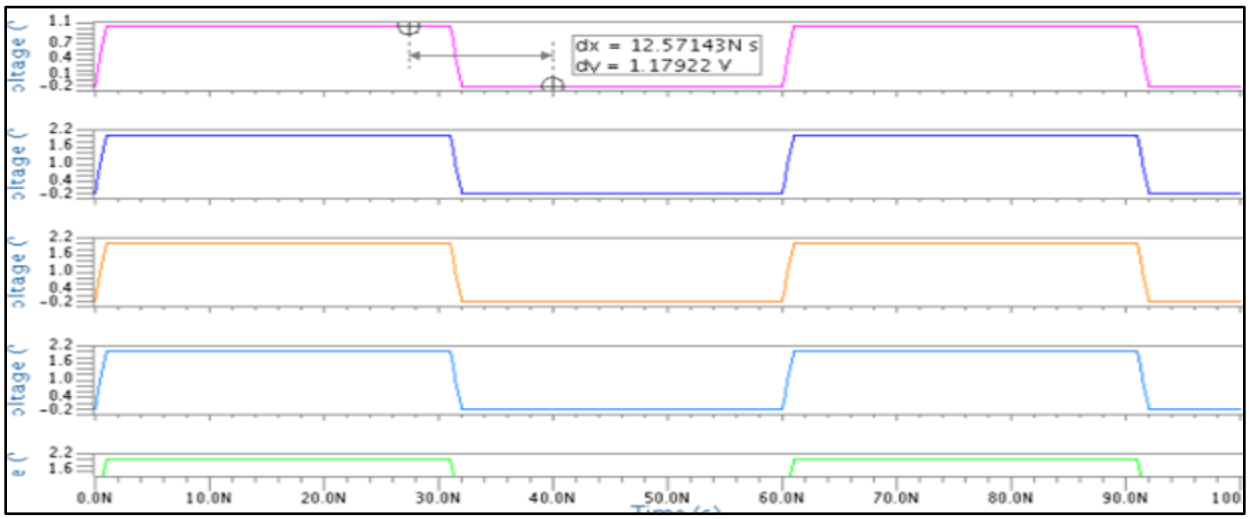

Figure 5: : input 0011111 and output is 1.17V for 3 bit Thermometer Code DAC

INTEGRAL NONLINEARITY

INL= Output value for input code n – output value of the reference line at that point

$$|\Delta I_K|_{max,INL} = \frac{I_{REF}}{2^N}$$

A binary-weighted current steering DAC we assume the current source corresponding to the MSB, B_{N-1} has a maximum positive mismatch error and the remaining bits B_0 Through B_{N-2}

have a maximum negative mismatch from Ideal so that the errors sum to zero. Thus the worst case INL for an N-bit DAC will given in above Equation, where ΔI_K is the mismatch in current source and $|\Delta I_K|_{max,INL}$ is the condition to keep the INL< 0.5 LSB.

Here for 3 bit Current Steering DAC Maximum INL is 0.15 and for 3 bit thermometer code DAC Maximum INL is 0.05 Shown in below Figure

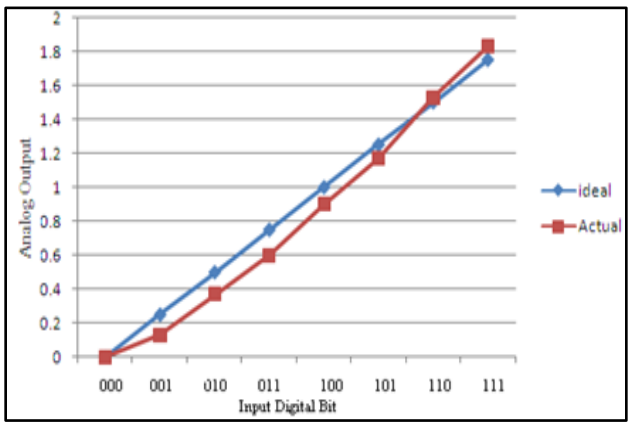

Figure 6: INL of Thermometer code DAC

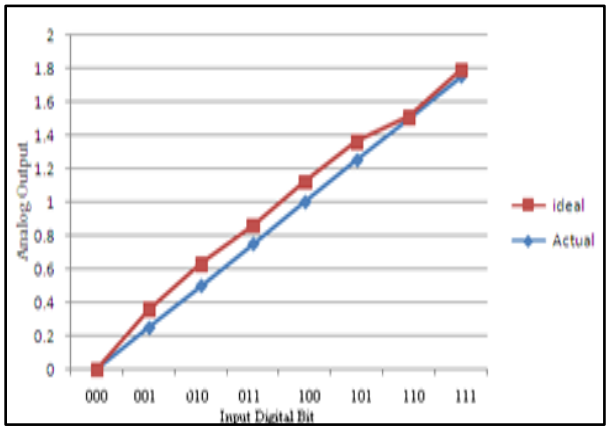

Figure 7: INL of Current steering DAC

DIFFERENTIAL NONLINEARITY

DNL = Actual increment height of transition n - Ideal increment height

A binary-weighted current steering DAC we assume the current source corresponding to the MSB, B_{N-1} has a maximum positive mismatch error and the remaining bits B_0 Through B_{N-2} have a maximum negative mismatch from Ideal so that the errors sum to zero. Thus the worst case INL for an N-bit DAC will given in above Equation, where ΔI_K is the mismatch in current source and $|\Delta I_K|_{max,DNL}$ is the condition to keep the DNL< 0.5 LSB.

The DNL will be largest at midscale when the input transitions from 0111..11 to 10000…00.for the DNL to be <0.5 LSB, the requirements for worst case mismatch are more stringent than INL.

$$|\Delta I_K|_{max,DNL} = \frac{I_{REF}}{2^{N+1} - 2}$$

Here for 3 bit Current Steering DAC Maximum DNL is 0.15 and for 3 bit thermometer code DAC Maximum DNL is 0.05 Shown in below Figure

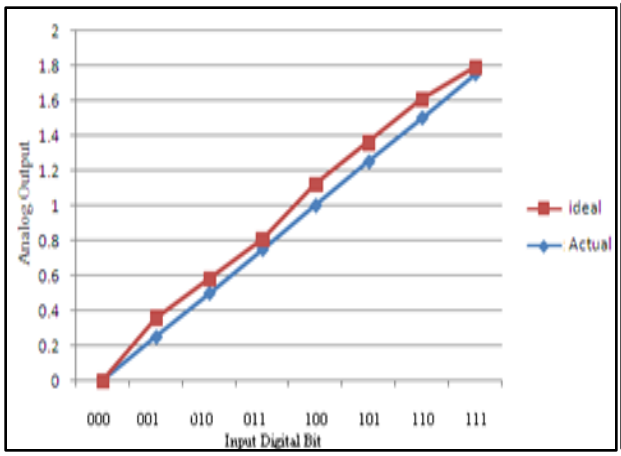

Figure 8: DNL of Current steering DAC

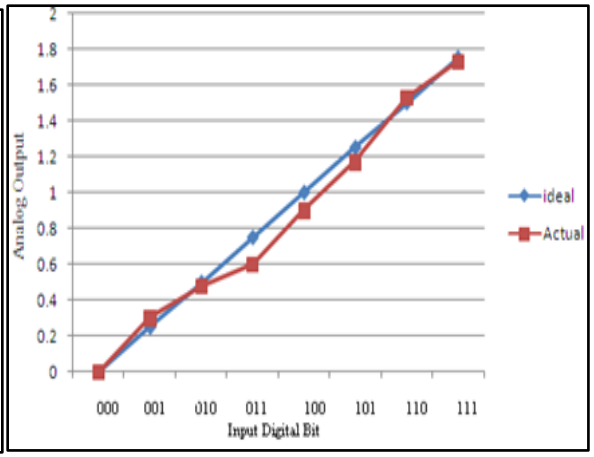

Figure 9: DNL of Thermometer code DAC

V. CONCLUSION

In this paper analysis of 3-bit Current Steering and Thermometer Code DAC proposed with most of the specification in the last decade has been done. All analysis have been supported by simulations results. To carry out the simulations Eldo spice. For all about Pre Layout simulation has been realized using (0.18um) CMOS process Technology. For Current Steering DAC Maximum INL and DNL 0.15 and For Thermometer Code Maximum INL and DNL 0.05 .

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