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TIME-BASED ALL-DIGITAL TECHNIQUE FOR ANALOGBUILT-IN SELF-TEST

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Abstract-- *A scheme for built-in self-test of analog signals with minimal area overhead for measuring on-chip voltages in and all-digital manner is presented. The method is well suited for a distributed architecture, where the routing of analog signal saver long paths is minimized. A clock is routed serially to the sampling heads placed at the nodes of analog test voltages. This sampling head present at each test node, which consists of a pair of delay cells and a pair of flip-flops, locally converts the test voltage to a skew between a pair of sub sampled signals, thus giving rise to as many sub sampled signal pairs as the number of nodes. To measure a certain analog voltage, the corresponding sub sampled signal pair is fed to a delay measurement unit to measure the skew between this pair. The concept is validated by designing a test chip in a UMC 130-nm CMOS process .Sub-mill volt accuracy for static signals is demonstrated for measurement time of a few seconds, and an effective number of bits of 5.29 is demonstrated for low-bandwidth signals in the absence of sample-and-hold circuitry.*

Keywords- *CMOS, Xilinx, flipflops , BIST.*

I. INTRODUCTION

Bias variation is a common problem in analog circuits and is getting worse as the technology scales. This is because the process variation is increasing and the power supply is reducing. With the increasing popularity of mixed signal IC designs in the deep submicron processes, it is of interest to precisely measure analog voltages for test and debugging purposes. Such situations arise when measuring on-chip voltages for built-in self-test (BIST) applications, while measuring voltages at the terminals of sleep transistors for power monitor applications, and in measuring low bandwidth signals in sensor systems. These analog voltages could be potentially located all over the chip. It is desirable that the measurement circuitry employed in such situations occupies as small an area as possible and is simple to design.

A technique was suggested in and for displaying analog signal waveforms using the technique of sub sampling .Although the method is well suited for viewing waveforms in Manuscript received May 7, 2012; revised October 17, 2012; accepted December 28, 2012. This work was supported by the Department of Information Technology, Ministry of Communication and Information Technology Government of India. The authors are with the Department of electrical Communication Engineering Indian Institute of Science, Color versions of one or more of the figures in this paper are available online at Digital Object Identifier a laboratory, it cannot be used directly for automated testing. n [1], an architecture of an analog/RF BIST subsystem was proposed, as well as the maximum area permissible for the BIST subsystem for the total (manufacturing and testing) cost reduction. In the proposed architecture, the dc voltages (of BIST sensors) of the test nodes are all tied together to a common bus and digitized centrally through a 12-b analog-to digital converter (ADC).

Even ac signals are converted to dc through an envelope detector circuit, but calibration is required in this case to map the digitized values to analog amplitudes .In such cases, one has to know the number of sensor nodes in advance or design for a worst case scenario to ensure that the ac case, calibration puts a lower bound on the testing time required. It would be beneficial to have an approach where the design of a driver for the bus can be made independent of the number of test nodes, and also eliminate the need for calibration in testing a.c. signals, which would reduce the time required for testing.

Techniques of analog routing, where in voltages and/or currents to be measured in some internal circuitry are literally “scanned” out to test pins, have been proposed but here analog circuits are used to route analog voltages/currents, which can themselves lead to signal distortion during propagation. It is hence desirable to have testing circuitry that is simpler than those being tested. Analog routing with digital interface has also been proposed, where an analog voltage is digitized and the bits are scanned out through a single pin. Similarly, one can also scan in digital bits and excite circuits with analog voltages using a digital-to-analog converter (DAC). But with reducing power supply voltages in the deep sub micrometer technology nodes, leading to reduction in the available voltage headroom, designing conventional AD architectures for such applications is becoming increasingly difficult. However, in the case of time-based architectures, time resolution has improved since the transition time of digital signals has reduced with technology scaling the all-digital nature of time-based approaches offers itself for scaling and suits the stringent area and power specifications.

II. ARCHITECTURE OF BIST

BIST is basically same as off-line testing using ATE where the test pattern generator and the test response analyzer are on-chip circuitry (instead of equipments). As equipments are replaced by circuitry, so it is obvious that compressed implementations of test pattern generator and response analyzer are to be designed. The basic architecture of BIST is shown in Figure 2.1.

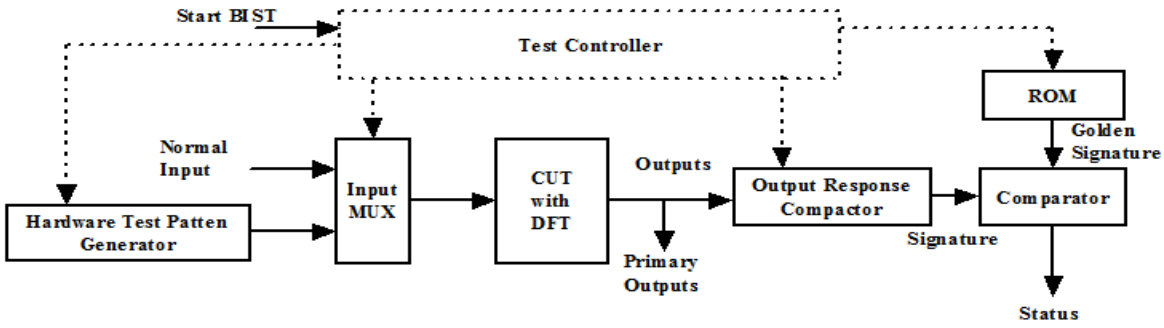

Figure 2.1. Existing architecture of BIST

As shown in Figure 2.1, BIST circuitry comprises the following modules (and the following functionalities)

2.1.1 Hardware Test Pattern Generator: This module generates the test patterns required to sensitize the faults and propagate the effect to the outputs (of the CUT). As the test pattern generator is a circuit (not equipment) its area is limited. So storing and then generating test patterns obtained by ATPG algorithms on the CUT (discussed in Module XI) using the hardware test pattern generator is not feasible. In other words, the test pattern generator cannot be a memory where all test patters obtained by running ATPG algorithms (or random pattern generation algorithms) on the CUT are stored and applied during execution of the BIST. Instead, the test pattern generator is basically a type of register which generates random patterns which act as test patterns. The main emphasis of the register design is to have low area yet generate as many different patterns (from 0 to 2^n , if there are n flip-flops in the register) as possible.

2.1.2 Input Mux: This multiplexer is to allow normal inputs to the circuit when it is operational and test inputs from the pattern generator when BIST is executed. The control input of the multiplexer is fed by a central test controller.

2.1.3 *Output response compactor:* Output response compacter performs lossy compression of the outputs of the CUT. As in the case of off-line testing, in BIST the output of the CUT is to be compared with the expected response (called golden signature); if CUT output does not match the expected response, fault is detected. Similar to the situation for test pattern generator, expected output responses cannot be stored explicitly in a memory and compared with the responses of the CUT. So CUT response needs to be compacted such that comparisons with expected responses (golden signatures) become simpler in terms of area of the memory that stores the golden signatures.

2.1.4 *ROM:* Stores golden signature that needs to be compared with the compacted CUT response.

2.1.5 *Comparator:* Hardware to compare compacted CUT response and golden signature (from ROM).

2.1.6 *Test Controller:* Circuit to control the BIST. Whenever an IC is powered up (signal start BIST is made active) the test controller starts the BIST procedure. Once the test is over, the status line is made high if fault is found. Following that, the controller connects normal inputs to the CUT via the multiplexer, thus making it ready for operation.

Among the modules discussed above, the most important ones are the hardware test pattern generator and the response compactor. The other ones are standard digital blocks [1]. In the next two sections we will discuss these two blocks in details.

2.2 HARDWARE PATTERN GENERATOR

There are two main targets for the hardware pattern generator—(i) low area and (ii) pseudo-exhaustive pattern generation (i.e., generate as many different patterns from 0 to 2^n as possible, if there are n flip-flops in the register). Linear feedback shift register (LFSR) pattern generator is most commonly used for test pattern generation in BIST because it satisfies the above two conditions. There are basically two types of LFSRs, (i) standard LFSR and (ii) modular LFSR.

2.2.1 MODULAR LFSRS

This LFSR in terms of the matrix can be written as $X(t+1)=T_S X(t)$. It may be noted the matrix T_sT_s defines the configuration of the LFSR. Leaving behind the first column and the last row T_s is an identity matrix; this indicates that X_0 gets input from X_1, X_1 gets input from X_2 and so on. Finally, the first element in the last row is 1 to indicate that X_{n-1} gets input from X_0. Other elements of the last row are the tap points $h_1,h_2,\ldots h_{n-2},h_{n-1}$. The value of $h_1,h_2,\ldots h_{n-2},h_{n-1}$, indicates that output of flip-flop X_i provides feedback to the linear XOR function. Similarly, the value of $h_i=0,\ (1\le i\le n-1)$, indicates that output of flip-flop X_i does not provide feedback to the linear XOR function.

This LFSR can also be described by the characteristic polynomial:

$$f(x)=1+h_1x+h_2x^2+\ldots h_{n-2}x^{n-2}+h_{n-1}x^{n-1}+x^n$$

Now, we give an example of a standard LFSR and illustrate the pattern generated the register. Figure 2.2 shows an example of a standard LFSR.

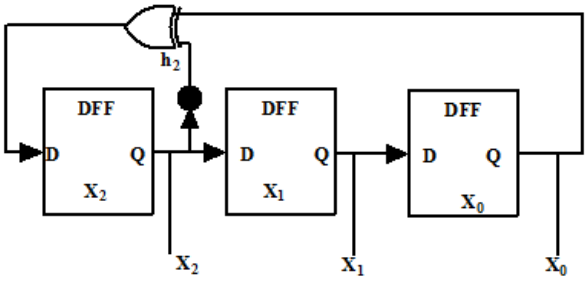

Fig 2.2: Example of a standard LFSR

The matrix of the LFSR is a follows:

$$\begin{bmatrix} X_0(t+1) \\ X_1(t+1) \\ X_2(t+1) \end{bmatrix} = \begin{bmatrix} 0 & 1 & 0 \\ 0 & 0 & 1 \\ 1 & 0 & 1 \end{bmatrix} \begin{bmatrix} X_0(t) \\ X_1(t) \\ X_2(t) \end{bmatrix}$$

It may be noted that output of flip-flop X_2 provides feedback to the XOR network, while flip-flop X_1 does not; so $h_1=0$ and $h_2=1$. The characteristic polynomial of the LFSR is $f(x)=1+x^2+x^3$.

If the initial values of the flip-flops are $X_0=1,X_1=0,X_2=0$ then the sequence of patters is as follows:

$$\begin{bmatrix} X_0 \\ X_1 \\ X_2 \end{bmatrix} ::: \begin{bmatrix} 1 & 0 & 0 & 1 & 1 & 1 & 0 & 1 & 0 \\ 0 & 0 & 1 & 1 & 1 & 0 & 1 & 0 & 0 \\ 0 & 1 & 1 & 1 & 0 & 1 & 0 & 0 & 1 \end{bmatrix}$$

So the LFSR generates 7 patterns (excluding all 0s) after which a pattern is repeated. It may be noted that this LFSR generates all patters (except all 0s) which are generated by a 3 bit counter, however, the area of the LFSR is much lower compared to a counter. In a real life scenario, the number of inputs of a CUT is of the order of hundreds. So LFSR has minimal area compared to counters (of order of hundreds).

2.2.2 MODULAR LFSRS

Figure 2.3 shows an internal exclusive-OR also called modular LFSR. The circuit representation of modular LFSR is shown in Figure 2.4. The difference in modular LFSR compared to standard LFSR is due to the positions of the XOR gates in the feedback function; in modular LFSR XOR gates are in between adjacent flip-flops. Modular LFSR works faster than standard LFSR, because it has at most one XOR gate between adjacent flip-flops, while there can be several levels of XOR gates in the feedback of standard LFSR.

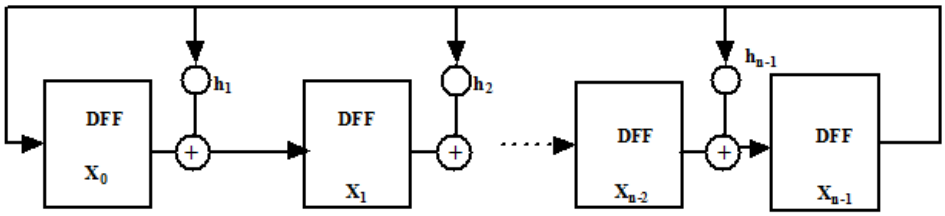

Fig 2.3: Modular LFSR

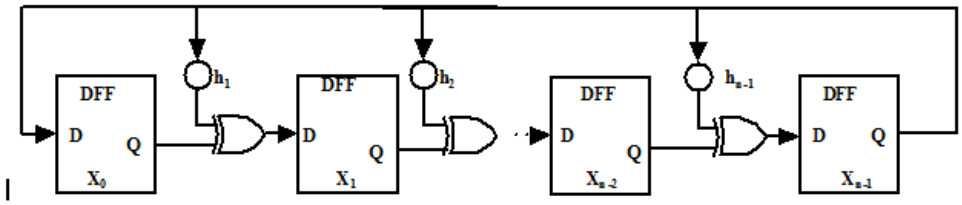

Fig 2.4: Circuit representation of modular LFSR

In modular LSFR the output of any flip-flop may or may not participate in the XOR function; if output of any flip-flop X_i say, provides input to the XOR gate which feeds the input of flip-flop X_{i+1} then corresponding tap point h_i (Figure 2.3) is 1. In the circuit representation (Figure 2.4) of $h_{i=1}$, then there is an XOR gate from output of flip-flop X_i to input of flip-flop X_{i+1}; else output of flip-flop X_i is directly fed to input of flip-flop X_{i+1}.

Similar to standard LFSR, a properly-designed modular LFSR can generate a near-exhaustive set of patters, as it can cycle through distinct 2^n-1 states (except 0s is all flip-flops).

The following matrix system of equations describes the modular LFSR.

$$\begin{bmatrix} X_0(t+1) \\ X_1(t+1) \\ X_2(t+1) \\ \cdots\cdots\cdots \\ X_{n-2}(t+1) \\ X_{n-1}(t+1) \end{bmatrix} = \begin{bmatrix} 0 & 0 & 0.....0 & 1 \\ 1 & 0 & 0.....0 & h_1 \\ 0 & 1 & 0.....0 & h_2 \\ \cdots\cdots\cdots\cdots\cdots\cdots\cdots\cdots \\ 0 & 0 & 0.....0 & h_{n-2} \\ 0 & 0 & 0.....1 & h_{n-1} \end{bmatrix} \begin{bmatrix} X_0(t) \\ X_1(t) \\ X_2(t) \\ \cdots\cdots \\ X_{n-2}(t) \\ X_{n-1}(t) \end{bmatrix}$$

This LFSR given the matrix can be written as $X(t+1) = T_S X(t)$. In this case $X_0(t+1) = X_{n-1}(t)$, which implies that X_{n-1}. Directly feedbacks X_0. $X_1(t+1) = X_0(t) + h_1 X_{n-1}(t)$. , which implies that depending on h_1 =0 (or 1), input to X_1 is X_0 (or X_0XORed with output of X_{n-1}). Similar logic holds for inputs to all flip-flops from $X_n$to X_{n-1}.

This LFSR can also be described by the characteristic polynomial:

$$f(x) = 1 + h_1 x + h_2 x^2 + \ldots h_{n-2} x^{n-2} + h_{n-1} x^{n-1} + x^n$$

Now, we give an example of a modular LFSR and illustrate the pattern generated by the register.

III. PROPOSED SOLUTION

As shown in Fig. 3.1, sampling heads are placed at each test node in order to minimize the routing of analog signals overlong paths. Each sampling head consists of a pair of identical delay cells (V2D) and a pair of flip-flops (DFF), as shown. A clock signal is routed serially to all the sampling heads, which is fed to both the delay cells in the sampling head. The delay of one element of the pair is controlled by the analog voltage VAi , and that of the other by a reference voltage Vref. Thus, a voltage difference between the node voltage and reference shows up as a delay difference in the clocks at the output of the delay cell pair. This pair of clocks is sampled by a slightly slower sampling clock, giving rise to a pair of beat frequency signals. We call them the subsample signals, and the skew between them is "amplified" by this process of "sub sampling" The details are explained in Section IV-A. Hence, there will be as many pairs of sub sampled signals as there are test nodes.

Another possible approach for the same setting, proposed in , although reduces the number of flip-flops used, has the limitation that nodes that do not contribute to signal information may end up adding to the noise since the sub sampled signals are daisy-chained through all the sampling heads. This technique of sub sampling provides bandwidth/resolution tradeoff, i.e., measurements requiring coarser resolutions can be done faster whereas finer resolution measurements need more time. It is not mandatory that Vref of Fig. Be the same amongst all IPs. If it is of interest to measure voltage difference between two voltages in the same IP, Vref can be replaced by that voltage. Such a situation arises when a programmable current source is employed to achieve current matching in the presence of variations. Otherwise, Vref can just be grounded. Ground bounce is not a concern, as the technique presented performs averaging over few seconds as determined by the settings.

A. Measurement Procedure

1) Calibration: Because of the nonlinearity of the delay cells, they will need to be calibrated a priori. The delay cell pair of sampling head SpHi , corresponding to VAi, is calibrated as follows. MUX cal (Fig. 3.1) is set to zero so that the calibration voltage is fed to one of the delay cells (instead of the local node voltage), while the other delay cell gets the reference voltage. MUX sel is set to a value so that the multiplexor selects the sub sampled pair corresponding to Sp Hiand feeds it to the DMU. Suppose gi1 and gi2 are the voltages to delay functions of the two delay cells of the sampling head SpHi , respectively, then the delay difference out of this sampling head, _Di, is given by _Di = gi1(Vcal) − gi2(Vref).But we are more interested in _Vi = Vcal−Vref. So, we define function fi (・) mapping _Vi to _Di as_Di = fi (Vcal−Vref) = fi(_Vi). (1)The calibration step measures this (potentially nonlinear)function f (・) at few points, which is used later to correct for nonlinearity and bias. Calibration also helps in mitigating mismatches, if any, between the delay cell pairs.

The delay at the input of the DMU is given as _DDMU = Di + _D residual where _D residual is the delay difference in the clock pair accrued in the rest of the path. This number will be independent of the voltage at node i and hence can be easily calibrated out.2) Measurement: During the measurement process, MUX cal(Fig. 3.1) is set low. To measure VAi , the corresponding sub sampled signal pair is selected by the multiplexor.

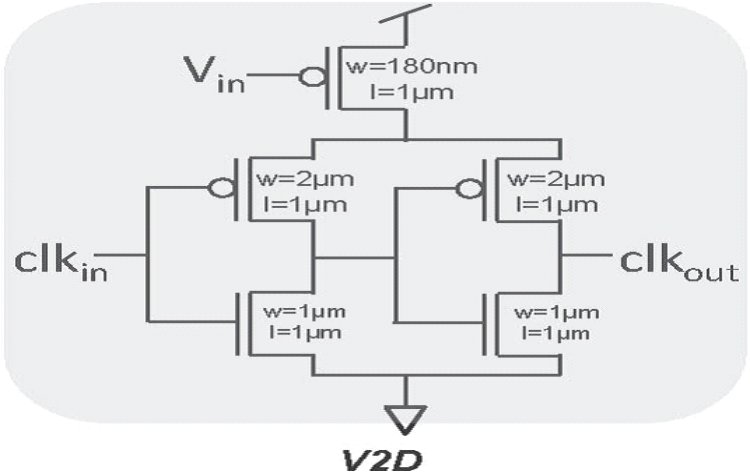

Fig 3.1. Schematic circuit of current-starved voltage-to-delay cell (V2D).

Thus, the delay cell pair of sampling head SpHi will create a delay differential given as_Di = gi1(V Ai) − gi2(Vref) (3):= fi (VAi−Vref). (4)The input delay difference at the DMU is as given in (2).From the calibration data, VAi can be inferred directly or by interpolation. Voltage-to-Delay Cell There are many existing topologies for a voltage-controlled delay element. a linear zed voltage is presented to a pulse-delay-time converter suitable for ADCs, based on current-starved

inverters. In this paper, our target measurement range was 0–100 mV. Hence, we have used PMOS-controlled current-starved inverters. However, alternative delay cell architectures could be used for other applications as the specifications demand. The area of the pair of delay cells chosen for this application and taped out is8.2 × 8.4 µm. As is evident from the circuit, the voltage influences only the delay of the rising edge, while the delay of the falling edge is uncontrolled. Hence, having chosen an input clock period of T and duty ratio D, the range of the system is the value of Vin that gives an absolute delay of Dr, where Dr = D×T, which is the maximum rising edge delay possible. For instance, for a clock period of 125 ns, a duty ratio of 0.5 and 120 mV gives delay of 62.5 ns, then the range of the system is1 120 mV. This range can be increased therefore by increasing the duty ratio, or input clock period, or both. A better design from the1The actual dynamic range will be slightly less due to some margin for the falling edge skew eliminator algorithm.

3.2 VOLTAGES-TO-DELAY CELL:

There are many existing topologies for a voltage-controlled delay element. In a linear zed voltage is presented to a pulse-delay-time converter suitable for ADCs, based on current-starved inverters. In this paper, our target measurement range was 0–100 mV. Hence, we have used PMOS-controlled current-starved inverters, as shown in Fig. 2. However, alternative delay cell architectures could be used for other applications as the specifications demand. The area of the pair of delay cells chosen for this application and taped out is8.2 × 8.4 µm .As is evident from the circuit, the voltage influences only the delay of the rising edge, while the delay of the falling edge is uncontrolled. Hence, having chosen an input clock period of T and duty ratio D, the range of the system is the value of Vin that gives an absolute delay of Dr, where Dr = D×T, which is the maximum rising edge delay possible. For instance, for a clock period of 125 ns, a duty ratio of 0.5 and 120 mV gives a delay of 62.5 ns, then the range of the system is1 120 mV .This range can be increased therefore by increasing the duty ratio, or input clock period, or both. A better design from the1The actual dynamic range will be slightly less due to some margin for the falling edge skew eliminator algorithm.

3.3 DESIGN CONSIDERATION:

With the sizing of the delay cell circuitry, the capacitance between the analog voltage and the input clock is about2 fF. With a decoupling capacitor of 4 pF, the kickback will be less than 0.6 mV. For a smaller kickback, either the decoupling capacitor has to be increased, or cas coding has to be implemented. With a transistor of gain 20 in the cascade, the decoupling capacitor can be as small as 0.1 pF. Since the delay of every cell is sensitive to supply voltage, variations in supply voltage directly impacts the voltage measurement. The power supply will have a distribution profile across the chip. This profile will get calibrated out provided the power supply does not change too much with time. To combat a time-varying supply voltage, a solution is tomake use of delay cells with a good power supply rejection ratio or to use a regulated power supply. Placing a transistor in cascade also helps to mitigate the effect of power supply noise on delay. The measurement of bias voltages is heavily dependent on Vcal for the calibration and interpolation. Hence, the generation of Vcal will have to be accurate and has to be shielded well so that noise coupled onto V cal will not impact the measurement. The noisy currents of the voltage-to-delay converter contribute to jitter on the clocks.

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IV. RESULTS

4.1 SIMULATION AND SYNTHESIS:

The differences in the delay ranges for the similar settings are present because they were measured on different days and hence conditions such as the supply voltage and temperature could be different. However, the measurements taken with the same setting about couple of hours apart (after offset cancellation 6) is stable enough. The use of this system necessitates precise control of the sampling clock frequency. This may be achieved by deriving this sampling clock from the core clock and mimicking asynchrony by artificially introducing frequency modulation .

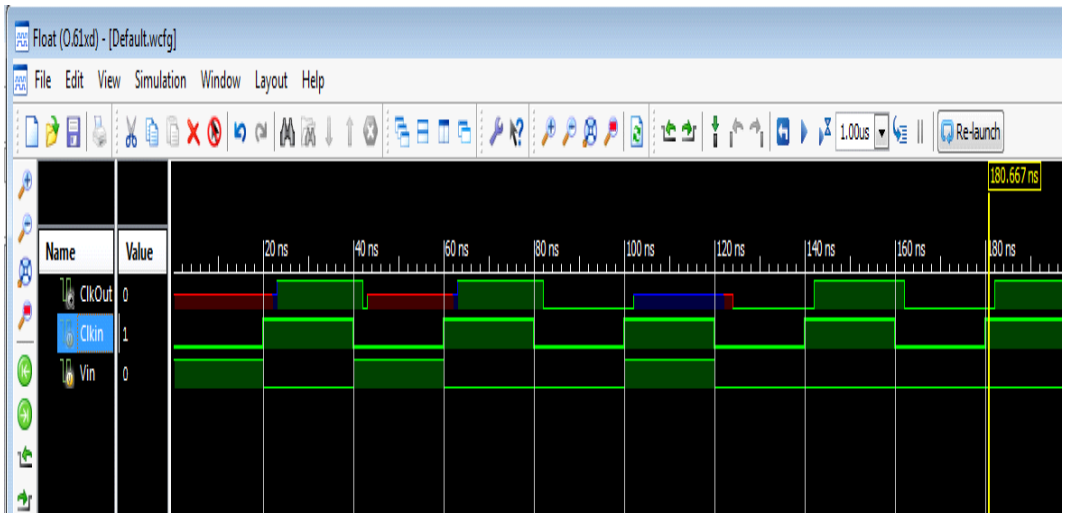

Fig 4.1: Waveform 1

Here the voltage to delay cell simulation is produce on different conditions according to the primitive Construction table of the V2D, the Clock out is Generated block is produced with some delay of Clkout.

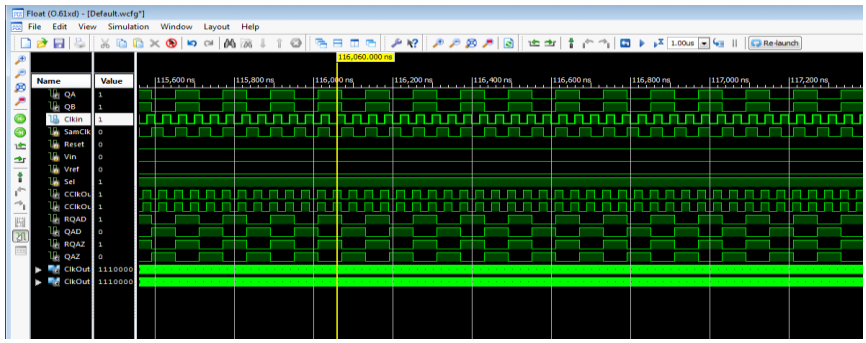

Fig 4.2: WaveForm 2

This is the simulation of On chip FrontEnd Module Contains Signal of Clkin, SamClkin, MuxSel, Vin , Vref signal on different Contains it is Produce it is Output Simulation Waveform QA,QB,. We Can observe the Delay below Clkin, with 12 Voltage to Delay cell of Vin and 12 Voltage to Delay Cell of Vref Voltage can be Observed by ClkOutA, ClkOutB internal Signal . Based MuxSel the input which feed from Reg generated it respective output.

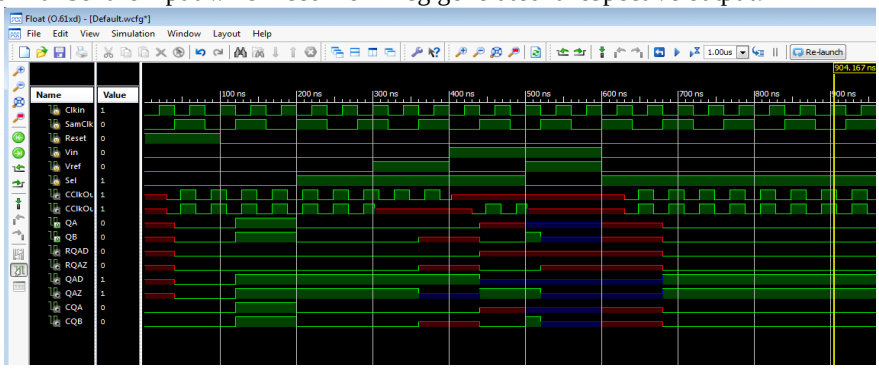

Fig 4.3: Waveform 3

This is the simulation of On chip FrontEnd Module with falling edge skew eliminatorContains Signal of Clkin, SamClkin, MuxSel, Vin , Vref signal on different Contains it is Produce it is Output Simulation Waveform QA,QB, CQA, CQB. We Can observe the Delay below Clkin, with 12 Voltage to Delay cell of Vin and 12 Voltage to Delay Cell of Vref Voltage can be Observed by ClkOutA, ClkOutB internal Signal .

Based MuxSel the input which feed from Reg generated it respective output. Based on the SamClkin Signal the Falling Skew Eliminator Block reduce the transistion from the Fallling edge of transition that can be taking place from 1 0 transistions and it produce CQA and CQB output Signal.

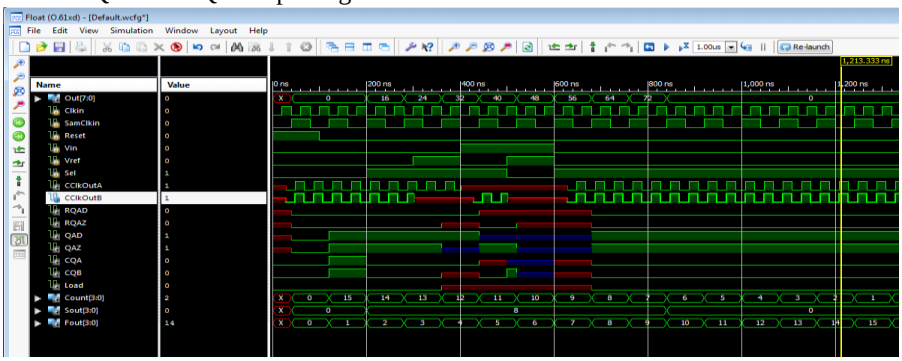

Fig 5.3: Waveform 4

This is the simulation of On chip FrontEnd Module with falling edge skew eliminatorContains Signal of Clkin, SamClkin, MuxSel, Vin , Vref signal on different Contains it is Produce it is Output Simulation Waveform QA,QB, CQA, CQB. We Can observe the Delay below Clkin, with 12 Voltage to Delay cell of Vin and 12 Voltage to Delay Cell of Vref Voltage can be Observed by ClkOutA, ClkOutB internal Signal . Based MuxSel the input which feed from Reg generated it respective output. Based on the SamClkin Signal the Falling Skew Eliminator Block reduce the transistion from the Fallling edge of transition that can be taking place from 1 0 transistions and it produce CQA and CQB output Signal. This signal Goes into the add Block that generate enable signal based on the updown counter operation is perform and shiftregister take now finally interpolation taking place. Here we are using 4- bit counter and 4- shifter register for that it is generate that o/p sequence random 0, 16, 24,32,40, 48, 56, 64,72 then same sequence generation can be operated.

V. CONCLUSION

A scheme for analog BIST is proposed, which is well suited to measure voltages distributed all over a chip by locally converting the test voltage into skew between a pair of sub sampled signals. This was achieved by a sampling head placed at each test node, each sampling head consisting of a pair of voltage-controlled delay cells and a pair of flip flops. This approach reduces the routing of analog signals overlong paths to the measurement unit, thereby saving chip area due to absence of shielding lines. Instead, a clock signal, a sampling clock of slightly different frequency, needs to be routed serially to each sampling head, and a pair of low frequency sub sampled signals need to be routed to the central DMU .

Behavioral modeling of the system was also presented, which indicates that a resolution of up to 12 b can be obtained by this approach. To validate the concept, we have implemented a sampling head in a UMC 130-nm process node and implemented the DMU on FPGA. Measured results from the test chip demonstrated a measurement accuracy of about 2 mV for a measurement time of about 1 s. This is reasonable for measuring bias voltages and other such static signals. An effective 5.29 b of resolution was demonstrated for low-bandwidth signals too, where sample-and-hold circuitry is avoided.

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