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SIMULATION & ANALYSIS OF WIDEBAND AND LOW POWER CMOS ANALOG MULTIPLIER IN DEEP SUBMICRON TECHNOLOGY

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Abstract: In this paper CMOS Four Quadrant Analog Multiplier is designed. It is based on combiner circuit and subtractor circuit, where subtractor circuit is used for input block and combiner circuit is act as nonlinear cancellation path. Simulated results using Eldo spice in Mentor Graphics Tools for a standard TSMC 180nm CMOS technology and power supply V_{DD} is taken 1.5V. The main performances of the multiplier including bandwidth, power dissipation, and gain are improved.

Keywords: Analog Multiplier,Combiner circuit, Subtractor circuit

1. INTRODUCTION

In analog signal processing the need often arises for a circuit that takes two analog inputs and produces an output proportional to their product. Such circuits are termed analog multiplier. So, the ideal output of the multiplier is $V_{out} = K_m.V_xV_y$, Where K_m = multiplier gain unit.Four quadrant analog multipliers are very useful building blocks in many circuits such as adaptive filters, frequency shifters, and modulators. These applications are required to operate in low voltage environment for improving their power efficiency and incorporating with mixed signal systems to be used in portable application.There are several means to realize a four quadrant analog multiplier and it is also suggested by that using saturated MOSFET in strong inversion is more practical than any other mean. Recently based on square law relation of Saturated MOSFET, various compact multiplier architectures. Most of them feature wide input range, high operating frequency and low power consumption which are resulted from excellent manipulation of the square law function in high compactness structure.Focusing in this designed circuit, which is seemed to be compact circuit, it is found that the overall multiplier circuit cannot be called compact since it is require an extra voltage reference connected between the resistive loads .to generate the extra voltage reference, more power consumption and circuit complexity are unavoidable. In this paper, we design a new multiplier which circuit has such an arrangement that transistor level improved such that the extra voltage reference becomes redundant and can be eliminated. This high bandwidth and low power analog multiplier is achieved using a simple combiner and subtractor circuit, the subtractor output is given as a input to the combiner and the combiner squares the given input. The difference of the two outputs of the combiner circuits gives the multiplication of two inputs, so the quarter square algebraic identity required to implement an analog multiplier is done by using very small amount of transistors which leads to small power dissipation.

The paper is being divided into six sections. In section 2, combiner circuit stage has been discussed, which combines two inputs. In section 3, subtractor circuit has been discussed

which subtract two inputs. In section 4, author has been discussed complete configuration of the CMOS analog multiplier. Section 5includes simulation result and comparison with reference. Finally in section 6, conclusion has been discussed.

2. COMBINER CIRCUIT

The combiner circuit shown in Fig. 1 takes the given set of input voltages and gives a output, which is sum of square of input voltages. It can be seen that the drain and source terminals of the NMOS transistor M1 and M2 are connected to each other, the input voltages V1 and V2 control the drain currents and these are summed in the load resistor R. Assuming matched devices and operation in the saturation region.

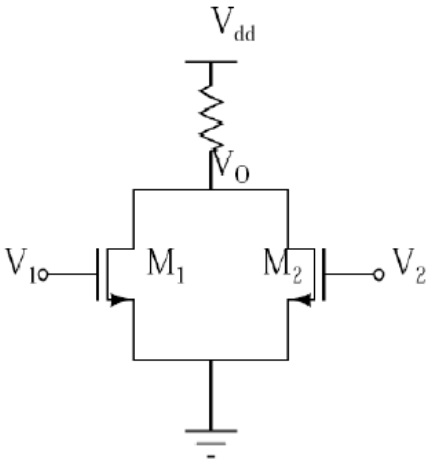

Fig.1 Combiner circuit [7]

The output voltage of the combiner may be expressed as

$$V_O = V_{DD} - K_n R\,[(V_1 - V_{tn})^2 + (V_2 - V_{tn})^2] \quad (1)$$

Where Kn is transconductance parameter, V_{tn} is threshold voltage.

From Eq. (1) it can be seen that output voltage V_O is combination of two input voltages V_1 and V_2.

3. SUBTRACTOR CIRCUIT

The subtractor circuit shown in Fig. 2 takes a set of inputs and provides an output which is the difference of two input voltages along with additional bias voltage. The output voltage V_Z differs from the input voltage V_X by the same amount as the source gate voltage of M_X, and the source gate voltage of M_X is related to the input voltage V_Y.

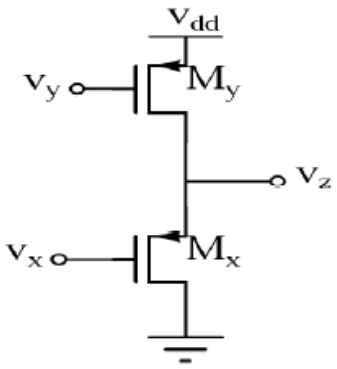

Fig.2Subtractor circuit[7]

Thus for the case of identical M_X and M_Y devices, the equation of V_Z is

$$V_Z = V_X + V_{tp} + \sqrt{\frac{I_{DX}}{K_p}} \quad (2)$$

$$I_{DX} = I_{DY} = K_p(V_{DD} - V_Y - |V_{tp}|)^2 \quad (3)$$

Substituting I_{DX} in Eq. (2) and simplifying, the output V_Z is

$$V_Z = V_X - V_Y + V_{DD} \quad (4)$$

4. CIRCUIT CONFIGURATION

The high bandwidth and low power analog multiplier shown in Fig.3 is implemented using a combination of subtractor cells and combiner circuits. The output of subtractor is given as an input to the combiner circuit, and the combiner circuit squares the two outputs of subtractor.

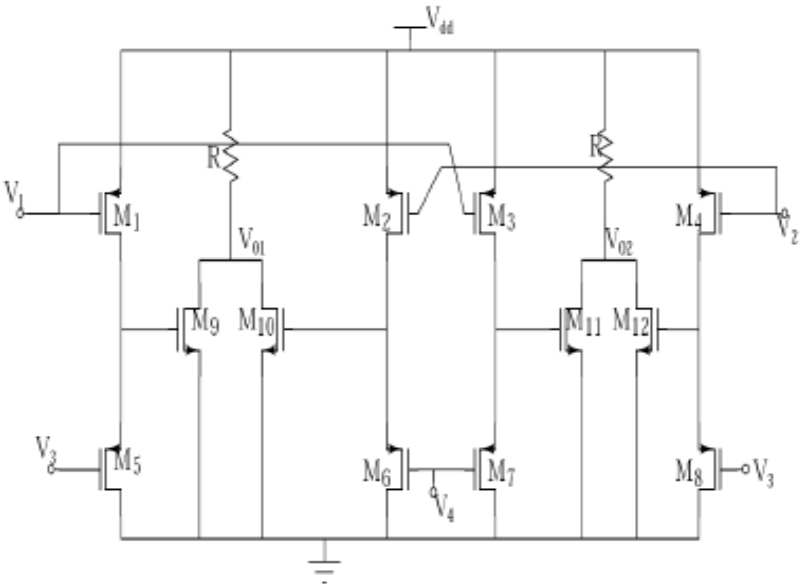

Fig. 3. CMOS Analog Multiplier [7]

Differential input voltages, defined by $V_{id1} = V_1 - V_2$ and $V_{id2} = V_3 - V_4$, are applied to input terminals of the four subtractor cells (M_1&M_5, M_2&M_6, M_3&M_7 and M_4&M_8), the outputs of which are connected to input terminals of the two combiner cells (M_9,M_{10}&R and M_{11},M_{12}&R). Applying the concept of subtractor circuit and combiner circuit to the Fig 3, the two output voltages results to

$$V_{01} = V_{DD} - K_n R\,[(V_{31} - V_{tn} + V_{dd})^2 + (V_{42} - V_{tn} + V_{dd})^2] \quad (5)$$

$$V_{02} = V_{DD} - K_n R\,[(V_{41} - V_{tn} + V_{dd})^2 + (V_{32} - V_{tn} + V_{dd})^2] \quad (6)$$

Taking $V_{OS} = V_{DD} - V_{tn}$ and simplifying Eq.(5)&(6) the values of the two outputs of combiner circuits are

$$V_{01} = V_{DD} - K_n R[(V^2{}_{41} + V^2{}_{32} + 2V_{os}(V_{41} - V_{32}) + 2V^2{}_{os} \quad (7)$$

$$V_{02} = V_{DD} - K_n R[(V^2{}_{31} + V^2{}_{42} + 2V_{os}(V_{31} - V_{42}) + 2V^2{}_{os} \quad (8)$$

Where $V_{OS} = V_{DD} - V_{tn}$ is an undesired term which is eliminated by fully differential operation. The differential output voltage can be obtained by subtracting the above two equation, yielding

$$V_{0ut} = K_n R(V^2{}_{31} + V^2{}_{42} - V^2{}_{41} - V^2{}_{32}) = -2K_n R.\,V_1.V_2 \quad (9)$$

5. SCHEMATIC AND SIMULATION RESULT

5.1 Schematic circuit

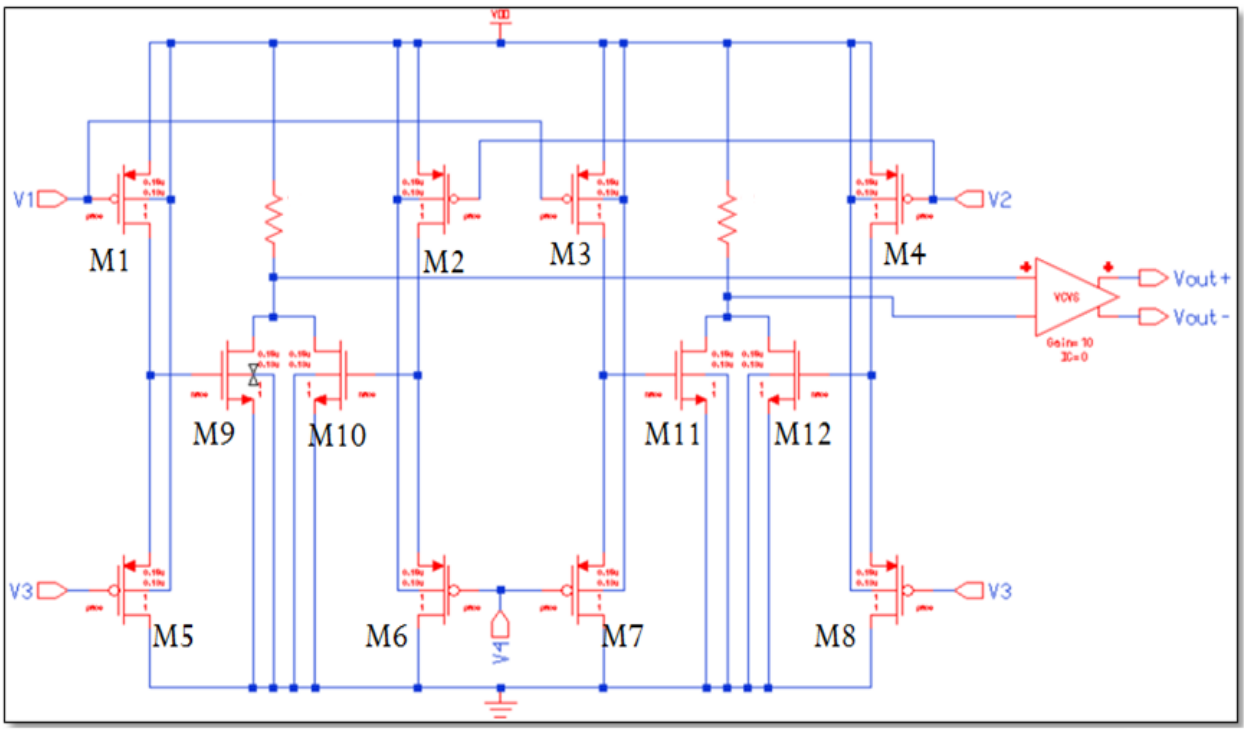

Fig. 4. Schematic Circuit of CMOS Analog Multiplier

5.2 Simulation Result

The multiplier circuit in Fig. 4 was designed and simulated by using Eldo Spice for 0.18 micron CMOS process parameter. The input voltage V_{12} and V_{34} are set to be balance with common mode voltages of 0.5V, respectively and supply voltage VDD is set at 1.2V. Amplitude modulated signal is shown for information signal of 5MHZ frequency and carrier of 60 MHZ in Fig.5. A DC sweep showing the operation of the multiplier is shown in Fig. 6. The x-input, V_x is swept from -0.1V to 0.1, while at the same time the y-input is stepped from 1V to 1V in 0.5V increment. Also DC characteristic show that CMOS Analog Multiplier is a four quadrant Multiplier. An AC characteristic of the multiplier is shown in Fig.7 and Bandwidth comes out to be 719.68 M_{HZ}.

(A)Transient response

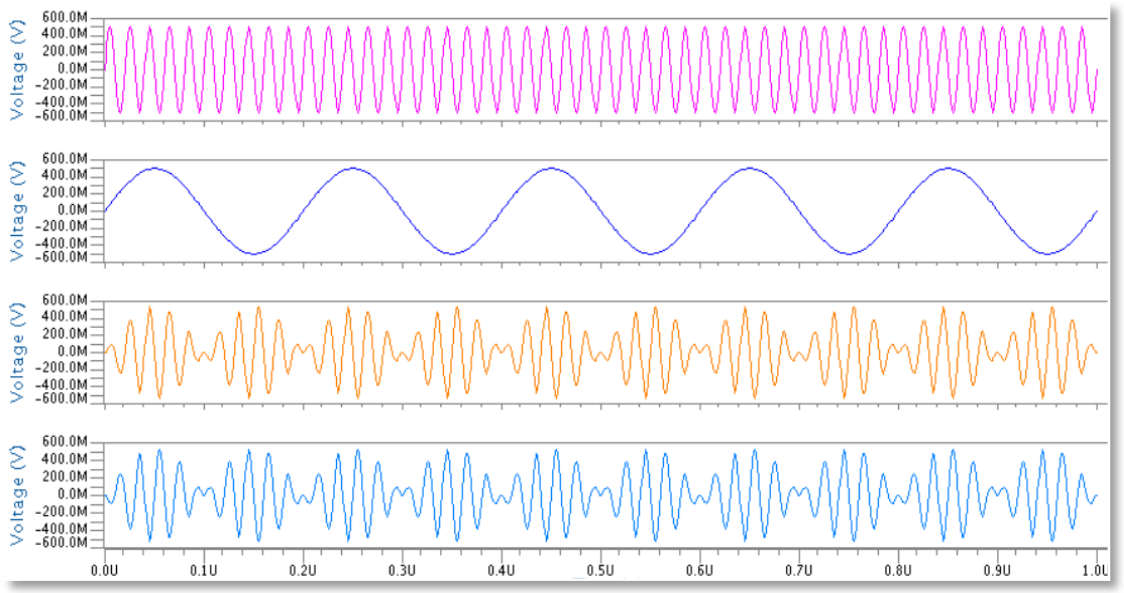

Fig. 5. Transient Response

(B) DC Characteristics

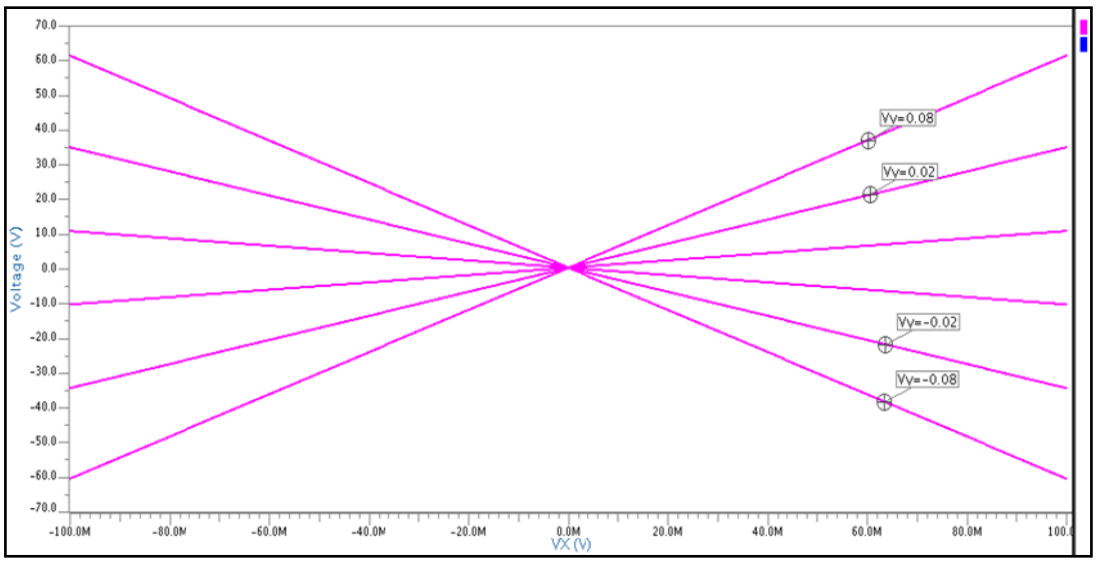

Fig. 6.DC Response

(C) Frequency Response

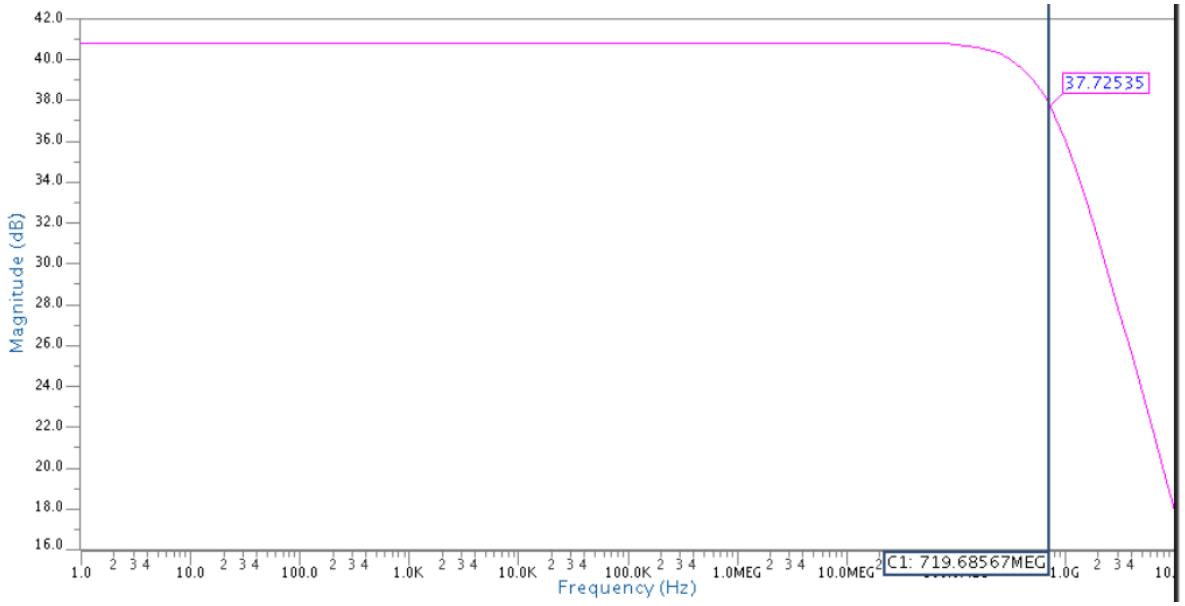

Fig.7 Frequency Response

(D) Layout

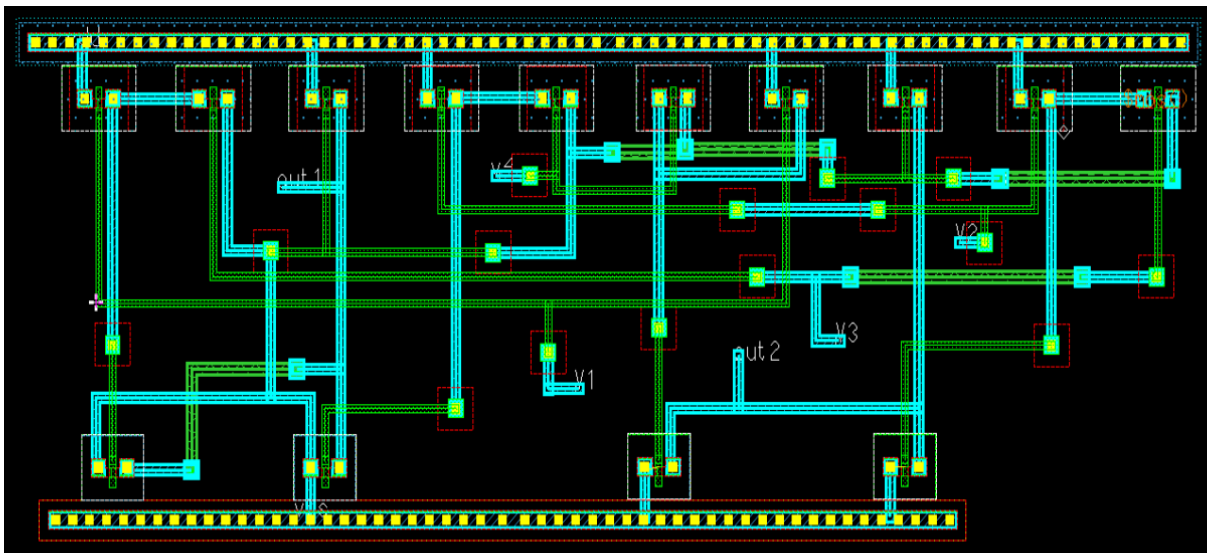

Fig. 8 Layout of CMOS Analog Multiplier

TABLE 1. Comparison of CMOS Analog Multiplier

Parameter	This Work	Ref.[7]
Power supply(V)	1.5	1.8
Bandwidth(M_{HZ})	719.68	64
Gain(dB)	37.72	-
Power dissipation(µW)	17.21	22.0

6.CONCLUSION

In this paper CMOS analog multiplier which is based on the combiner circuit and the subtractor circuit is simulated using eldo spice in Mentor Graphics tool for 180nm CMOS technology. As we seen that in above table that simulated circuit id operated at less power and also have less power dissipation. The input range of multiplier is $\pm$0.5V. The gain, bandwidth and power dissipation in 180nm CMOS technology are respectively 37.72 dB, 719.68 M_{HZ} and 17.21 µW. The layout of CMOS analog multiplier is made using IC Studio in Mentor Graphics tool and LVS is matched.

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