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Design and Analysis of a New Loadless 4T SRAM Cell with 32nm CMOS Technology

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Abstract —*A significantly large segment of modern system on chips (SoCs) is occupied by Static Random Access Memory (SRAM). The goal of this paper is to reduce power and less area of SRAM. Here two different configurations of SRAM cell are designed and analysed. The standard six-transistor (6T) SRAM cell and a new loadless four transistor (4T) SRAM cell are designed using 32nm CMOS technology. Here the various configurations of SRAM cells are designed, 1-Bit, 16-Bit, 64-Bit and 1-Kb using both 6T SRAM cell and a new loadless 4T SRAM cell using 32nm CMOS technology for checking its functionality: power dissipation, area occupancy, read access time and write access time. Compared to 6T SRAM array, the new loadless 4T SRAM array consumes less power and requires less area.*

Keywords- *6T SRAM cell, new loadless 4T SRAM cell, deep-submicron*

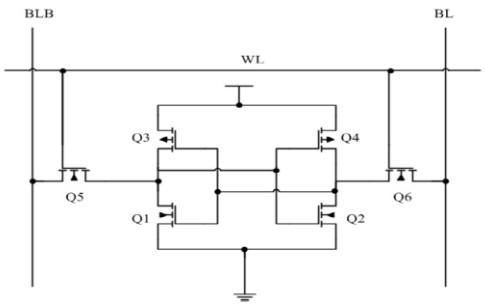
I. INTRODUCTION

A significantly large segment of modern SoCs is occupied by SRAM. The onchip caches in embedded microprocessors are implemented using arrays of densely packed SRAM Cells [01]. For instance, SRAM-based caches occupy more than 90% of 1.72 billion transistors in processor.

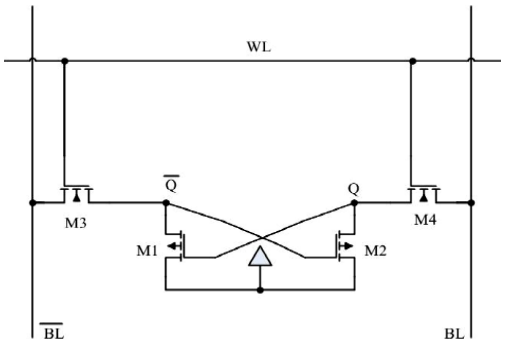
A few critical circuits in a system not only affect the design metrics but may fail to operate in deep submicron technology. Hence the SRAM arrays are designed, analysed and checked for its design metrics in deep submicron CMOS technology. Two types of SRAM cells will be considered in this paper. (i) Conventional six-transistor (6T) SRAM cell, as shown in Figure 1(a). (ii) New Loadless four-transistor (4T) SRAM. They will be designed and analysed with respect to functionality, power dissipation, area occupancy and access time. In this paper new loadless 4T SRAM cell which uses NMOS transistors as access transistors. In addition, the bitlines are precharged to ground (0volts) instead of Vdd (0.9 volts) with a 32nm CMOS technology.

II. CELL DESIGN & OPERATION

A 6T SRAM cell consists of two cross-coupled inverters (Q1-Q3 and Q2-Q4) forming a latch and the access transistors (Q5 and Q6). In the new loadless 4T SRAM cell, two NMOS transistors (M3 and M4) are used as pass transistors to access the cell and two PMOS transistors (M1 and M2) are used as drivers for the cell.To design SRAM, it require precharge circuit, sense amplifier, row and column decoder and write driver circuit. First all the peripheral circuits are discussed.



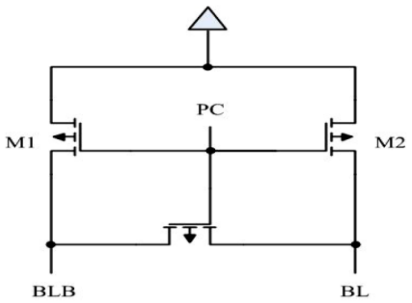
"***Figure 1. Six Transistor (6T) SRAM Cell*** [10] "



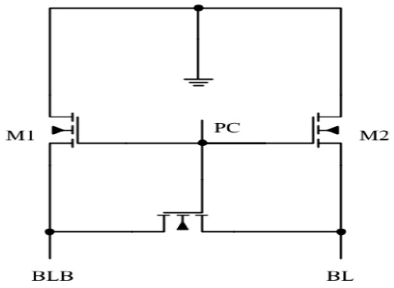
"***Figure 2.New Loadless 4T SRAM cell*** [1,2,4] "

Precharge circuit of the power line voltages in a high voltage DC application is a preliminary mode which current-limits the power source such that a controlled rise time of the system voltage during power up is achieved. When a high-voltage system is designed appropriately to handle the flow of maximum rated power through its distribution system, the

components within the system can still undergo considerable stress upon the system "power up". In some applications, the occasion to activate the system is a rare occurrence, such as in commercial utility power distribution which is typically on almost all of the time.



"***Figure 3. Precharge circuit for 6T SRAM Cell [10] "***

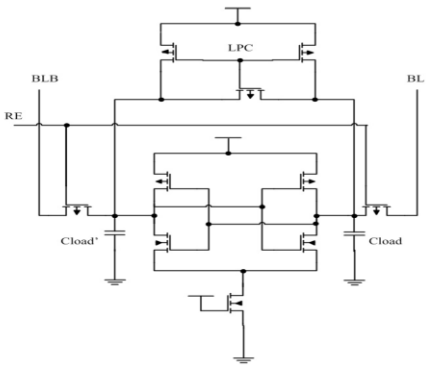


"***Figure 4. Precharge circuit for new loadless 4T SRAM Cell [10] "***

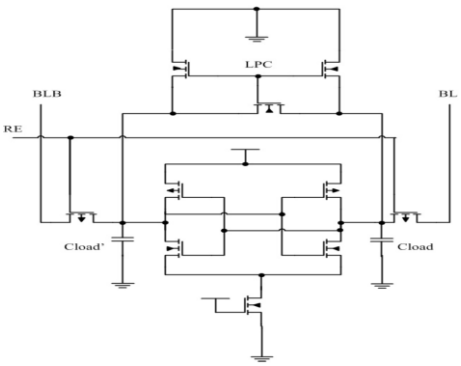
The precharge circuit used for the 6T SRAM array is show in figure 3. The function of the precharge circuit in the 6T SRAM array is to charge the Bit Line (BL) and Bit Line Bar (BLB) to VDD. In this circuit three PMOS transistors are used, which is precharge by the VDD. The precharge circuit used for the new loadless 4T SRAM array is different from that of the 6T SRAM array.In the new loadless 4T SRAM array the bitlines are precharged to ground instead of VDD and thus consuming less power than the 6T SRAM array. The schematic of the pre-charge circuit for the new loadless 4T SRAM array is shown in Figure 4. In new loadless 4T SRAM has three NMOS transistors, which is precharge bits line by ground [1].

The sense amplifier is in charge of detecting what value is stored in an SRAM cell during read cycle and displaying that value at the output. Since only one row of data is accessed during each read cycle, each column of cells within the SRAM array requires only one sense amplifier [12]. A sense amplifier works by sensing a relatively small difference between the voltages of the two bitlines, then amplifying the difference at the output to show if a cell is storing either logic 1 or 0. The bitlines are precharged before each read cycle to ensure that the difference between the bitline voltages are caused by the value that is stored in the cell. If the bitlines are not precharged, there is a chance that the sense amplifier could misread and present an incorrect value at the output. Often times sense amplifiers are followed by an output buffer to ensure that the full logic level is shown at the output. There are two main sense amplifier categories; voltage sense amplifiers and current sense amplifiers [8].

The choice and design of a SA defines the robustness of bit line sensing, impacting the read speed and power. High density memories commonly come with increased bit line parasitic capacitances. These large capacitances slow down voltage sensing and makes bitline voltage swings energy-consuming, which result in slower and more power hungry memories. The need for larger memory capacity, higher speed, and lower power dissipation, impose trade offs in the design of SA. Also since SRAMs do not feature data refresh after sensing, the sensing operation must be non-destructive.



"***Figure 5. Sense Amplifier for 6T SRAM Cell [1] "***

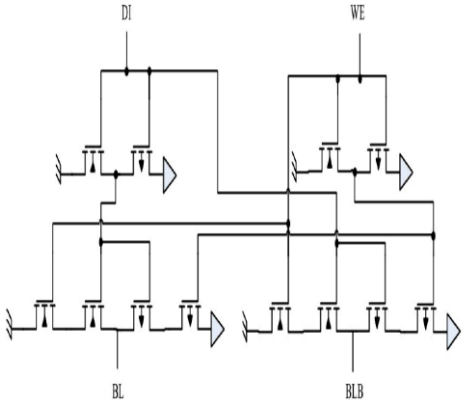


"***Figure 6. Sense Amplifier for new loadless 4T SRAM Cell [1] "***

Except the local precharge circuits both the versions of SRAM array use the same type of SA. Figure 5 shows the Sense amplifier for the 6T SRAM Cell and Figure 6 shows the Sense amplifier for the new loadless 4T SRAM Cell. Here precharge circuit is local level available. Each sense amplifier has owned precharge circuit.

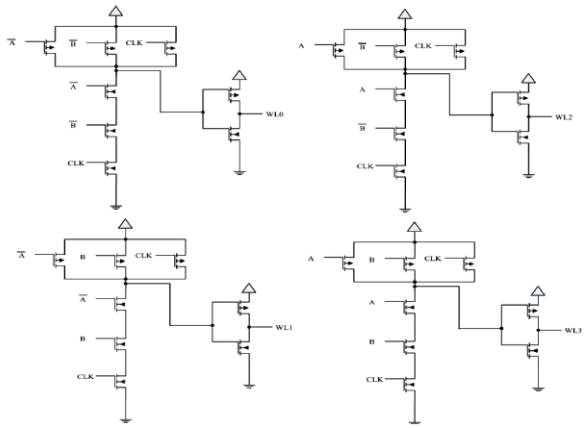
The function of the SRAM write driver is to write the input data to the bitlines when the Write Enable (WE) signal is enabled; otherwise the data is not written onto the bitlines. Only one write driver is needed for each SRAM column. Thus the area impact of a larger write driver is not multiplied by the number of cells in the column and hence the

write driver can be sized up if necessary. The function of the SRAM write driver is to quickly discharge one of the bit lines from the precharge level to below the write margin of the SRAM cell. Normally, the write driver is enabled by the Write Enable (WE) signal and drives the bit line using full-swing discharge from the precharge level to ground. The order in which the word line is enabled and the write drivers are activated is not crucial for the correct write operation [9]. The schematic of the write driver circuit is shown in Figure 7.



"***Figure 7. Write driver*** [1] "

A decoder is used to decode the given input address and to enable a particular WL(word line). There is various types of decoders available. Here we have the dynamic decoder used. Dynamic decoders [12] have the following advantages when compared to the other types of decoders. (a) The number of transistors used is less. (b) The layout of the decoder is simple and less time consuming. (c) The power consumption is less. (d) The speed of the decoder is also good. In particular dynamic CMOS AND gate decoder is used in rather than dynamic CMOS OR gate decoder, as the former consumes less area and less power than the latter. For a word memory, an m: n dynamic CMOS AND gate decoder is used, where m=log2n. The schematic of a 2:4 dynamic CMOS AND gate decoder is shown in Figure 8.



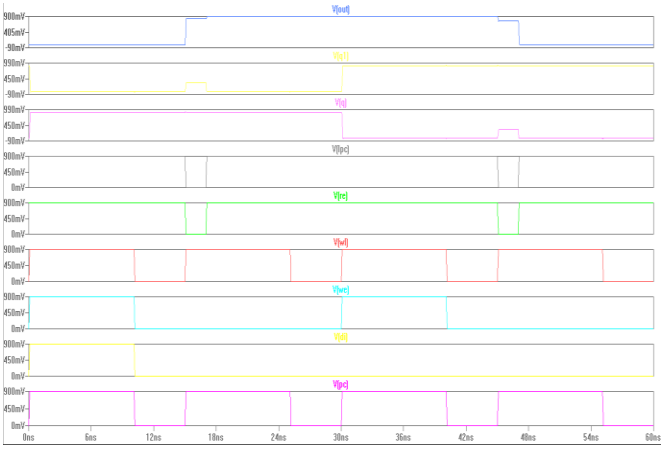
"***Figure 8. Dynamic CMOS AND Gate Decoder*** [13] "

III. OPERATION & SIMULATION RESULTS

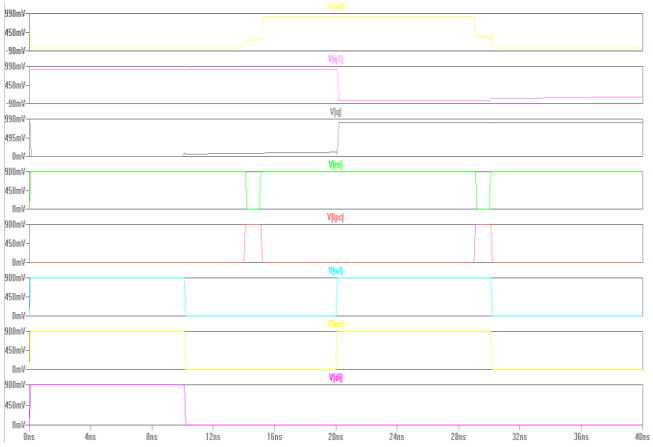
Firstly the write operation of the cell is described as follows. In order to store logic "1" to the cell, BL is charged to V_{dd} and BL' is charged to ground and vise versa for storing a logic "0". Then the wordline voltage is switched to V_{dd} to turn "on" the NMOS access transistors. When the access transistors are turned on, the values of the bitlines are written into Q and Q'. The node that is storing the logic "1" will not go to full V_{dd} because of a voltage drop across the NMOS access transistor. After the write operation the wordline voltage is reset to ground to turn "off" the NMOS access transistors. The node with the logic"1" stored will be pulled up to full V_{dd} through the PMOS driver transistors. The read operation of the cell is different from that of the 6T transistors. To read from the cell the bitlines are charged to ground instead of V_{dd} and the wordline voltage is set to V_{dd} to turn on the NMOS access transistors. The node with logic "1" stored will pull the voltage on the corresponding bitline up to a high (not V_{dd} because of the voltage drop across the NMOS access transistor) voltage level. The other bitline is pulled to ground. The sense amplifier will detect which bitline is at a high voltage and which bitline is at ground. If the cell was storing a logic "0" the voltage level of BL will be lower than BL' so the sense amplifier will output a logic "0". If the cell was storing logic "1" then the voltage level of BL will be higher than BL' then the sense amplifier will output a logic "1".

3.1 SIMULATION RESULTS

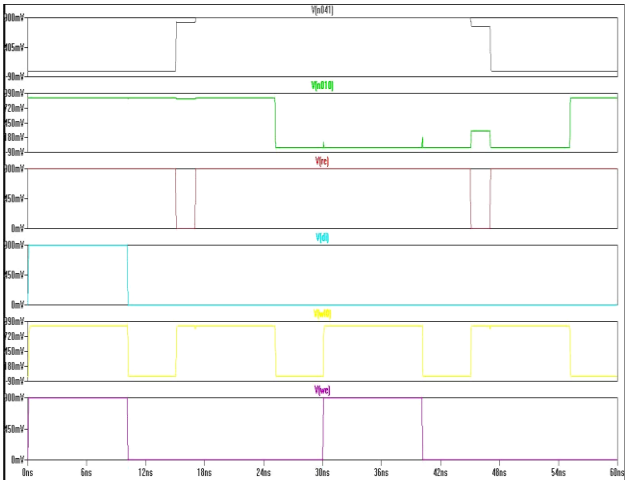
Write / read operation of 1-Bit, 16-bit, 64-bit and 1Kb 6T SRAM Cell is shown in Figure. 9, 11 and 13 accordingly. When WL is high, at that time access transistors turn on, and when WE is high at that time data is sent to the SRAM Cell through DI. The stored data is shown in the signal of Q and Q1. When the stored data is "1", it is called write 1. When WL is low, at time access transistors turn off so the stored data will retain. Also when WL is high and WE is low, data will be as it is. When WE is high and DI is low then data stored is "0", known as write 0. Write / read operation of 1-Bit, 16bit, 64-bit and 1Kb new loadless 4T SRAM Cell is shown in Figure. 10, 12 and 14 accordingly. New loadless 4T SRAM of read/write operation is same like 6T SRAM Cell. In this figure has write 1, write 0, read 1 and read 0, is same like 6T SRAM Cell with same stability. In figure has just precharge signal has changed while all other signals are same like 6T SRAM Cell.



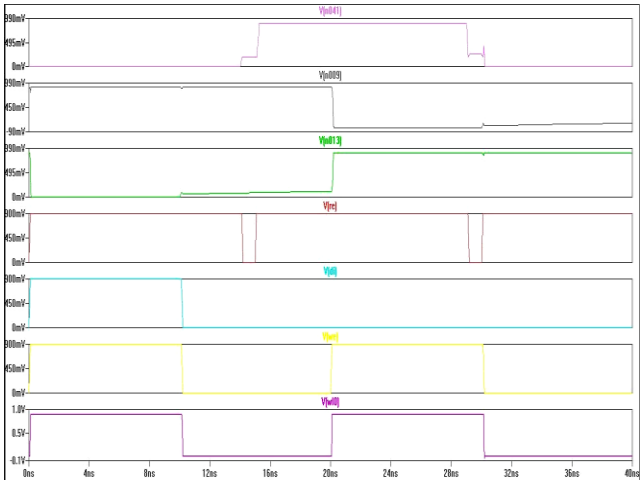
"***Figure 9. Read/Write operation of 1bit 6T SRAM cell "***



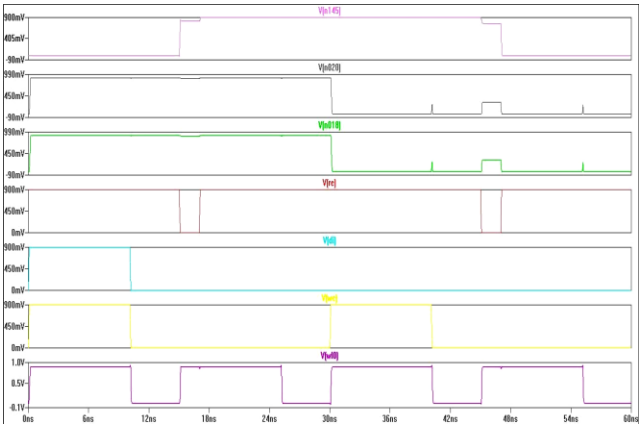
"***Figure 10. Read/Write operation of 1bit new loadless 4T SRAM cell "***



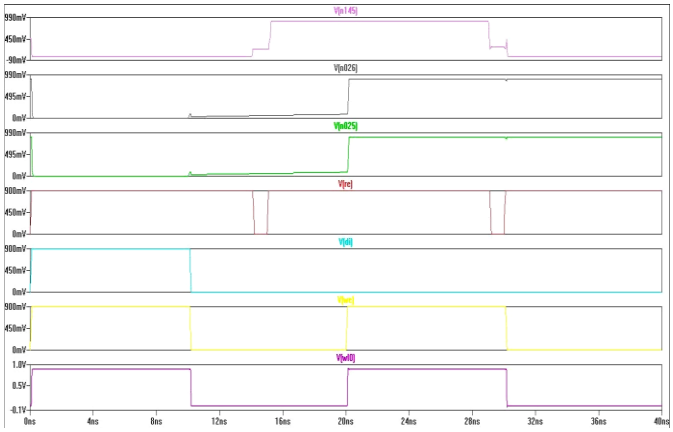
"***Figure 11. Read/Write operation of 16bit 6T SRAM cell "***



"***Figure 12. Read/Write operation of 16 bit new loadless 4T SRAM cell "***



"*Figure 13. Read/Write operation of 1Kb 6T SRAM cell* "



"*Figure 14. Read/Write operation of 1Kb new loadless 4T SRAM cell* "

IV. PERFORMANCE

The total number of transistors used for various configurations of SRAM arrays using both the types of SRAM cells has been tabulated as shown in Table 1. It is observed that for various configurations the new loadless 4T SRAM arrays uses lesser number of transistors and hence the lower area than that of the 6T SRAM array.

Configuration	Total Number of Transistors		
	6T SRAM	New loadless 4T SRAM	Reduction
1-bit	31T	29T	6.45%
16-bit	232T	200T	13.79%
64-bit	670T	542T	19.10%
1Kb	7402T	5354T	27.66%

"*Table 1. Comparison of Total Number of Transistors for Different Configurations*"

The total power dissipation (TPD) of various configurations of SRAM arrays using both the types of cells was measured and the results obtained have been tabulated. The comparison of TPD for different array configurations with CR=3 for 6T SRAM for New Loadless 4T SRAM in 32nm CMOS technology is shown in Table 2.

Configuration	Total Power Dissipation for 6T SRAM (in mW)	Total Power Dissipation for New loadless 4T SRAM(in mW)	Reduction
1-bit	0.00897mw	0.004614mw	48.56%
16-bit	0.04264mw	0.02397mw	43.78%
64-bit	0.0867mw	0.04862mw	43.92%
1Kb	1.2604mw	0.8468mw	41.36%

"*Table 2. Comparison of Power Dissipation for Different Configurations*"

The Access time was measured for both the types of 1Kb SRAM array and the results are tabulated. The Read Access time is the time measured from the point at which the RE signal reaches 10% of VDD to the point at which the output signal becomes +/- 10% VDD of the required logic value. The Write Access time is the time measured from the point at which the WE reaches 50% of VDD to the point at which the storage node of the cell reaches 50% of VDD. The access times for both the types of SRAM arrays with CR=3 are tabulated in Table 3 and 4.

Configuration	6T SRAM	New Loadless 4T SRAM
1-Bit	98.43ps	85.69ps
16-bit	104.67ps	90.83ps
64-bit	108.52ps	94.63ps
1Kb	1.8ns	0.86ns

"*Table 3. Comparison of Read Access Time for Different Configurations*"

Configuration	6T SRAM	New Loadless 4T SRAM
1-Bit	144.86ps	142.54ps
16-bit	148.37ps	146.95ps
64-bit	152.56ps	151.42ps
1Kb	178.63ps	169.25ps

"***Table 4. Comparison of write Access Time for Different Configurations"***

V. CONCLUSION

In this paper two types of SRAM cell is designed, namely 6T SRAM cell and new leadless 4T SRAM cell, using 32nm CMOS technology. By comparing results of both SRAM cell structures, it found that the working of new loadless 4T SRAM cell is same as that of 6T SRAM cell, but 4T SRAM structure requires less area. Also, in new loadless 4T SRAM cell, read access time is faster than that of 6T SRAM cell.

REFERENCES

[1] Sandeep R, Narayan T Deshpande, "Design and Analysis of a New Loadless 4T SRAM Cell in Deep Submicron CMOS Technologies" Second International Conference on Emerging Trends in Engineering and Technology, ICETET-09

[2] Jinshen Yang and Li Chen, "A New loadless 4-transistor SRAM cell with a 0.18µm CMOS technology" Electrical and Computer Engineering, CCECE Canadian Conference, pp. 538 – 541, April 2007.

[3] K. Noda, K. Matsui, K. Takeda, and N. Nakamura, "A Loadless CMOS Four-Transistor SRAM in a 0.18-µm Logic Technology," IEEE Transactions on Electronic Devices, pp.2851-2855, December 2001.

[4] Sreerama Reddy G.M and P. Chandrashekara Reddy, "Negative Word Line Scheme Based Low Power 8Kb SRAM for Stand Alone Devices" European Journal of Scientific Research ISSN 1450-216X Vol.26 No.2 (2009), pp.223-237

[5] James S. Caravella, "A Low Voltage SRAM for Embedded Applications", IEEE Journal of Solid-State Circuits, vol. 32, no. 3, pp. 428 – 432, March 1997.

[6] Kevin Zhang, Member, IEEE, Uddalak Bhattacharya, Zhanping Chen, Member, IEEE, Fatih Hamzaoglu, Daniel Murray, Narendra Vallepalli, Member, IEEE, Yih Wang, Member, IEEE, B. Zheng, and Mark Bohr, Fellow, IEEE, "SRAM Design on 65-nm CMOS Technology With Dynamic Sleep Transistor for Leakage Reduction"

[7] Ming-Long Fan, Student Member, IEEE, Yu-Sheng Wu, Student Member, IEEE, Vita Pi-Ho Hu, Student Member, IEEE, Chien-Yu Hsieh, Pin Su,Member, IEEE, and Ching-Te Chuang, Fellow, IEEE- Comparison of 4T and 6T FinFET SRAM Cells for Subthreshold Operation Considering Variability—A Model-Based Approach IEEE TRANSACTIONS ON ELECTRON DEVICES, VOL. 58, NO. 3, MARCH 2011

[8] Ingvar Carlson – "Design and Evaluation of High Density 5T SRAM Cache for advanced Microprocessors" Master's thesis performed in Electronic Devices by Ingvar Carlson Reg nr: LiTH-ISY-EX-3481-2004, 23rd March 2004

[9] Mohammad Sharifkhani "Design and Analysis of Low-power SRAMs"- thesis Waterloo, Ontario, Canada

[10] Andrei Pavlov and Manoj Sachdev, "CMOS SRAM Circuit Design and Parametric Test in Nano-Scaled Technologies", Springer, 2008

[11] Tegze.P.Haraszti, "CMOS Memory Circuits", Kluwer Academic Publishers

[12] Anantha Chandrakasan – " High-Performance Energy-Efficient Microprocessor Design – Springer

[13] Sung-Mo Kang and Yusuf Leblebici, "CMOS Digital Integrated Circuits", TMH, 2003.

